Weekly Report for Yu Hu's work from Sep. 5 to Sep. 11

September 11, 2005

1. **Integrate Jinjun's vBuf package into BIC package.** The integrated vBuf package (2-parameter based buffer insertion considering process variation) now share the same input file formats for net description, buffer library. Also the technical parameters (such as unit length wire resistance and capacitance) and variation settings can now be costumed by users in an input file. All testcases in Jinjun's ICCAD'05 submission are tested to check the correctness of the integration. Besides, a little tool for translating vBuf's input net file format to BIC's is included in the integrated package. Users can generate more vBuf testcases and translate them to BIC compatible format with it. The integrated package can be found in cvs dir "BIC_package".

2. **Papers reading.** I read several papers about timing budgeting and package routing. The summary and comments of these paper can be found in the websites `http://eda.ee.ucla.edu/member_only/time-budgeting` and `http://eda.ee.ucla.edu/member_only/package-routing`, respectively. For the timing budgeting problem, I have discussed with Jinjun and there are the following ideas,

   Topic - Simultaneous buffer insertion, voltage assignment and gate sizing for power minimization with timing constraints.

   Problem formulation (beta version) - There exist some literature for power minimization with timing budgeting, but generally the approach used for power reduction is all gate sizing. However, it'll be more practical if we can add buffer insertion into consideration. Besides buffering, voltage assignment is another efficient way to manage power based on the given slack allocation. At the same time, simultaneous buffer insertion, voltage assignment and gate sizing bring us more challenges as the problem becomes more complicated. To formulate this problem, we treat the given circuit as a directed acylic graph (DAG). My initial idea is to use the following LP as the problem formulation,

$$\begin{array}{lll} \max & \sum s_i d_i & \\ s.t. & AT_i > AT_j + d_i^0 + d_i & \forall j \in FI(i) \\ & AT_o \leq RAT & \forall o \in PO \end{array} \tag{1}$$

   where $s_i = \delta Power/\delta Delay$ is the power-delay sensitivity of node i. This formulation is almost the same with [Murari Mani et at DAC'05], but we allow negative slack in Eq. 1. The negative slack means that the timing constraint is broken and we have to insertion buffers. On the other way, the positive slack means that we can reassign the voltage level or resize the gates to reduce more power. I'll keep working on refining the formulation.