A STATISTICAL MODEL OF INPUT GLITCH PROPAGATION AND ITS APPLICATION IN POWER MACROMODELING

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ABSTRACT

Power macromodeling technique can result in huge underestimation without the consideration of input glitches. In this paper, we propose a statistical model for the propagation of input glitches and their effects on circuit power consumption. Based on this model, we develop an analytical power macromodeling approach incorporating input glitches. Specifically, we divide the macromodel parameter space into three regions and characterize each region separately. We have evaluated the proposed technique on ISCAS85 and LGSynth93 benchmark circuits. Compared with switch level simulation results, the average power estimation errors are 1.8% and 3.1% for combinational and sequential circuits, respectively. Our model also provides useful insight for glitchy circuit identification and input glitch power reduction.

1. INTRODUCTION

Power estimation techniques based on power macromodeling proceed in two phases. In the characterization phase, synthetic input signals of different statistics are used to simulate a given circuit block to derive the power dissipation. Power macromodels are created based on the relation between the signal statistics and power dissipation. In the estimation phase, the actual signal statistics are computed and applied to the power macromodels for the power estimates.

In the actual operating condition, input signals of a circuit may contain glitches that are generated by the previous stage circuitry. Unless registers are placed at every input nodes, these glitches can propagate into the circuit and increase circuit power dissipation significantly. To guarantee accurate estimation results, it is important to include input glitch information into power macromodels.

In this paper, we present a statistical model for the propagation of input glitches and their effects on circuit power consumption. Based on this model, we propose a novel power macromodeling scheme that incorporates input glitch power effect. Specifically, we divide the input parameter space into 3 regions based on the average input glitch duration and derive an individual power macromodel function in each region. In the estimation phase, the macromodel corresponding to the actual input glitch duration is used to compute the power estimate.

We applied our macromodeling approach on ISCAS85 and LGSynth93 benchmark circuits to demonstrate its high effectiveness. For combinational circuits, the average and maximal errors of the power estimation are 1.8% and 10.2% on the average, respectively. For the sequential circuits, the average and maximal errors are 3.1% and 20.9% on the average, respectively. Our macromodel not only provides superior estimation accuracy but also indicates ways of reducing input glitch power.

Power macromodeling has been investigated using various signal statistics and different mapping approaches. A look-up table (LUT) approach was introduced in [7] and improved in [1]. The LUT stores power estimates for equally-spaced discrete values of the input statistics. Interpolation is used to obtain estimates for statistics not in the LUT. The notion of power sensitivity was introduced in [4, 5] for improving the accuracy of interpolation. In this approach, discrete planes are used to approximate the power surface and reduce the large memory requirements of the LUT. Analytical power macromodeling uses mathematical expressions to map input signal statistics to power dissipation, thus avoiding the space cost of LUT approaches [2, 8]. The application of power macromodeling on system designs was discussed in [9]. That work assumes a pure register interface, however, and does not consider the propagation of glitches among circuit blocks. The combination of glitch analysis and analytical power macromodeling was first investigated in [10].

The remainder of the paper has 5 sections. In Section 2, we give the background on glitch and analytical power macromodeling. In Section 3, we describe our statistical glitch propagation model and derive the relation between average input glitch duration and circuit power dissipation. We present our power macromodeling technique in Section 4. Our experiments are given in Section 5. We summarize our paper in Section 6.

2. BACKGROUND

2.1. Glitching in Static CMOS

In static CMOS circuits, due to the imbalance of delays among the different combinational paths ending at the output of a gate, the output signal might switch more than once within a clock period before it stabilizes. These extra transitions are called glitches. Figure 1 gives an example of glitch generation. The signals at the two inputs of the AND gate **b** change at different times, resulting in a pulse in the output signal. Once created, glitches can propagate through gates as seen at the output of inverter **c** in Figure 1. There are two conditions under which glitches can be terminated. First, if some other input has the controlling signal as in gate **e**, a glitch will not propagate to the output no matter how strong it is. Second, if the duration of an input glitch is too short compared to the delay of a gate, it will not result in a considerable swing at the output node. This fact is illustrated by the inverter **d** in Figure 1, in which case the output signal change can be ignored.

In CMOS circuits, power dissipation is mainly due to transition activities of the signals, a large portion of which can be due to glitches. Glitches are known for contributing 20% to 70% of total power dissipation in static CMOS circuitry, even with glitch-free

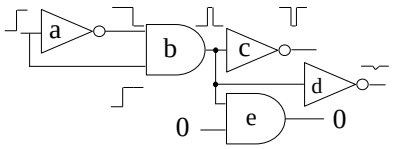

Figure 1: Generation, propagation, and termination of a glitch

inputs [3, 13]. As a result, glitch estimation and reduction have been one of the most active research areas in low power circuit design [6, 11, 12].

2.2. Analytical Power Macromodel

In analytical power macromodeling, a function g maps the space of input/output signal properties to the power dissipation of a circuit. When the input parameters of g are solely determined by the input signals, the computation of power estimates is a straightforward and fast function evaluation. The key challenges in analytical macromodeling are the choice of appropriate function template and input parameters for the macromodel.

The most commonly used templates for the macromodel function g are low-order polynomial functions. For a kth order complete polynomial function with n input parameters, a total of C^k_{n+k} coefficients need to be computed.

Three input parameters are widely used in power macromodels: the average input signal probability P_{in}, the average input transition density D_{in}, and the input spatial correlation S_{in} [2]. Although P_{in}, D_{in}, and S_{in} are effective in capturing the statistics of the input signals, they do not contain input glitch information, because they are calculated using clock period as the time unit. Additional input parameters are required to include the input glitch effect into analytical power macromodels.

Input glitches increase power dissipation by propagating into circuits and generating a high level of signal activity. The more input glitches a circuit has, the more power it consumes. Wider input glitches propagate longer and generate more activity, therefore, resulting in more power dissipation. In [10], glitch frequency G_f, which is defined as the average number of glitches per input node per clock cycle, and average glitch duration G_d are used to characterize input glitches and analyze their power impact.

Figure 2(a) shows the relation between the power dissipation of c1908 circuit in ISCAS85 benchmark and input glitch durations with sequences of different G_f. The P_{in}, D_{in} and S_{in} are 0.5, 0.5, and 0.25, respectively. It is found that, even with input glitch frequency as low as 0.04, power dissipation can increase by up to 25%. Figure 2(b) shows the same relation but with input sequences of different P_{in}, D_{in} and S_{in}. The input glitch frequency G_f is set to 0.04. Again, significant power increase due to input glitching is observed. Therefore it is essential to include input glitch information to any macromodel to ensure power estimation accuracy. As a result, the power macromodel function becomes

$$\mathcal{P} = g(P_{in}, D_{in}, S_{in}, G_f, G_d)\,, \tag{1}$$

where $\mathcal{P}$ is the circuit power dissipation.

The power effect of each individual parameter K can be analyzed using the *power sensitivity* to K, which is defined as:

$$\lim_{\Delta K \to 0} \frac{\Delta \mathcal{P}}{\Delta K}\,. \tag{2}$$

In analytical power macromodeling, power sensitivity is computed as the partial derivative of the power macromodel function g.

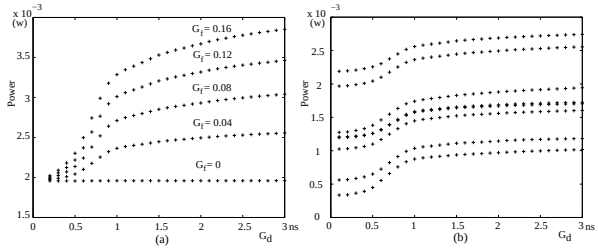

Figure 2: Power dissipation vs G_d for various (a) G_f and (b) signal statistics

3. INPUT GLITCH MODELING

In this section, we present our statistical model for input glitch propagation and its power effect.

We first introduce some notation. The *input combinational path length* is the average gate number on a combinational path between a primary input node and a register or a primary output node. It provides an upper bound for the number of gates that an input glitch can propagate through in a circuit. The *average blocking probability* is the average probability that a glitch cannot propagate through a gate because some other input has the controlling signal. This value is determined by the circuit structure and the input signal statistics.

To simplify our model, we assume that glitches never merge. Theoretically, two glitches can merge if they propagate to the same node at the same time. However, the probability of such a case is very small in actual circuits because the glitch frequency is usually very low. Furthermore, we assume that a glitch terminates at the input of a gate if the gate delay is larger than the glitch duration. Otherwise, the glitch propagates through the gate without changing its duration. This assumption simplifies the wave form of glitches and can introduce power estimation error. However, as we show in Section 5, the error is very small when we estimate *average* power dissipation.

The following theorem gives the relation between the duration of an input glitch y and the number of glitches generated by y.

Theorem 1 *Given a circuit with input combinational path length l and average fanout m, let p_b be the average blocking probability and $f(x)$ be the probability density function of a gate delay being x, then the average number of glitches that are generated in the circuit by an input glitch of duration D can be derived as:*

$$N_{avg}(D) = \frac{1-(mp)^{l+1}}{1-mp}\,, \tag{3}$$

where $p = (1-p_b)\int_0^D f(x)dx$.

Proof. (sketch) Based on our assumptions, all glitches due to input glitch propagation have duration D. Therefore, a glitch can propagate through a gate if the gate delay is shorter than D and the glitch is not blocked by other controlling signals. Since these two conditions are independent, we have $p = (1-p_b)\int_0^D f(x)dx$ is the probability that a glitch can propagate through a gate.

We then use induction to prove that, starting from the input, on the average, there are $(mp)^k$ glitches on the kth level downstream of the circuit. The proof for $k = 1$ is easy. If the glitch passes the first gate there will be m glitches, otherwise there is no glitch. Therefore, the average number of glitches is pm. We next assume that the statement is true for $k \le k_0$ and prove the case of $k =$

$k_0 + 1$. The probability that certain number of glitches propagate from k_0th level to $(k_0 + 1)$th level follows binomial distribution. Therefore the average number of glitches at $k_0 + 1$ level is

$$\begin{aligned} n_{k_0+1} &= \sum_{n=0}^{\infty} p_r(n) \cdot \sum_{x=0}^{n} x \cdot \binom{x}{n} p^x (1-p)^{(n-x)} \cdot m, \\ &= \sum_{n=0}^{\infty} p_r(n) \cdot n \cdot m \cdot p = (mp)^{(k_0+1)}, \end{aligned} \tag{4}$$

where $p_r(n)$is the probability that there are n glitches at level k_0. Total number of glitches generated is therefore computed as

$$N_{avg}(D) = \sum_{k=0}^{l} (mp)^k = \frac{1-(mp)^{l+1}}{1-mp}. \tag{5}$$

□

Figure 3 shows the relation between the input glitch duration and the number of glitches generated according to Theorem 1. The gate delay distribution is a Gaussian distribution with a mean of 2ns and a standard deviation of 1ns. The average fanout and input combinational path length are set to 2 and 8, respectively.

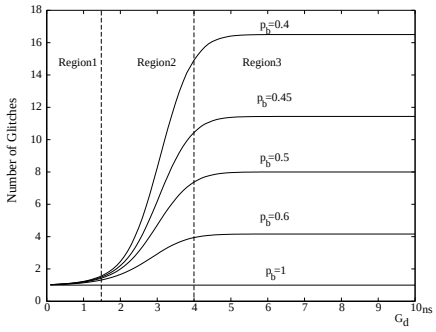

Figure 3: G_d vs the number of glitches generated

As a first order of approximation, the extra energy dissipation $\mathcal{E}_{ig}$ due to input glitches can be computed using the number of glitches generated within a circuit as

$$\mathcal{E}_{ig} = C_{ave} \cdot V_{dd}^2 \cdot N_{avg}(G_d), \tag{6}$$

where C_{ave} is the average node capacitance and V_{dd} is the voltage of power supply. (The leakage power is relatively constant and hardly affected by glitches.) Since C_{ave} and V_{dd} are constant, the glitch power curves will have the similar shape as those in Figure 3. Total circuit power dissipation curves can be derived by shifting the glitch power curves up by a constant value, which is the power consumption with glitch-free inputs. The similarity between Figure 3 and simulation results in Figure 2(a) demonstrates the validity of our model.

4. POWER MACROMODEL WITH INPUT GLITCHES

Though our model can describe the power effect of input glitches fairly well, some parameters in the model, such as average blocking probability p_b and the gate delay density function $f(x)$, are difficult to compute. Nevertheless, a key observation of Figure 3 reveals that the dependency of power on input glitch duration can be divided into 3 regions. Theorem 1 indicates that the middle region is the range of most gate delays in the circuit. This range is *independent* of input signal statistics. Therefore, we propose to divide the input parameter space into 3 regions based on the power sensitivity to input glitch duration and create a power macromodel in each region.

Our characterization phase proceeds as follows. We simulate a given circuit using sequences of various statistics and input glitch distributions to build the power macromodel as in [10]. We then compute the power sensitivity to input glitch duration $\mathcal{S}_{G_d}$ for a randomly chosen (P_{in}, D_{in}, S_{in}, G_f). The G_d values whose power sensitivities are equal to $(\max\{\mathcal{S}_{G_d}\})/2$ are chosen to divide the parameter space into 3 regions. This procedure is illustrated in Figure 4. (The region division result can vary slightly when a power curve of different (P_{in}, D_{in}, S_{in}, G_f) is used. However, our experimental results show that such small variation causes little change in the power estimation accuracy.)

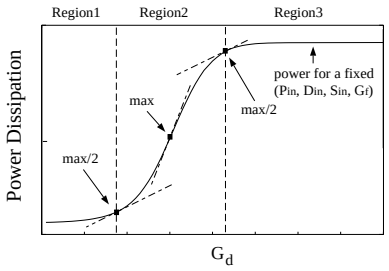

Figure 4: The division of macromodel parameter space

In all three regions, the complete 3rd order polynomial function is used as the template to create new macromodels. In order to achieve a smooth transition between adjacent regions, the data points around region boundary are used in the macromodel derivation of both regions. The complexity of the proposed characterization procedure is almost the same as that in [10], because no more time consuming simulation is required. Only 3 more macromodel fitting procedures are performed.

5. MACROMODEL EVALUATION

In this section, we evaluate our power macromodel using the ISCAS85 and LGSynth93 benchmark circuits.

In our characterization procedure, we sampled the input parameter space into 6,600 points. The parameters P_{in}, D_{in}, and S_{in} varied from 0.05 to 0.95 with a granularity of 0.1. G_f ranged from 0.1 to 0.5 with a granularity of 0.1. G_d ranged from 0.1ns to 3.0ns with a 0.5ns difference. The ranges for G_f and G_d were determined by computing the average output glitch frequency and duration of circuits with glitch-free inputs. The clock period was set to 100ns so that all signal propagation could complete. Each circuit was simulated for 2,000 clock periods using Delft University's switch-level simulator SLS for power dissipation. The *MATLAB* function *nlinfit* was used to fit all power macromodels.

To evaluate the accuracy of the proposed macromodel, for each circuit, we specified 348 vectors in the 5-dimensional input parameter space. These vectors were substantially different from those in the characterization to avoid correlation between characterization and estimation. The parameters P_{in}, D_{in}, and S_{in} ranged from 0.1 to 0.9 with a granularity of 0.2. G_f took on values from the set $\{0.15, 0.25, 0.35, 0.45\}$, and G_d was from the set $\{0.2, 0.9, 1.6\}$. For every statistics combination, we generated the corresponding sequences of input signals and simulated the

Table 1: Estimation accuracy for combinational circuits

Circuit	ϵ_{ave}(%)	ϵ_{max}(%)
c432	2.37	8.48
c499	0.94	5.35
c880	5.36	49.57
c1355	0.99	4.71
c1908	1.36	4.69
c2670	1.44	4.58
c3540	0.97	5.23
c5315	1.22	5.86
c6288	2.59	9.56
c7552	0.78	3.66
Average	1.80	10.17

Table 2: Estimation accuracy for sequential circuits

Circuit	ϵ_{ave}(%)	ϵ_{max}(%)
s1423	2.39	13.05
s280	3.26	40.30
s420	3.37	11.06
s628	4.00	17.93
s723	4.13	37.90
s838	3.64	19.71
s937	1.18	6.48
Average	3.13	20.92

circuits using SLS. The power dissipation results from the simulations were then compared with the values derived by our analytical power macromodels.

Our experimental results are given in Tables 1 and 2. Our macromodels can provide highly accurate power estimates for all circuits. The average absolute estimation error is 1.8% for combinational circuits, on the average. The corresponding maximal estimation error is 10.17%, on the average. For sequential circuits, average and maximal estimation errors are 3.13% and 20.9% on the average, respectively.

Our model of input glitch propagation also provides insight for glitchy circuit identification and glitch power reduction. By computing the power sensitivity to input glitch duration, we can check whether the power dissipation of a given circuit increases significantly under glitchy inputs. For circuits that are sensitive to input glitches, our model provides two possible ways of reducing glitch power. First, the gate delay density function $f(x)$ can be adjusted by replacing fast gates by slow ones on the non-critical paths. This approach will reduce glitches by decreasing p in Theorem 1. Second, retiming can be applied to reduce the input combinational path length l. (Input glitching power can be eliminated by inserting registers at every input nodes of a circuit. This approach, however, introduces one more pipeline stage and, therefore, might be infeasible in certain designs. Furthermore, the inserted registers can dissipate extra power.)

6. CONCLUSION

This paper presents a statistical model for the propagation of input glitches and the effect on circuit power consumption. Based on this model, an analytical power macromodeling technique that considers the input glitch power effect is proposed. Specifically, in the proposed approach, the macromodel parameter space is divided into 3 regions based on input glitch duration and an individual macromodel is created in each region. Experimental results using ISCAS85 and LGSynth93 benchmark circuits demonstrate the high accuracy of our technique. The average estimation errors are 1.8% and 3.1% for combinational and sequential circuits, respectively. Our model also indicates possible ways of identifying glitchy circuits and reducing input glitching power.

7. ACKNOWLEDGMENTS

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