Introduction to Chip-Package Co-design

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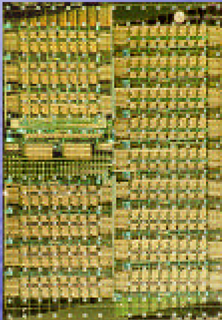
Outline

- Background and motivation
- Chip Package Co-design Flow
- Signal Integrity
  - Simultaneous Switching Noise
- Power Integrity
  - Plane impedance and resonance
- Conclusion

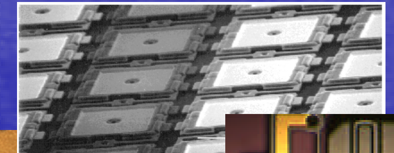
Heterogeneous Systems Integration

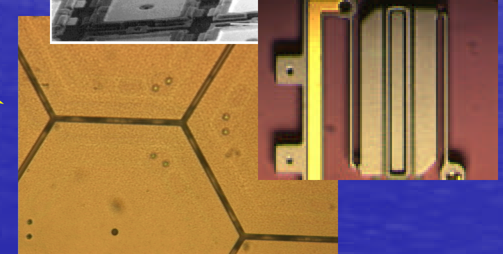
CMOS VLSI
- Full Custom
- RF Telemetry
- ASIC
- Embedded Core



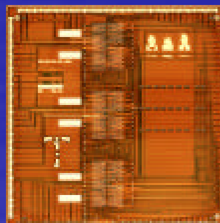
Novel System Integration
- Human-computer interfaces
- Enhanced capabilities
  (eg. smart sensors and actuators)
- High complexity
  (eg. bio-complexity)

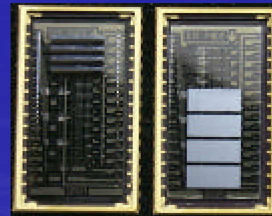
MEMS
- Bulk
- Surface
- Emboss
- Other





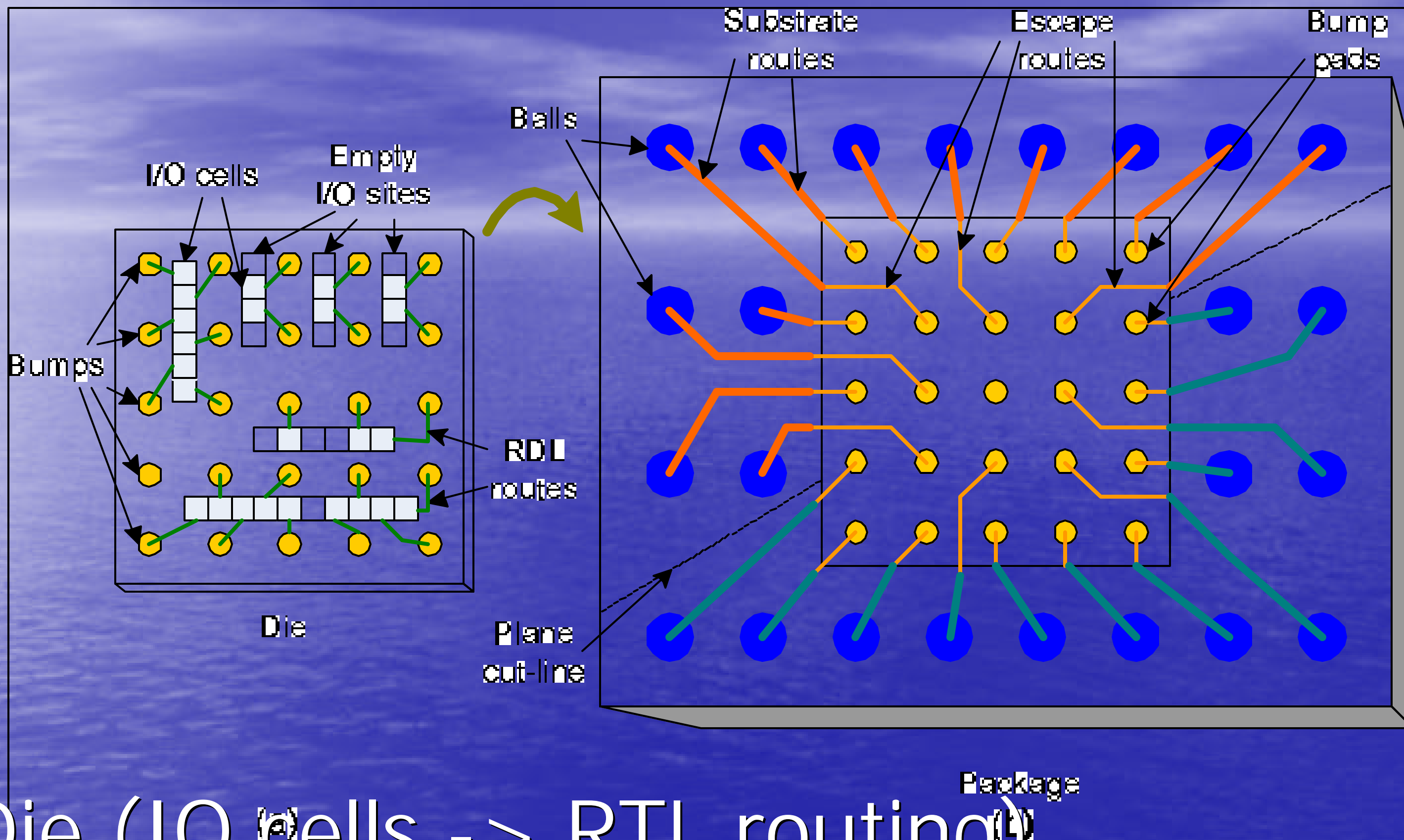
Advanced Packaging
- Seamless integration
- Embedded Passives





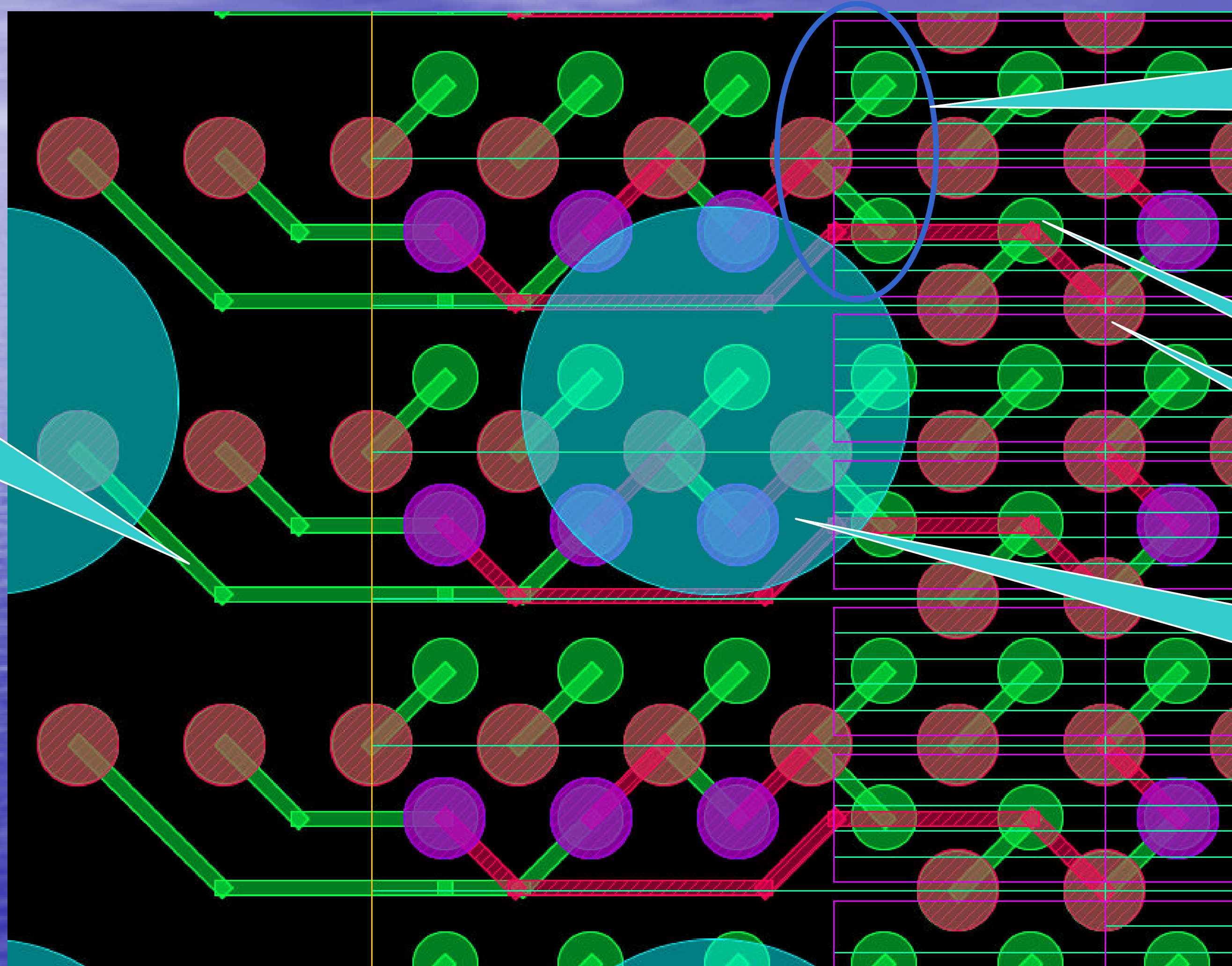
(From P. Franzon)

Connection from die to board



- Die (IO cells -> RTL routing)
- -> package (bumps -> escape routing -> balls)
- -> board

Top View of Layout



Escape routes

Two P/G bumps sharing a via

Bump

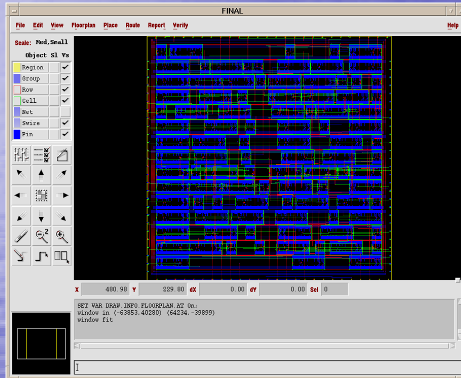
Via

Ball/Via in one view

VLSI-Centric Design (Problematic)

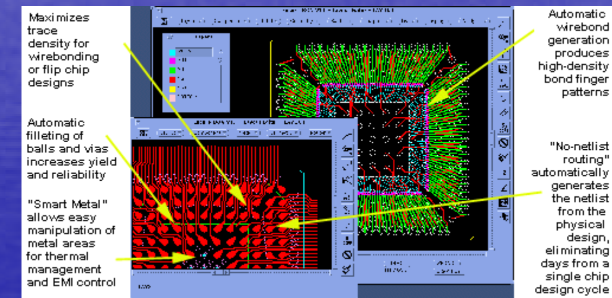
- IC and package tools very separated:

IC Physical Design

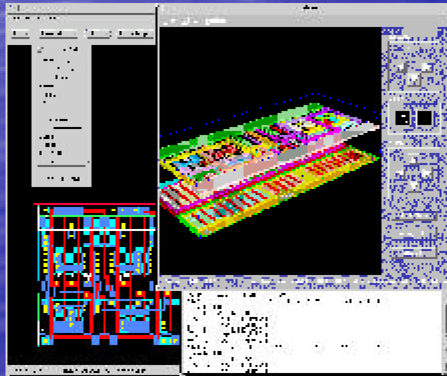


I/O Locations
IBIS Models

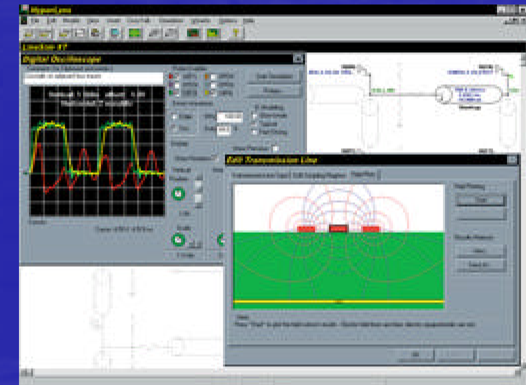
Package Physical Design



IC Modeling/Simulation



Package Modeling/Simulation



(From P. Franzon)

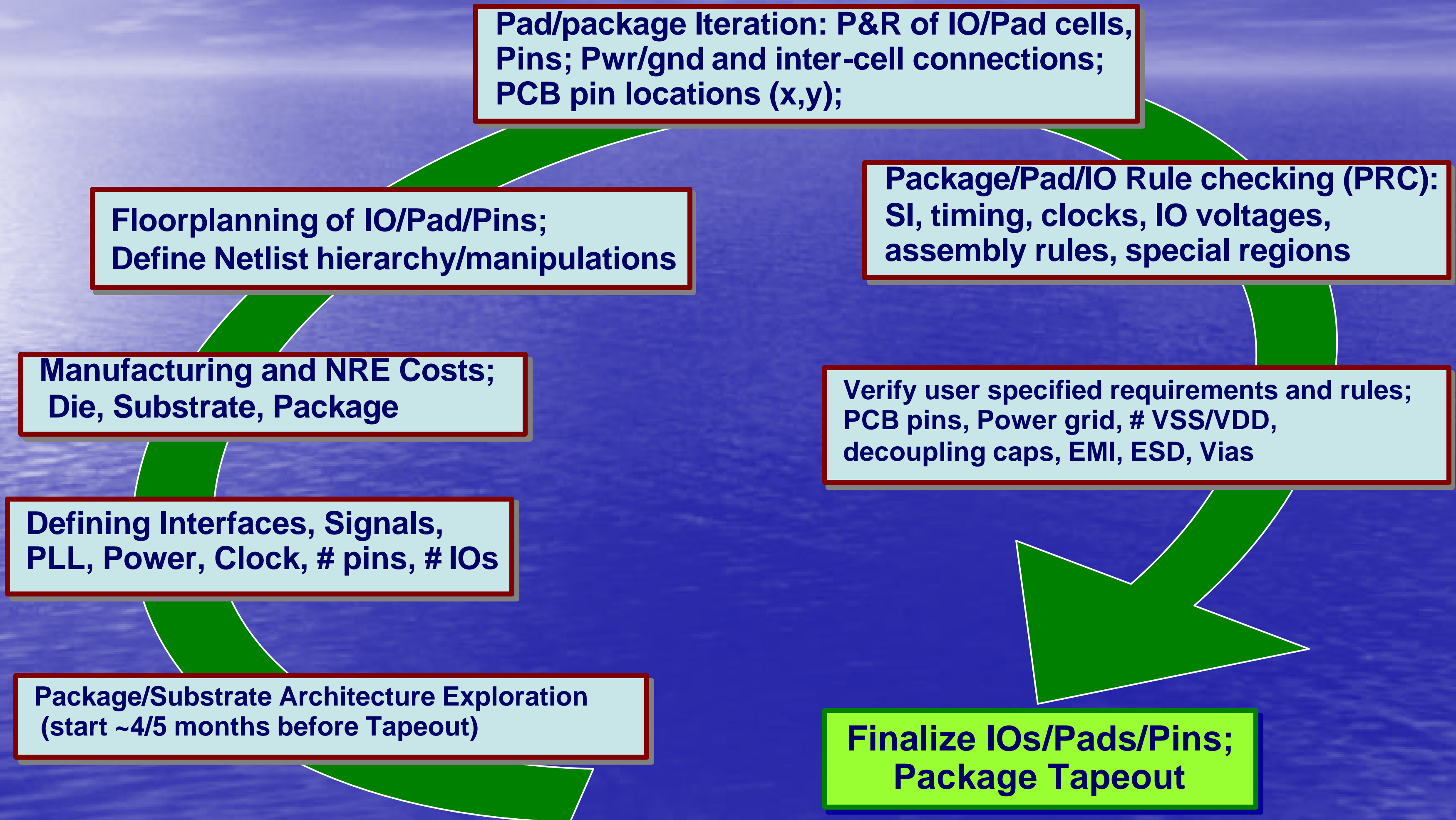
On-Chip Design Concerns

- Physical Concerns
  - Die Netlist Connectivity (logic cells to IO cells)
  - System Connectivity (IO cells to package)
  - Power Network Design
- Electrical Concerns
  - Core Timing Constraints
  - System Timing Constraints
  - Power Budget
  - Signal Integrity and Reliability Constraints
    - Supply voltage scaling imposes very tight noise margins on chip and package designs
    - Significant noise contribution from core switching
    - But greater on-chip exposure to package-side SSN

Package Design Concerns

- Physical Concerns
  - Reduce Package Cost
  - Reduce Stack-up Layers
  - Optimize Decoupling Capacitance
- Electrical Concerns
  - Reduce AC Noise Effects
  - Low Impedance Power Distribution System
  - Meeting Timing Constraints

Typical Package Design Cycle



Needs for Co-Design

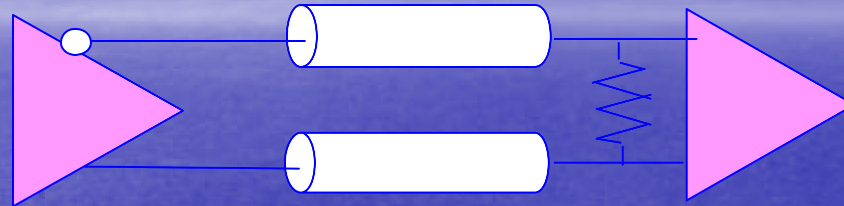
- High-frequency Designs
  - 400 MHz buses becoming common
  - On-chip exposure to package noise
    - Simultaneous switching noise
    - Package resonance
- Tighter Turnaround Time
  - Package design convergence
  - System design convergence
- High Density Packaging

High Density Packaging Trends

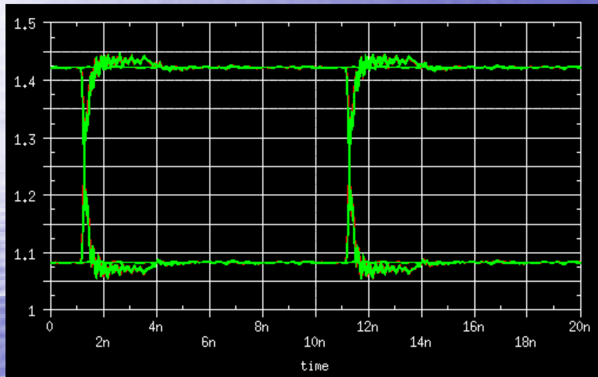
- Short Term
  - Increased penetration of Direct Chip Attach (DCA) (solder balls) and Chip-On-Board (COB)
    - On-chip design and functionality suffer due to the increased scope of package-induced SSN
    - Layout difficulties due to high pin count systems
    - Routing resources becoming very tight, flip-chip escape routing is difficult
- Long Term
  - Package technology *adding value* to the system
    - High density, low-cost packaging
    - Meet design constraints for both SI and PI

(From P. Franzon)

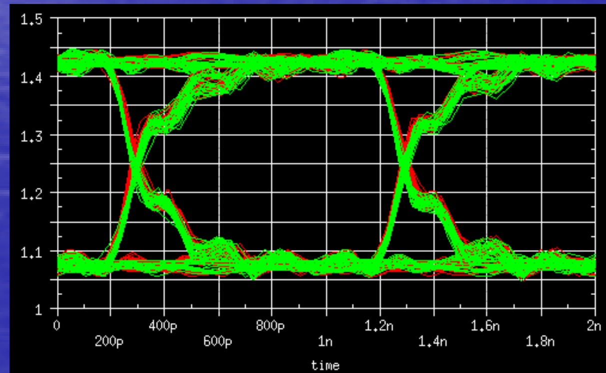
Eye Diagram for LVDS with Frequency Dependent Coupled Transmission Lines



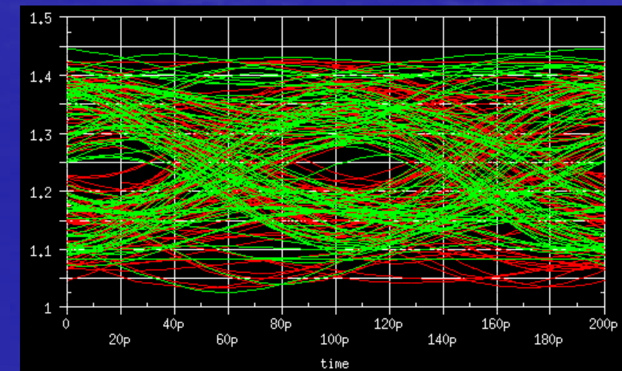
100Mbit/sec



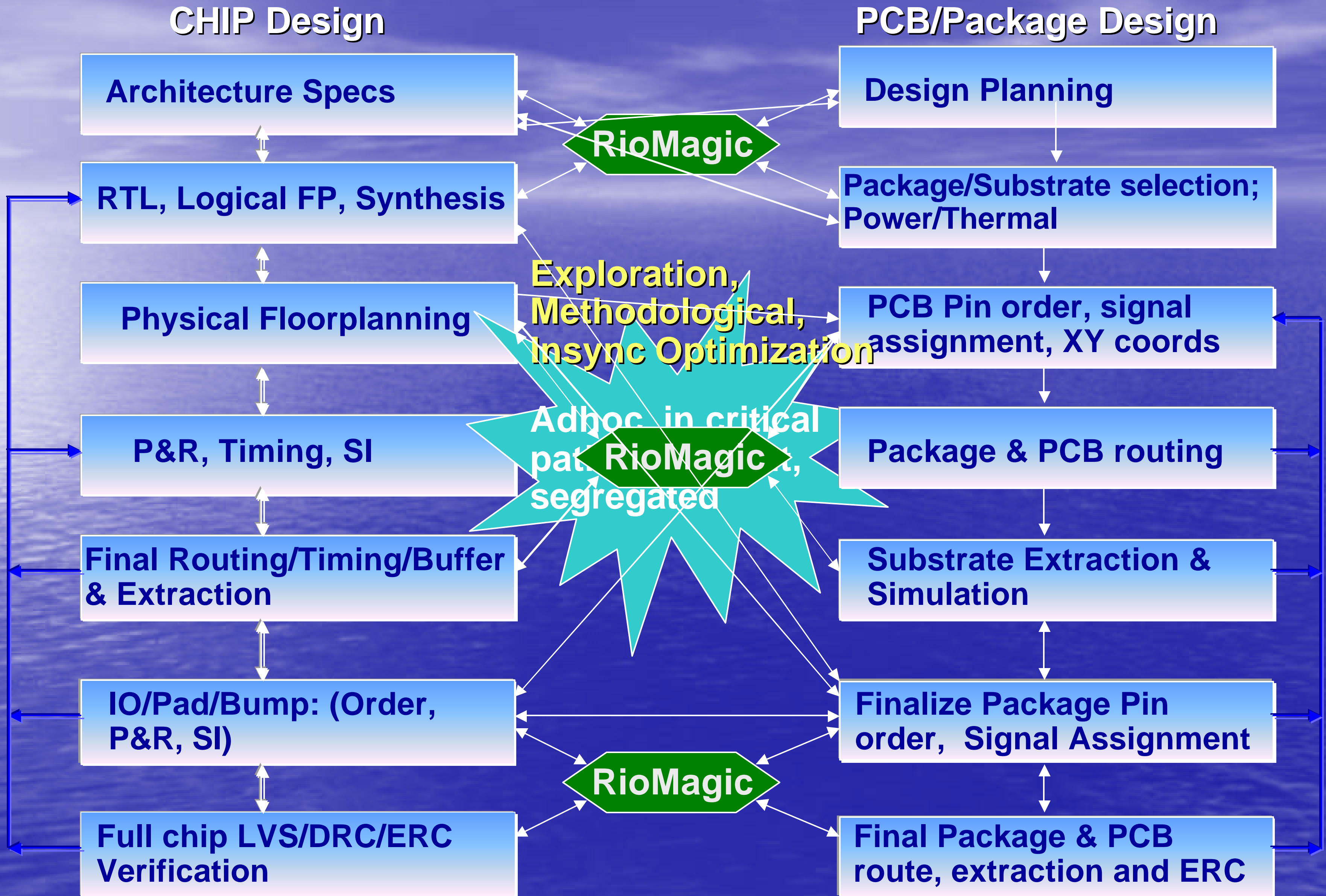
1Gbit/sec



10Gbit/sec



A Co-Design Flow with RioMagic



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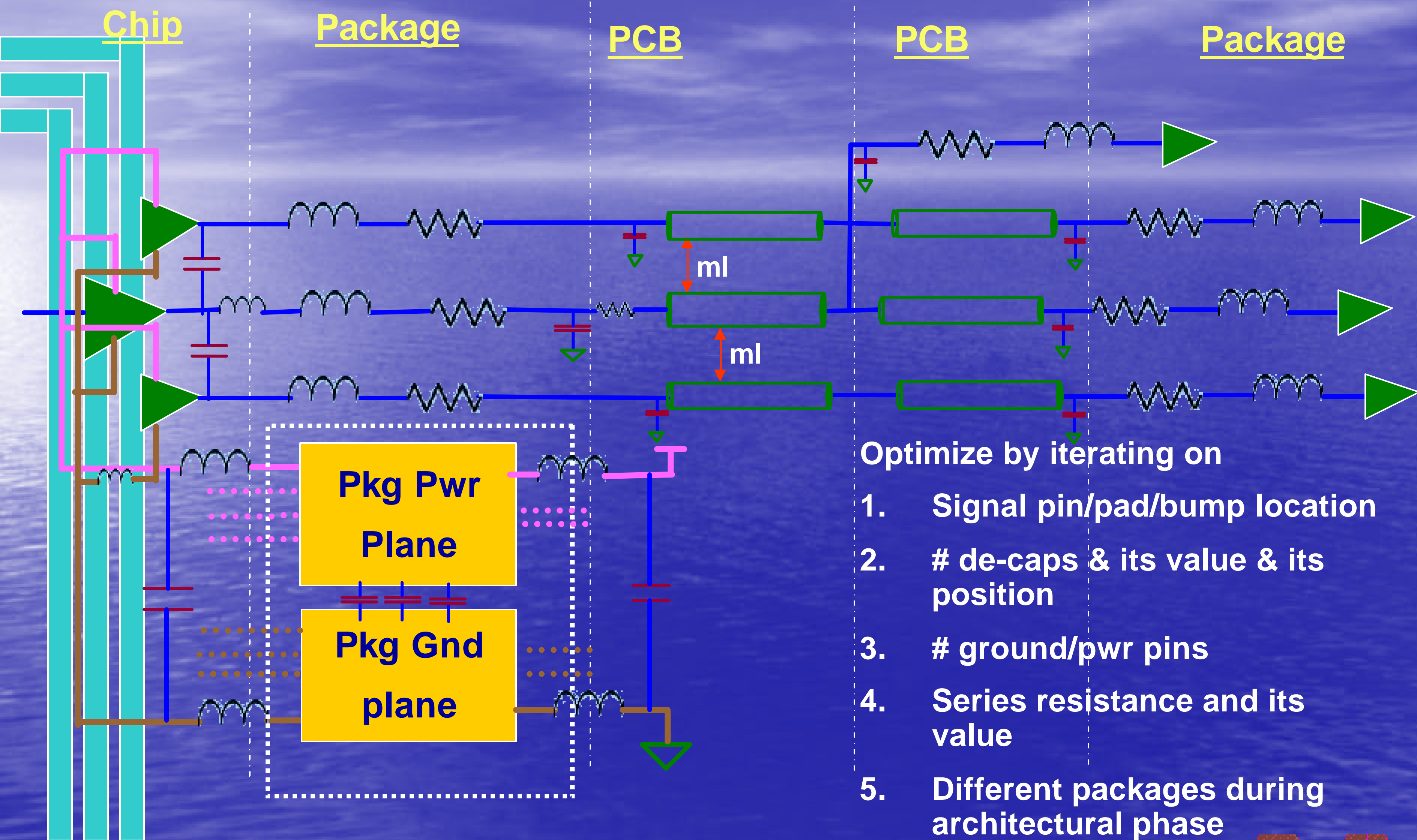
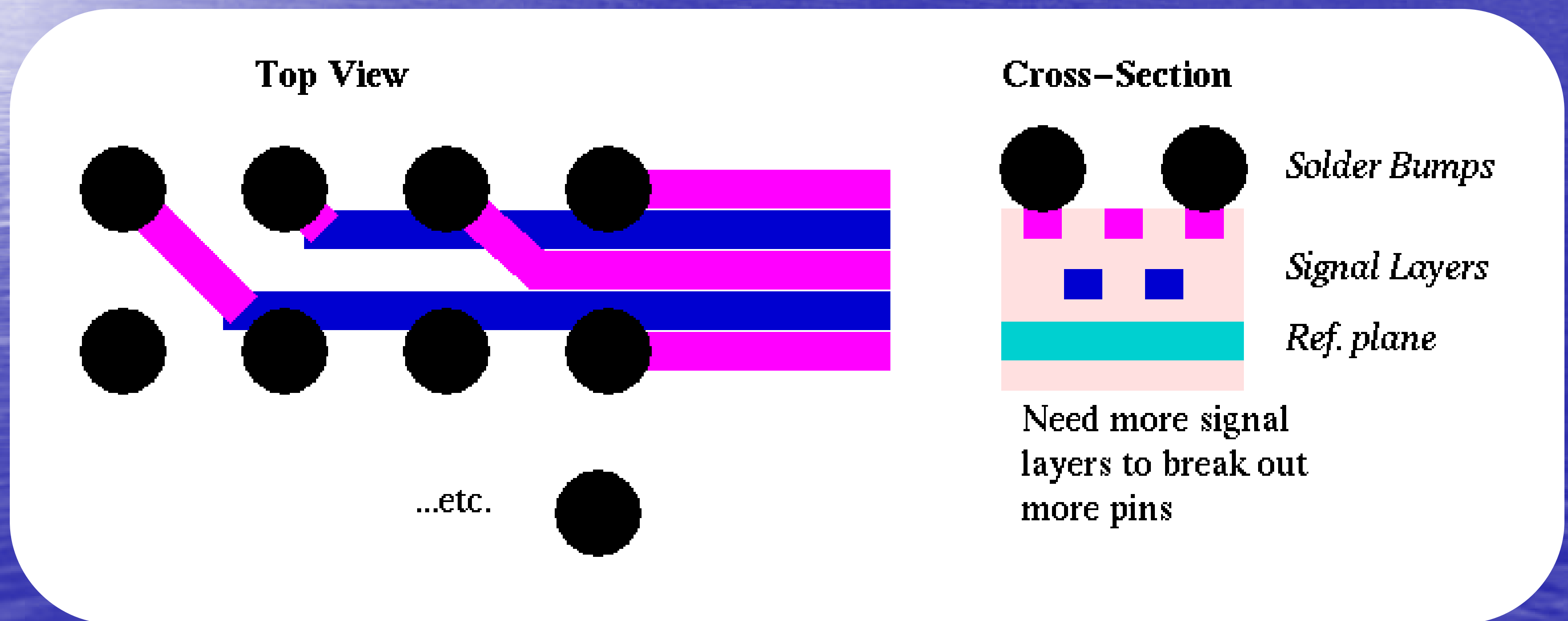
Chip-Package-PCB Co-optimization



Package Escape Routing

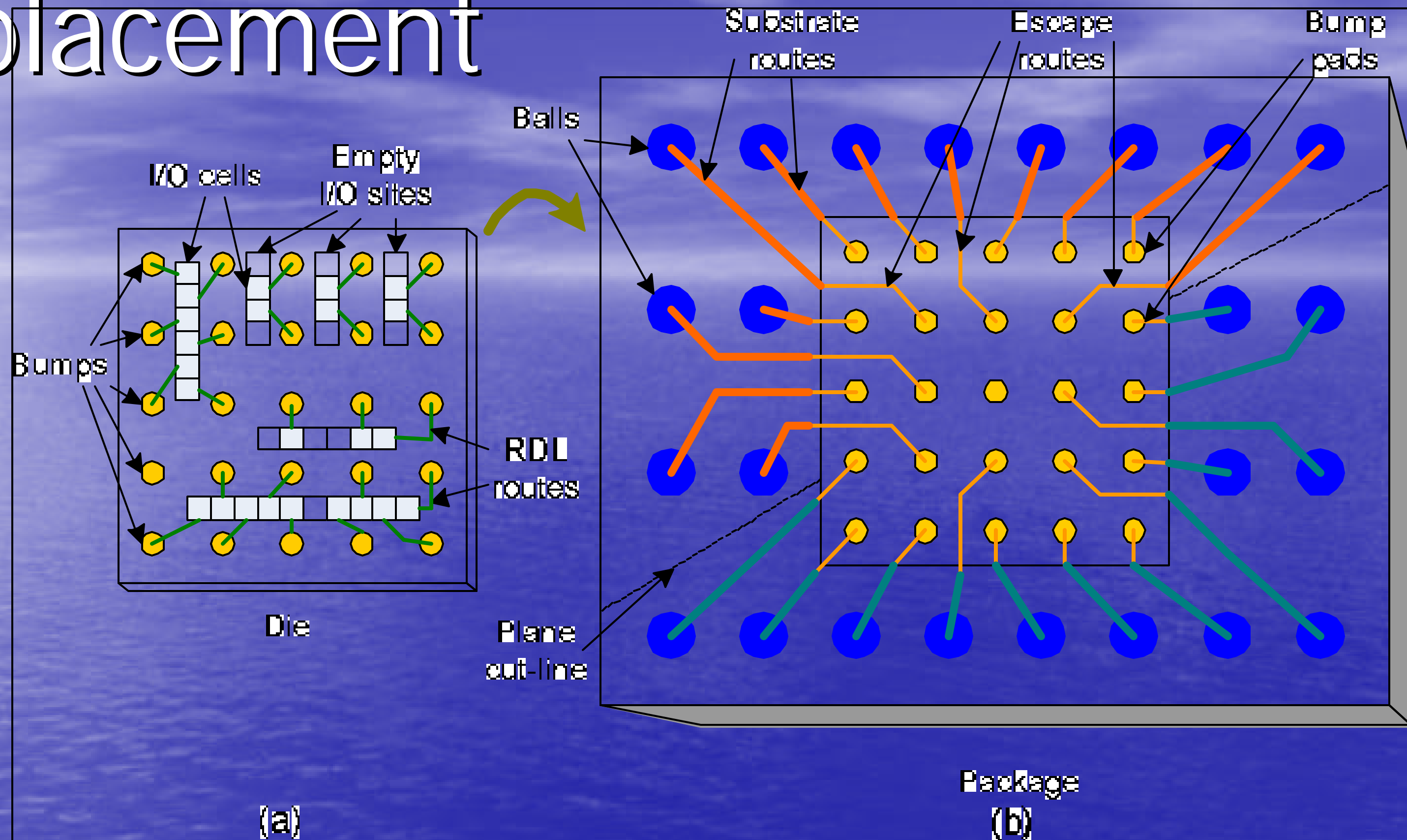
- Escape routing of IO pads imposes chip and package design constraints



IO Ring Planning

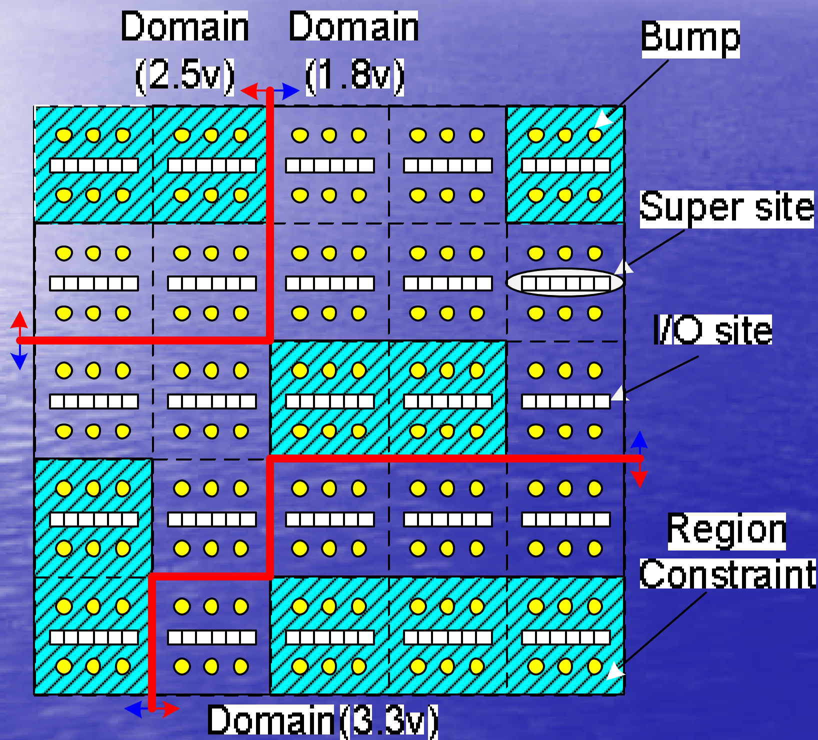
- Flip-chip Design: Area IO vs Peripheral IO
  - Area IO breaks-up most current CAD tools
  - Peripheral IO: cost-effective to transform from wire-bonding to FC
  - Peripheral IO forms a ring
- IO Ring Planning
  - IO locations (placement)
  - Escape routing (escapability analysis)
  - Signal IO vs PG cells/bumps (core power supply)
  - Satisfy SI constraints (SSN)
- Needed early in the design to enable the chip-package co-design
  - System Level Timing Constraints
  - Chip Level Timing Constraints

IO placement



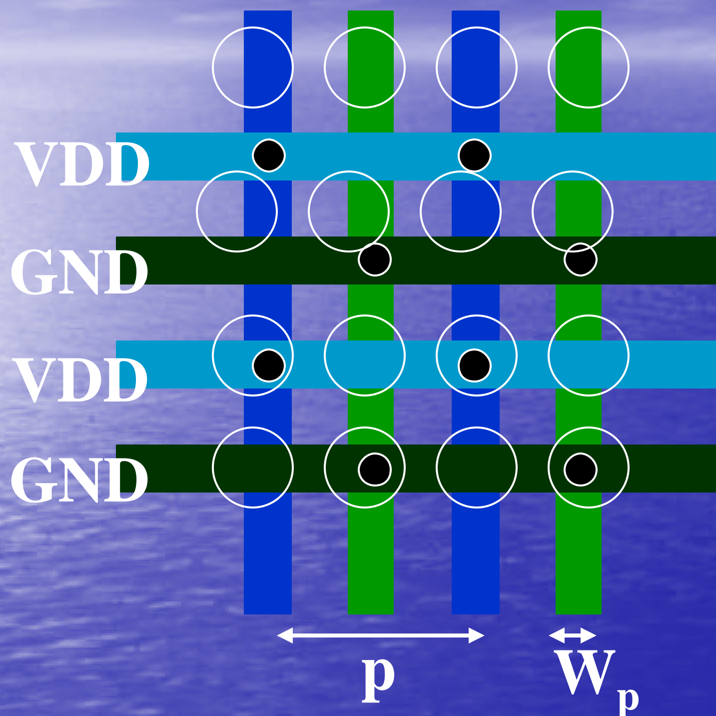
- Placement of bump arrays
- Placement of I/O sites
- Placement of I/O cells

Example of IO placement



- Regular Bump pattern is preferred
- IO sites are decided by proximity
- IO sites are more than IO cells
- Power domains are defined

Core Power Supply Distribution



Voltage drop is given by the equation:

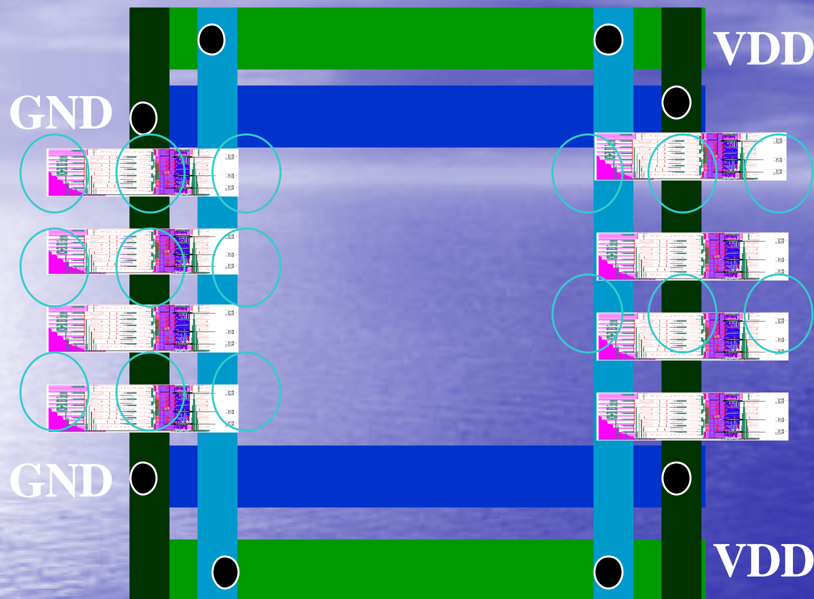
$$IR = J_z r_{m,sh} \frac{p^2}{8}(1 - \frac{W_p^2}{p^2}) \ln(\frac{p}{W_p})$$

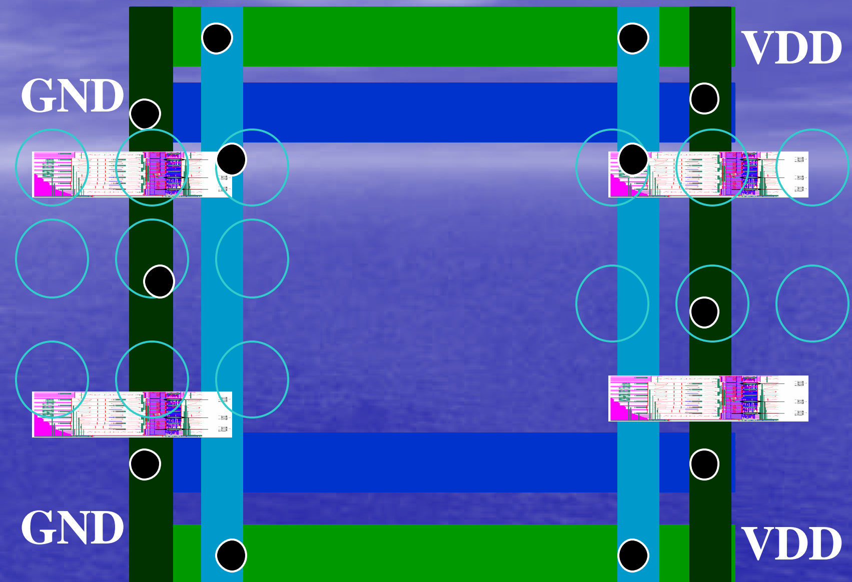
Given the maximum allowed IR drop, it is possible to solve for $r_{m,sh}$, the required metal coverage, iteratively.

However, IR drop constraint should not be a major issue for FC design!

Adapted from:
Power Supply Distribution and Other Wiring Issues for Deep-Submicron ICs
by W.T. Lynch of Semiconductor Research Corporation

IO Power Routing





Wire-bounding IO Power Route

- IO P/G Cells embedded in IO Ring to feed signal IOs
- IO P/G Cells contain ESD cells
- Consumes a lot of space in Ring (constrains pad-limited designs)

Flip-chip IO Power Routes

- No P/G Cells in IO Ring
- Still Need ESD Cells
- P/G bumps cells feed IO Ring
- More Saving on Die Size (especially for pad-limited designs)

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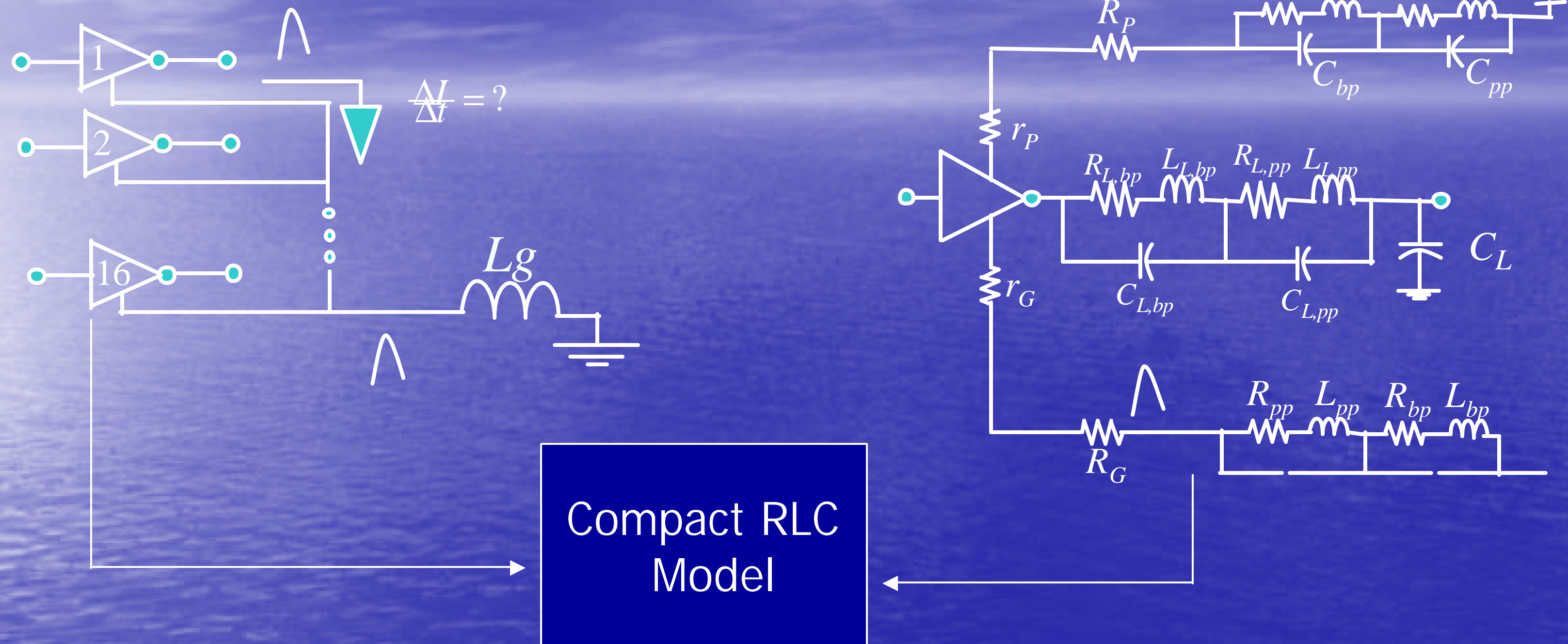
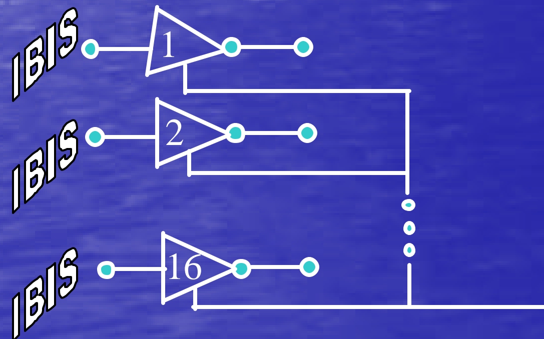
Simultaneous Switching Noise

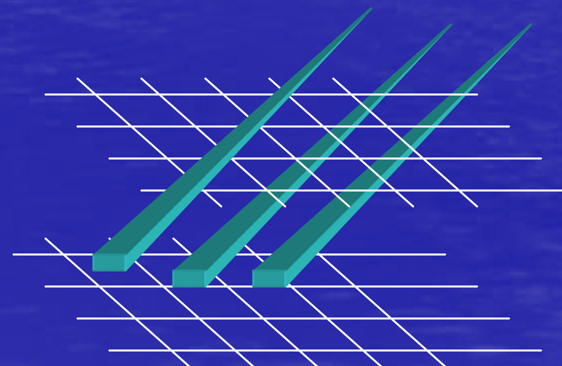


- Package pins, signal traces, and stack-vias exhibit inductive effects
- Power/ground bounce effects limit the performance of design
- Noise effects become more prominent: Ldi/dt
  - Higher clock speed
  - More number of I/O drivers switches simultaneously

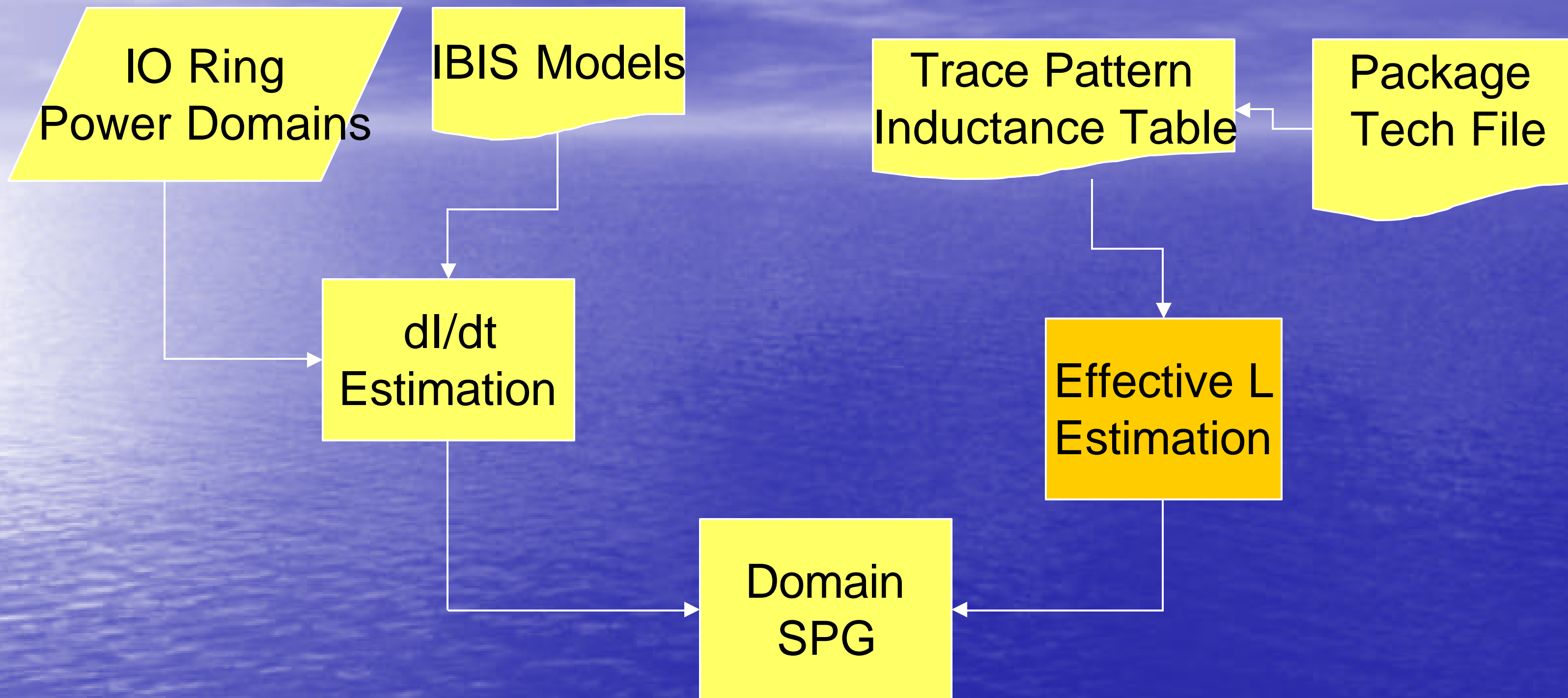
Simultaneous Switching Noise

- SSN Issue Addressed by Signal to PG ratios (SPG) in the IO Ring
  - Accounts for package trace, termination, power and ground
  - Domain by domain: multiple-domain design is not un-usual
- SPG Estimation
  - Accurate and efficient driver model
    - Macro models: (IBIS)
  - Effective inductance modeling for signal traces and package (which yet to be designed)
    - Pre-characterized package templates



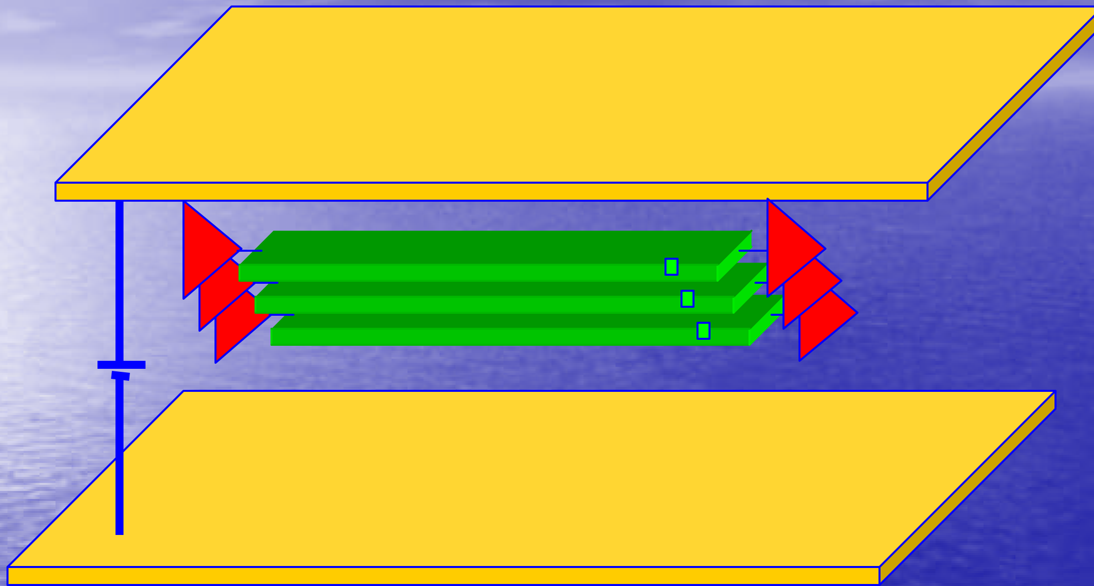


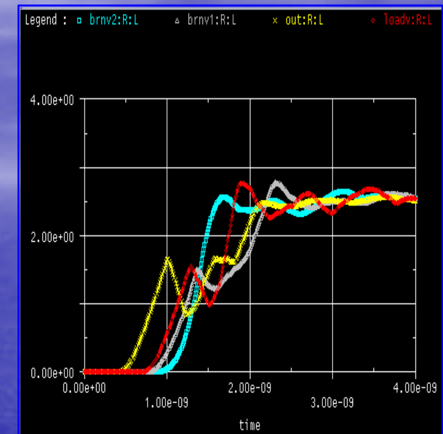
Simultaneous Switching Noise

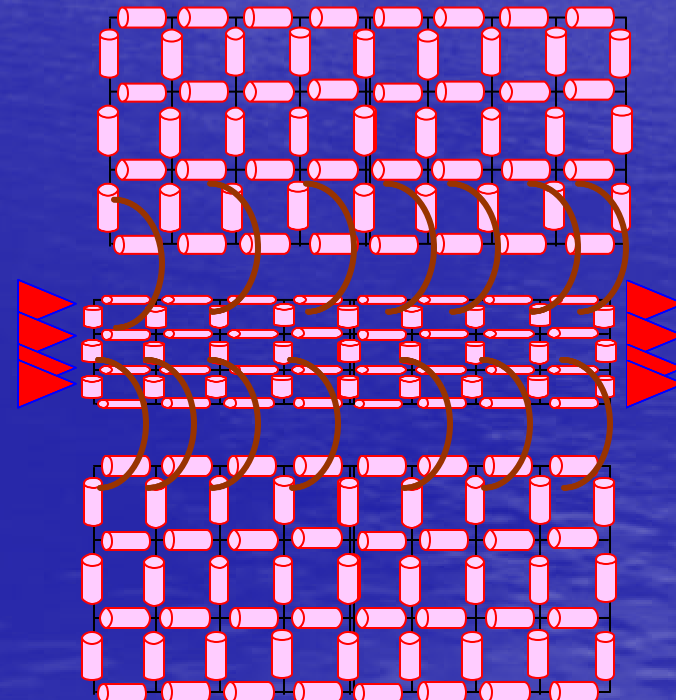


- *dI/dt = f(IV, R_term, VT)*
- Effective L assumed *Common Excitation* for All Ports
- SPG value assumes all drivers switch simultaneously

SSN: Detailed PEEC Modelling







Design: PEEC-based characterized models are employed for SSN estimation

Verification: Detailed PEEC extracted models are employed for SSN analysis

Return Path Modelling

- Needed to model *Ldi/dt* Noise
  - L is defined for a current loop
  - Current distribution depends on routing path and switching pattern
- In early stages, no package routes or power planes exist, and estimated models are developed
  - Rather pessimistic than optimistic
  - Efficient, with reasonable accuracy

Return Path Modelling

- Loop Model: a conservative (pessimistic) model
    - To build a seed IO plan

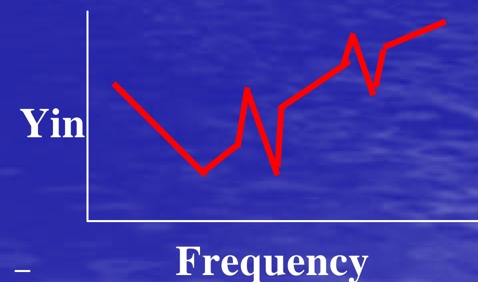
$$
\begin{matrix} L_s & L_{sg} & L_{sp} \\ L_{sg} & L_g & L_{gp} \\ L_{sp} & L_{sg} & L_p \end{matrix}
$$

$$L_{loop} = L_s + L_g - 2L_{sg}$$

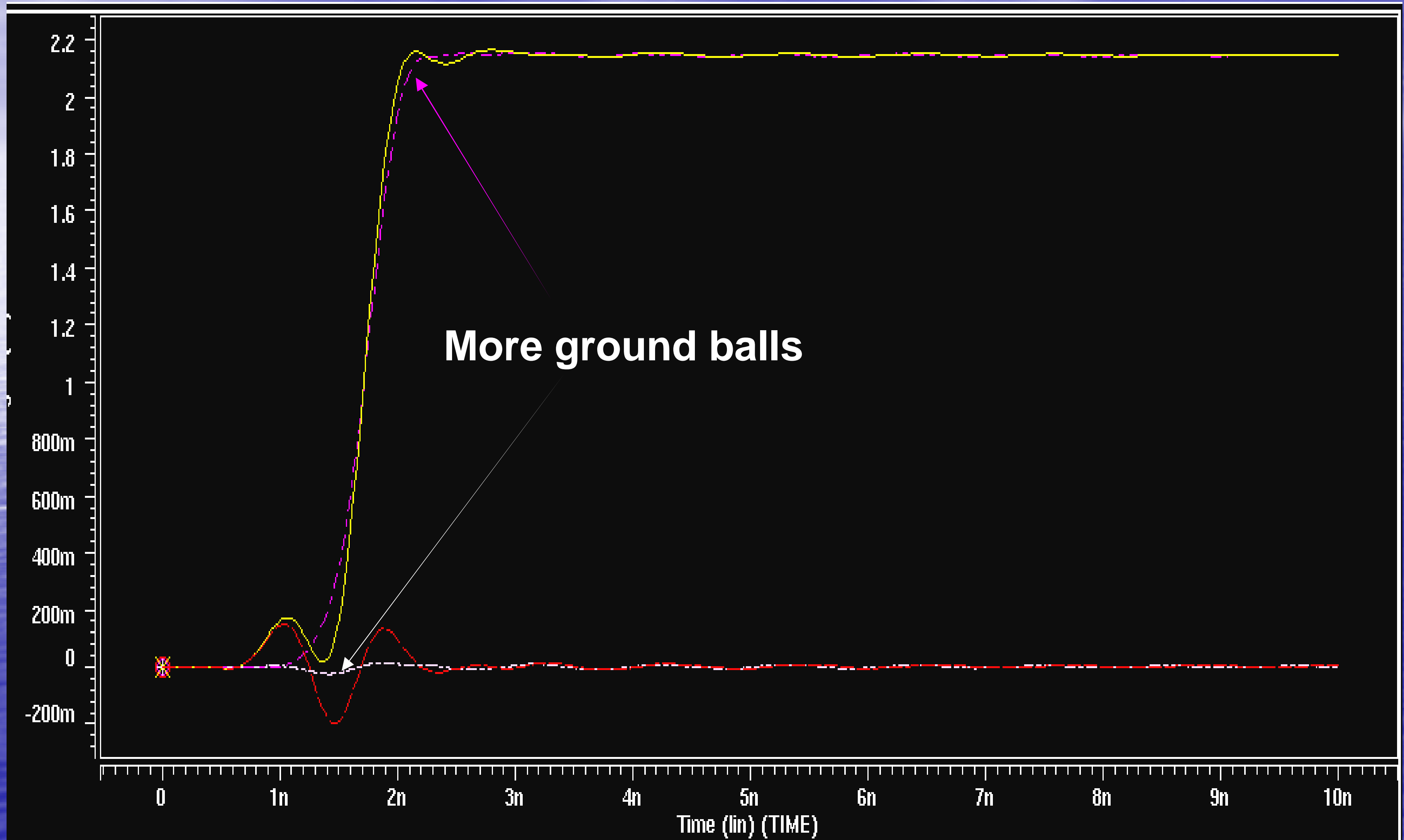
- Effective Inductance Modeling: based on early PEEC models (accurate with computation cost)
    - Based on Impedance/Admittance

$$Leff = \frac{1}{2pf\ \mathrm{Im}(Y_{in})}$$

Two Point Inductance



Simultaneous Switching Noise



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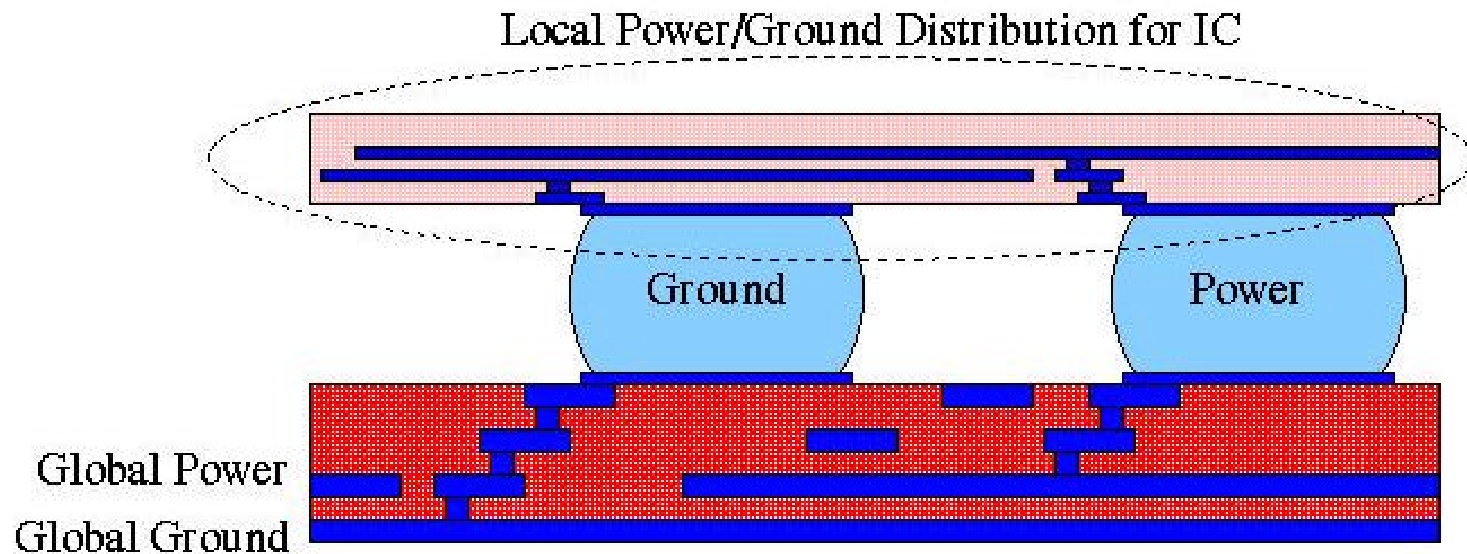
Power Integrity

- Frequency domain analysis of Power Planes Impedance
- Return Path Modelling for EMI and SSN analysis
- EMI Analysis
- Package Plane Resonance

- Time domain Power and Signal integrity
- Signal Noise Analysis coupled with power plane models
- Superposition of Power Noise on Signal Noise
- IBIS, SPICE and PEEC models are employed

PDS: Power Distribution System

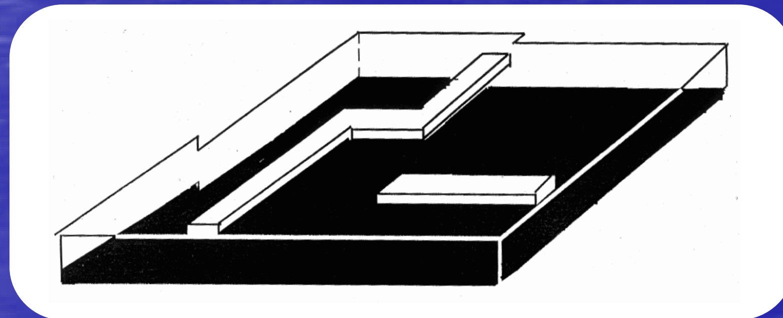


Detailed Network Modeling is needed for accurate analysis of Core and IO Power

Ideal Package Power Planes

Early Package Design Exploration

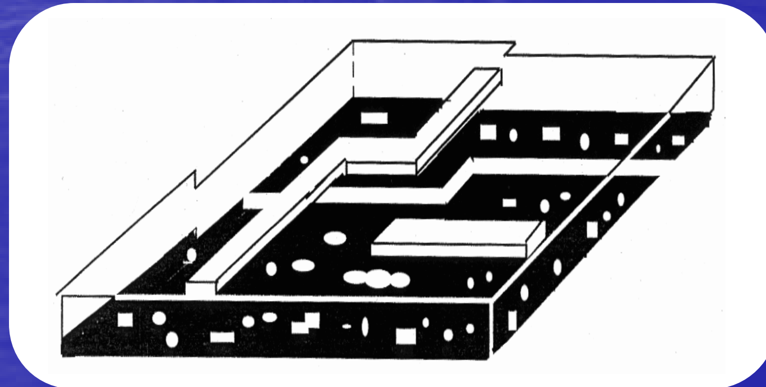
- Planes have no holes or perforations
- Perfect Microstrip or Stripline Patterns
- Impedance is well conditioned



Non-ideal Package Power Planes

Detailed Plane Modeling

- Planes are split for different voltage domains
- Planes could have any number of holes / perforations
- Microstrip or Stripline Patterns: imperfect



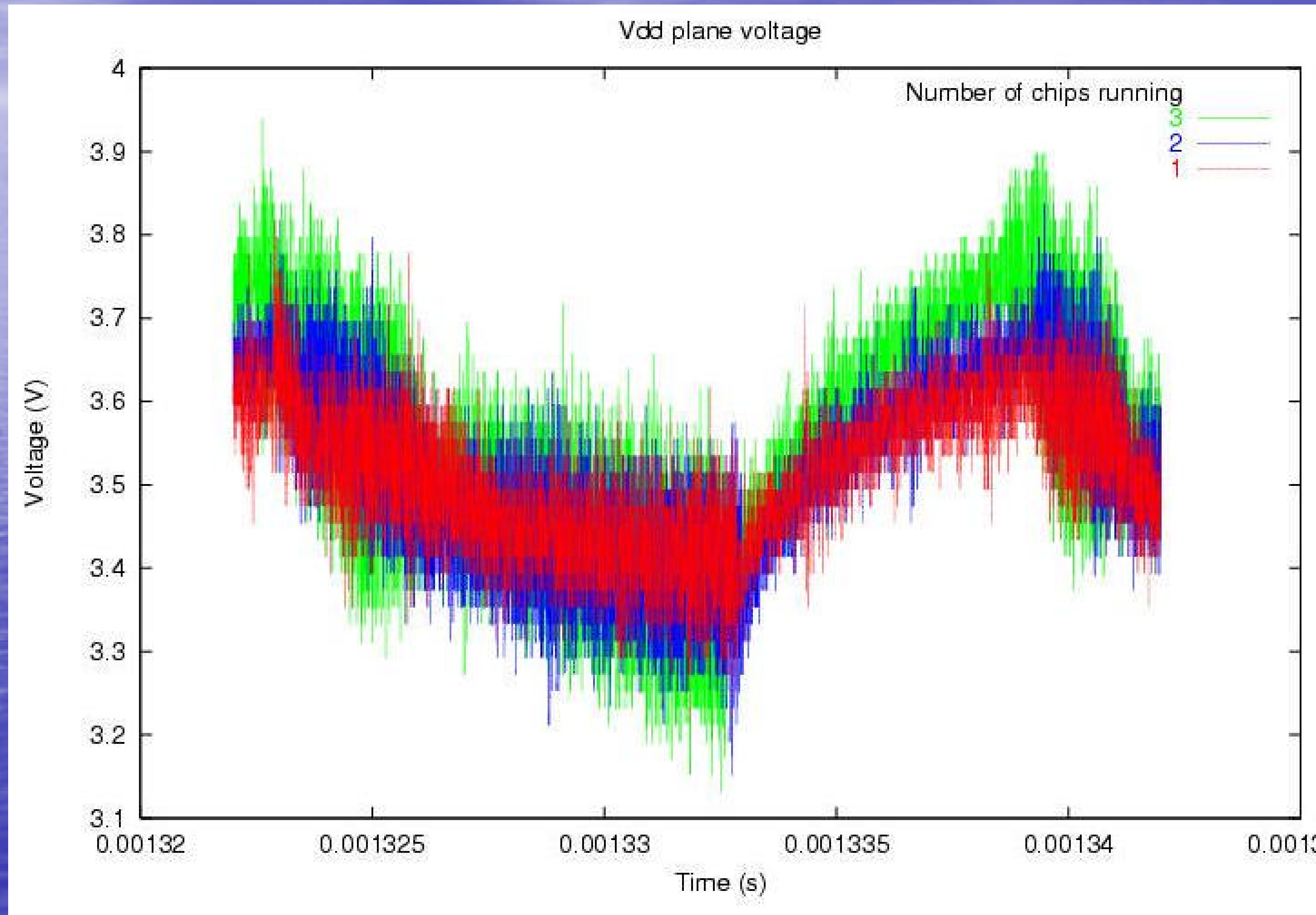
PDS Design

- Assign power planes in package stackup
- Assign power domains: V_{18}, V_{25}, V_{analog},…
- Decide via stapling
  - Improve power delivery
  - Reduce current loop and eliminate noise
- Assign P/G balls

PDS Concerns

- DC Concerns
  - On-Chip IR Drop
    - Not a big concern in Flip-chip Designs
  - In-Package IR Drop
    - Important but still very small
  - In-PCB IR Drop
    - Can be ignored
- AC Concerns
  - Low impedance Network across a broad frequency spectrum
  - Reduce inductive effective to reduce SSN
  - Control Chip/Package resonance

AC-Dominant Power Plane Noise



PDS Design

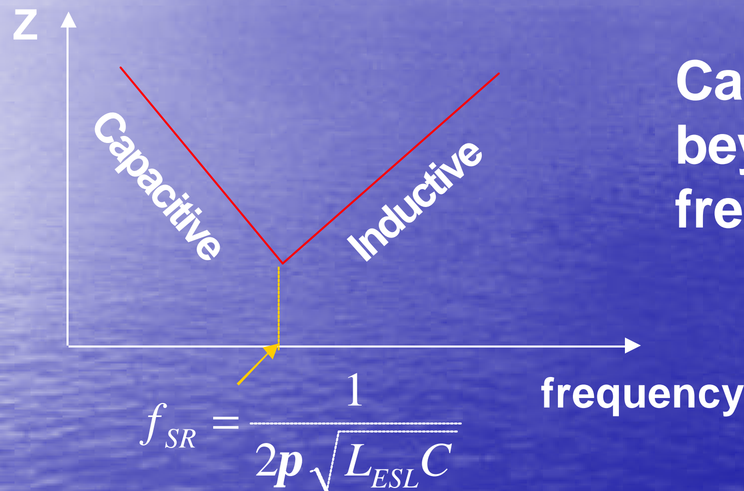
- PDS Impedance
  - Smaller Zo ⇔ larger current

$$Z_o = \frac{0.05 \times V_{dd}}{I_{transient}}$$

- PDS Bandwidth
  - Maintain Zo from 0 to fmax
- Decide on Decap Allocation
  - High speed drivers draw current from nearby decoupling capacitors
  - Decoupling capacitors reduce the size of the current loop

Chip-Package Plane Resonance

Resonances are produced due to inductance and capacitance

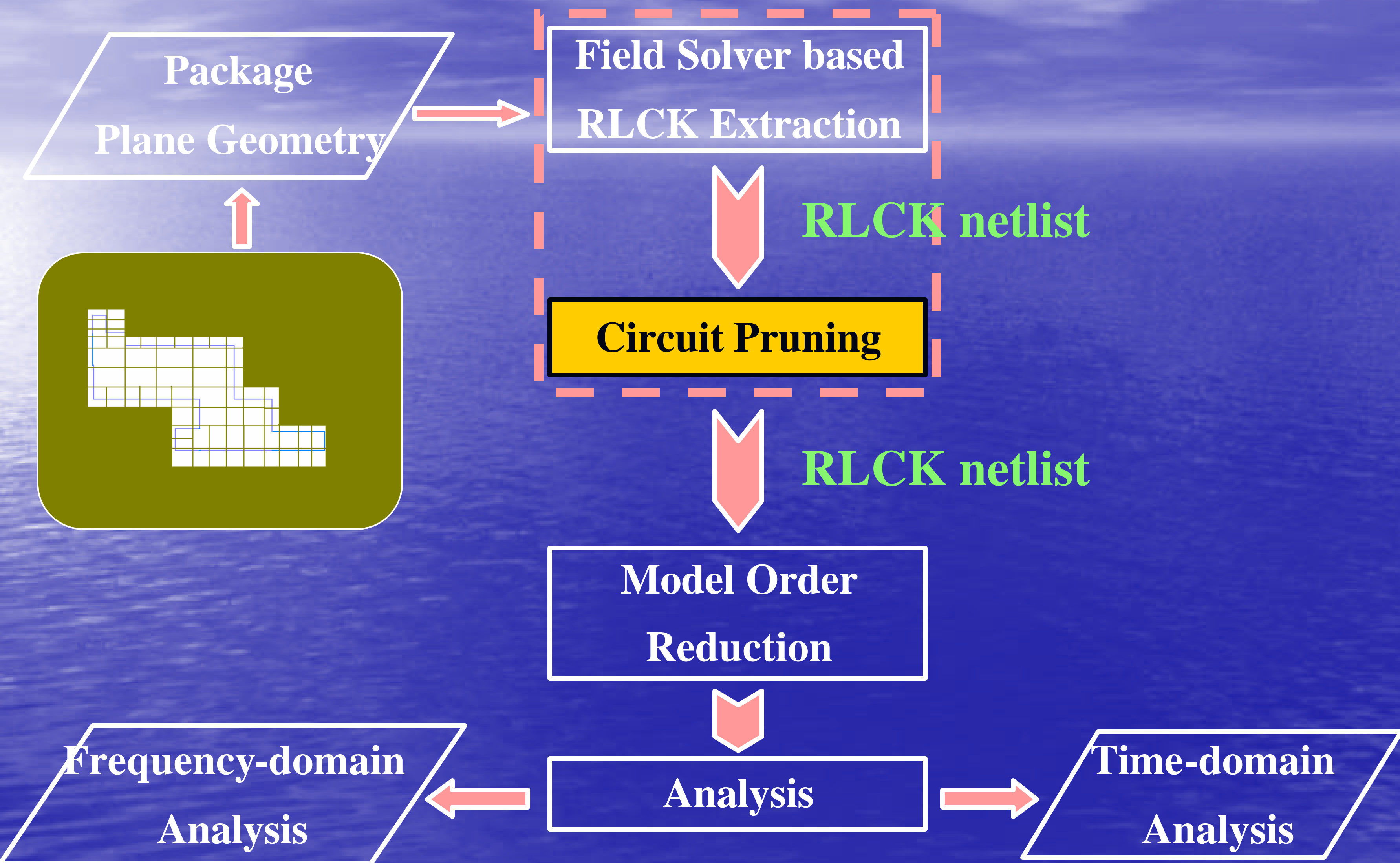


Capacitor becomes inductive beyond its self resonant frequency, *f(SR)*

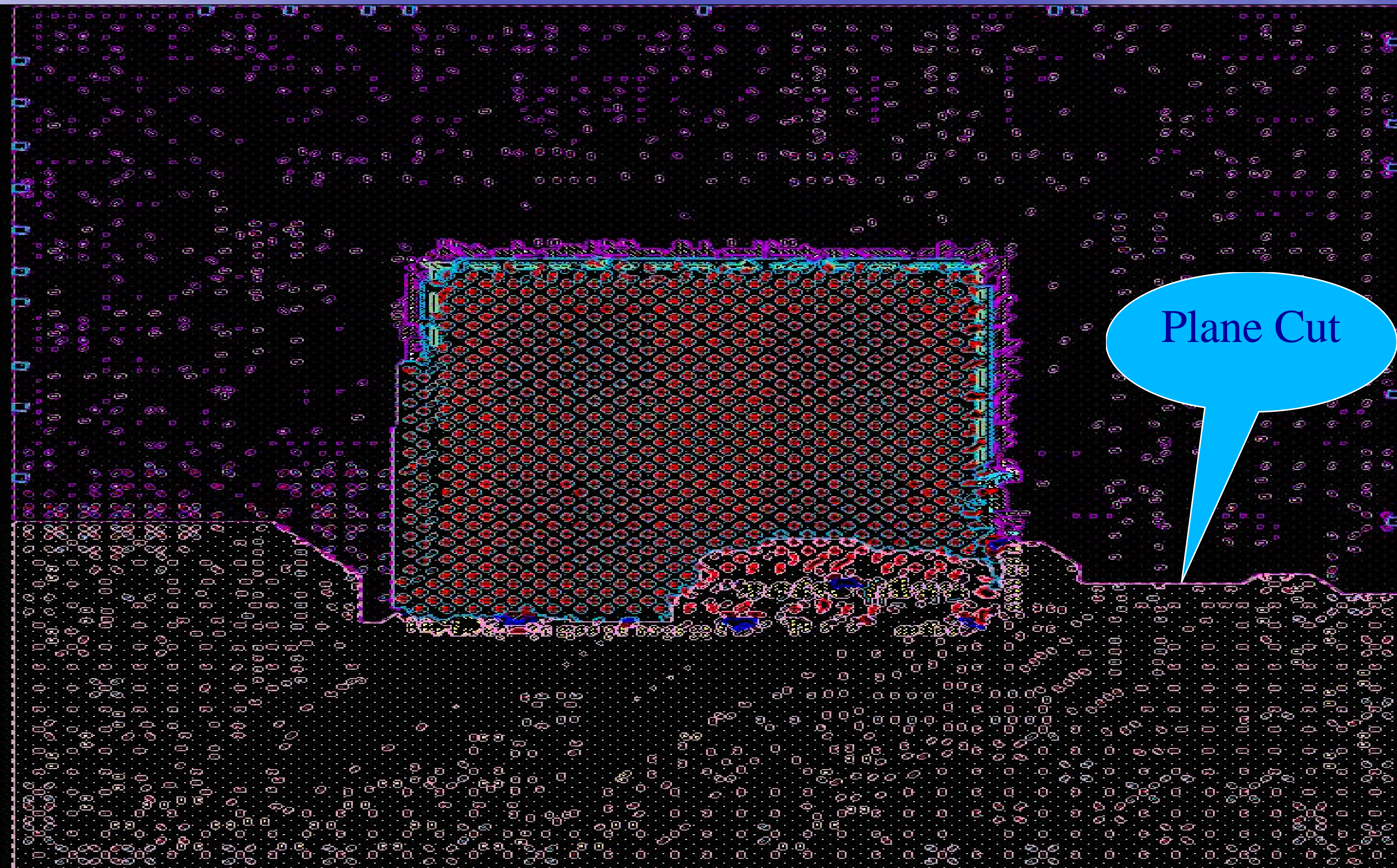
Resonant frequency is $f_{\max} = \frac{1}{2\pi\sqrt{2L_{pkg}C_{pkg}}}$

Need a set of capacitors to cover small, medium, and high frequency ranges

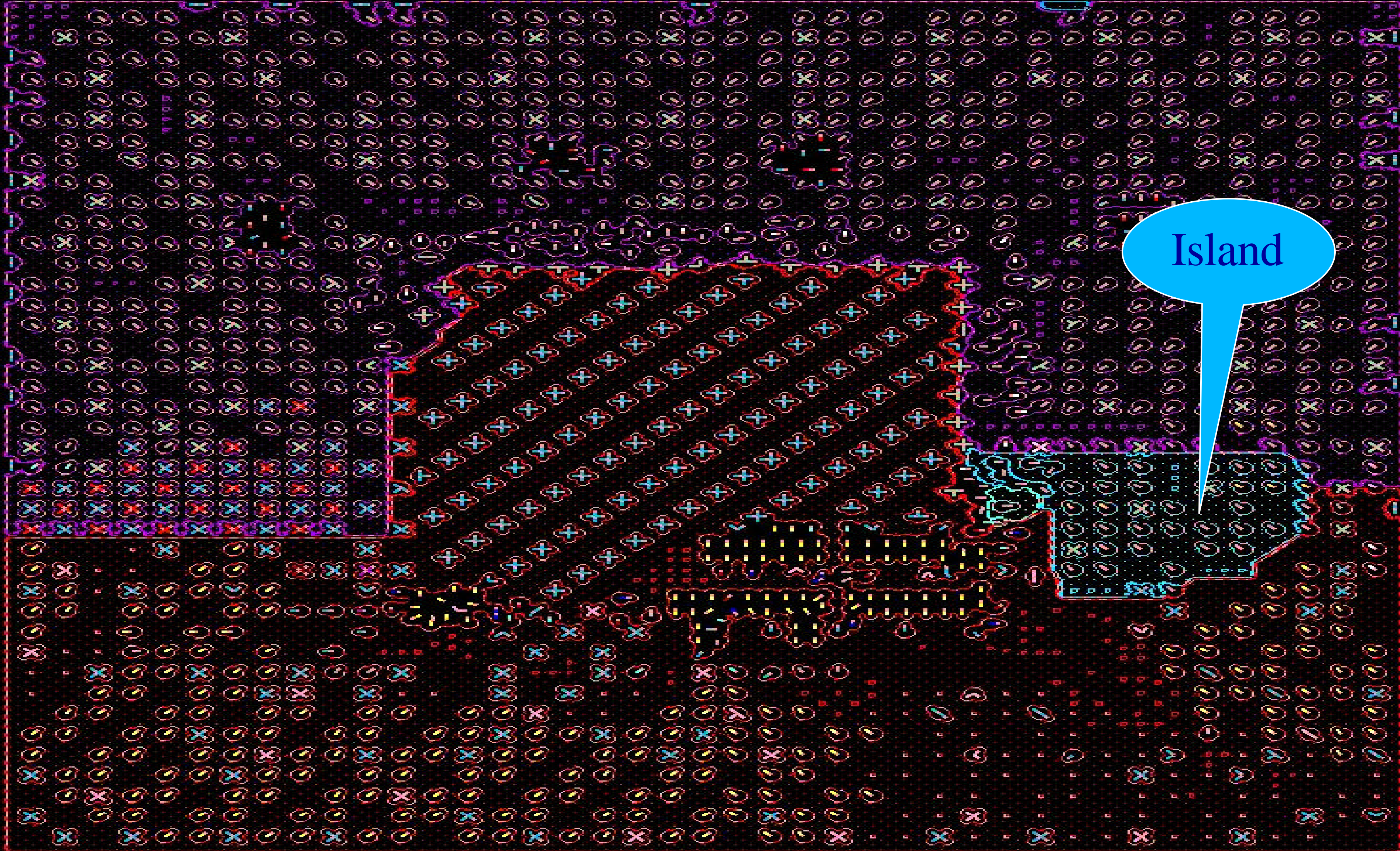
Plane Modeling Design Flow



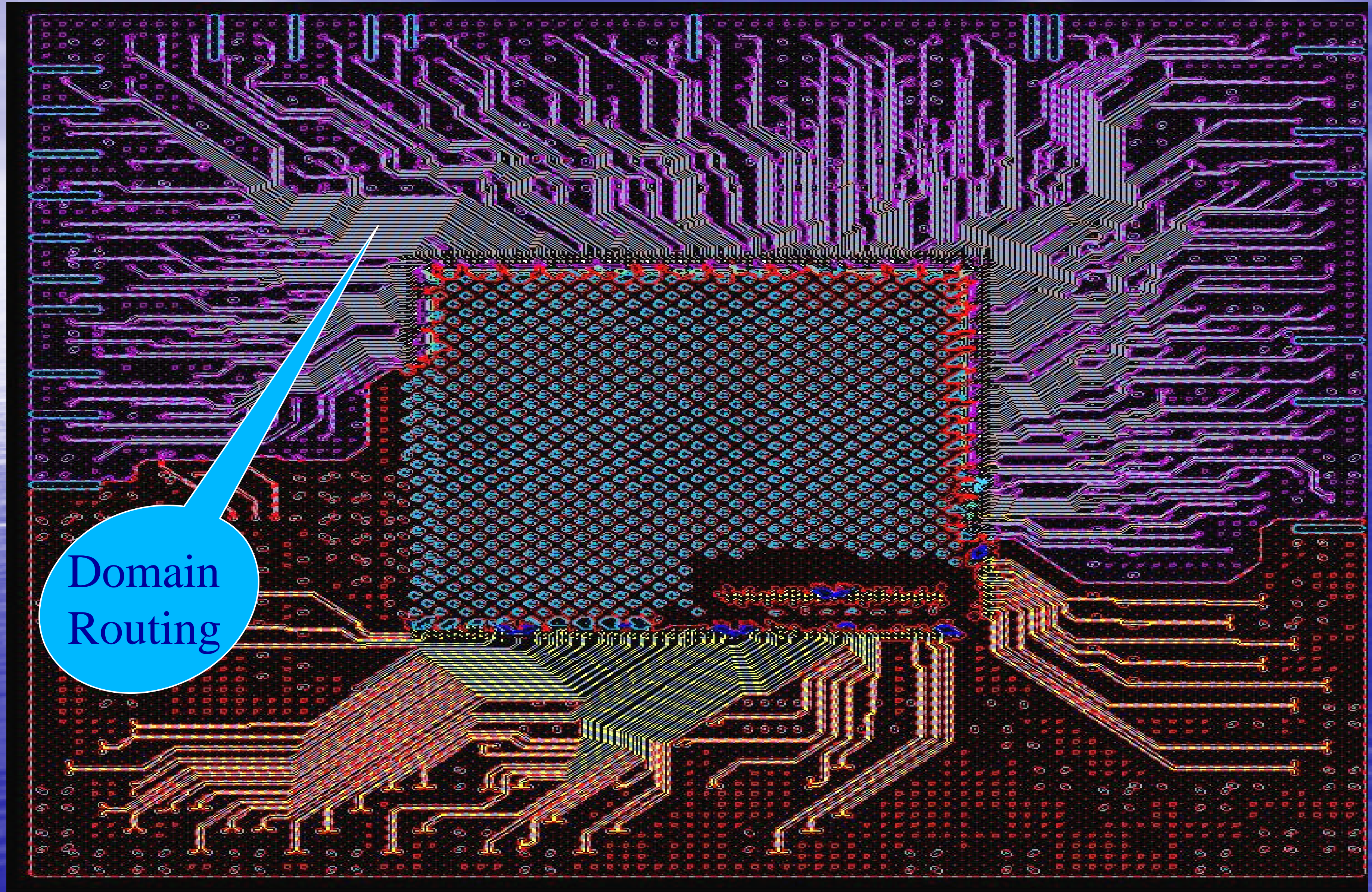
Power Plane Cuts



Power Plane Cuts (Island)



Power Domain Routing



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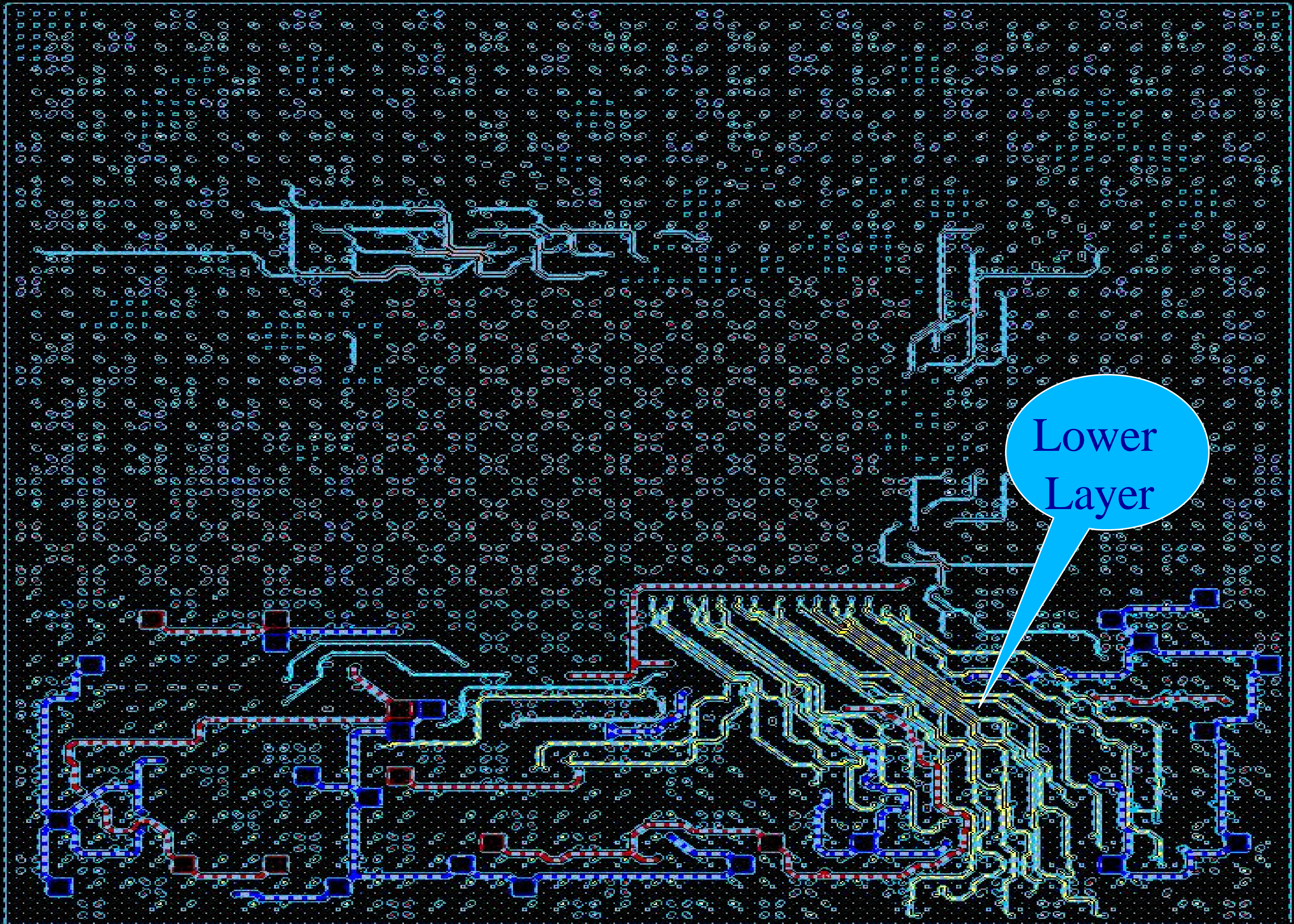
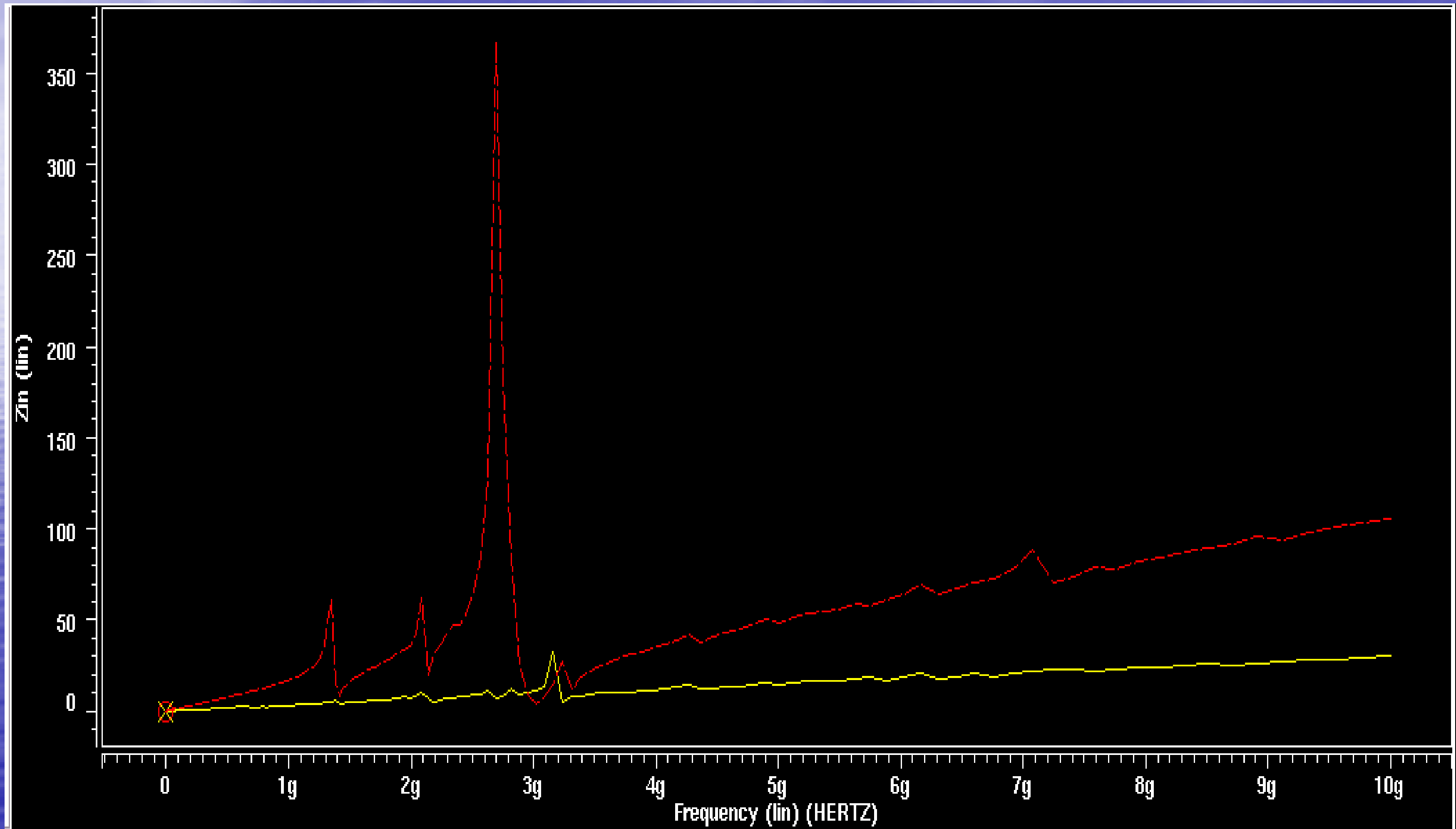


Plane Impedance (impact of de-cap)



Conclusion

- High-speed IO signaling requires package-aware design and analysis (co-design)
- Package-aware chip IO planning improves convergence and turnaround time
- On-chip devices are increasingly exposed to package effects
- Power integrity is getting harder
- Efficient and accurate macro models are needed to enable chip-package co-design