On-Chip Inductance and Coupling Effects

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Outline

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Introduction

On-Chip Inductance effects have become increasingly significant because:

1) For performance considerations, some global signal and clock wires are routed with large widths and thicknesses at the top levels of the metal to minimize delays. This decreases the resistance of the wires, making their inductive impedance comparable to the resistive part.

There is more to impedance than resistance: $Z = R + j\omega L$.
When ωL is comparable to R, inductive effects must be considered.

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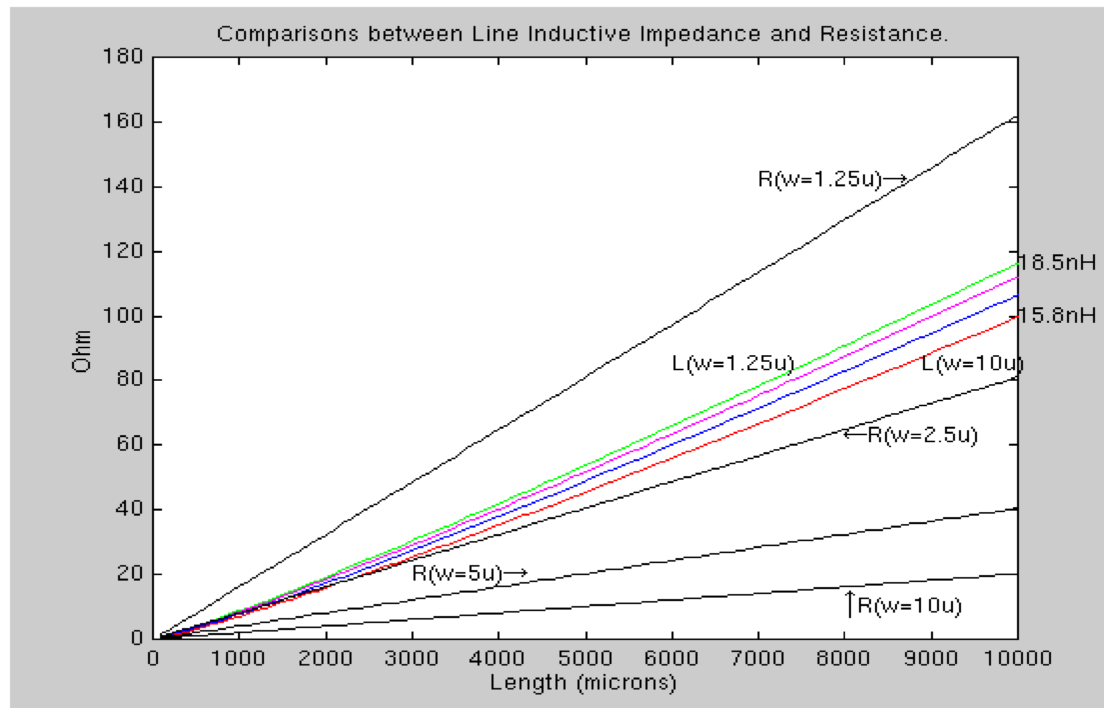
Partial-Self-Inductance Increases Super-linearly:

$$L(nH) = 2l \times \left[\ln\left(\frac{2l}{w+t}\right) + 0.5 - k\right]$$



Resistance and inductive reactance of ***Al*** wires at 1GHz for different lengths and widths.

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Introduction (cont.)

On-Chip Inductance effects have become increasingly significant because:

2) As the clock frequency increases and the rise times decrease, electrical signals comprise more and more high-frequency components, making the inductance effects more significant.

Table 1: SIA Roadmap (1999 Rev.)

Year	Frequency (GHz)
1999	1.25
2002	2.1
2005	3.5
2008	6.0
2011	10.0
2014	13.5

1.71x every 3 years

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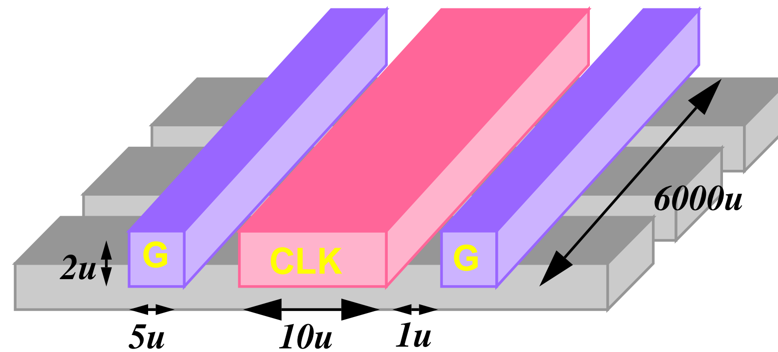
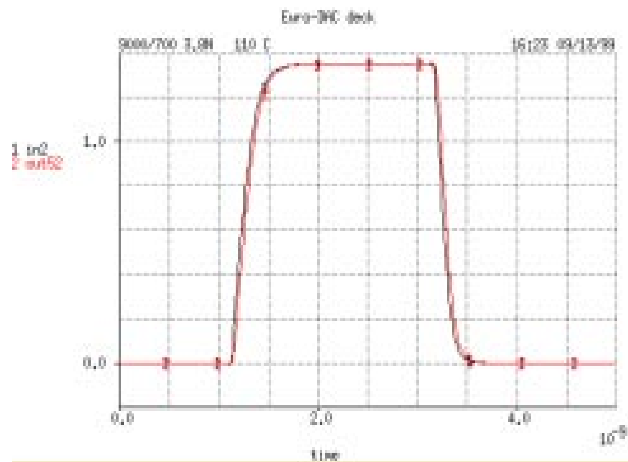
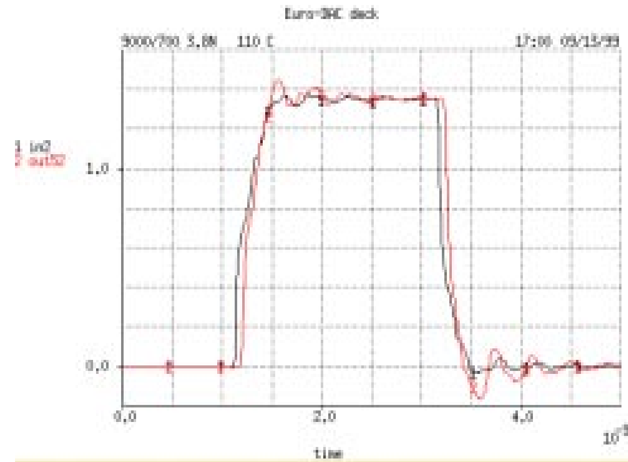
Example of Inductance Effects

(1) over/under-shoot edges, (2) $L\frac{di}{dt}$ voltage drop,

(3) long range crosstalk, and (4) *f*-dependent *R*







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On-Chip Inductance effects have become increasingly significant because:

3) With the increase of chip size, it is fairly typical that many wire are long and run in parallel, which increases the inductive crosstalk and delay.

4) With the push of performance, some low-resistivity metals, e.g. ***Cu*** wires, have been explored to replace ***Al*** in order to minimize wire **RC** delays. This could make the wire inductive reactance larger than the resistance.

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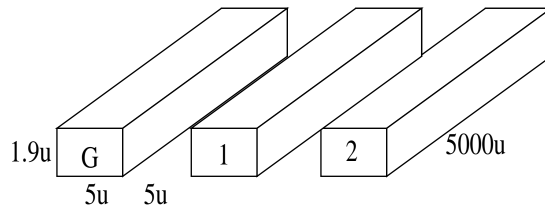
Differences in On-Chip Inductance Consideration

1. The internal inductance of on-chip wires needs to be considered because the skin depths at the frequencies that we consider are comparable to the wire thickness or width. Most electrical currents flow inside the wires.



Inductance is calculated by

$$\tilde{L} = \frac{1}{c^2}\tilde{C}^{-1}$$

in RC2.

Frequency	RI3	RC2	% difference
1 GHz	$\begin{bmatrix} 3.768\times10^{-9} & 2.563\times10^{-9} \\ 2.563\times10^{-9} & 5.125\times10^{-9} \end{bmatrix}$	$\begin{bmatrix} 2.983\times10^{-9} & 2.133\times10^{-9} \\ 2.133\times10^{-9} & 4.266\times10^{-9} \end{bmatrix}$	23%
100 GHz	$\begin{bmatrix} 3.538\times10^{-9} & 2.425\times10^{-9} \\ 2.425\times10^{-9} & 4.850\times10^{-9} \end{bmatrix}$	$\begin{bmatrix} 2.983\times10^{-9} & 2.133\times10^{-9} \\ 2.133\times10^{-9} & 4.266\times10^{-9} \end{bmatrix}$	15%
10,000 GHz	$\begin{bmatrix} 3.203\times10^{-9} & 2.233\times10^{-9} \\ 2.233\times10^{-9} & 4.626\times10^{-9} \end{bmatrix}$	$\begin{bmatrix} 2.983\times10^{-9} & 2.133\times10^{-9} \\ 2.133\times10^{-9} & 4.266\times10^{-9} \end{bmatrix}$	10%

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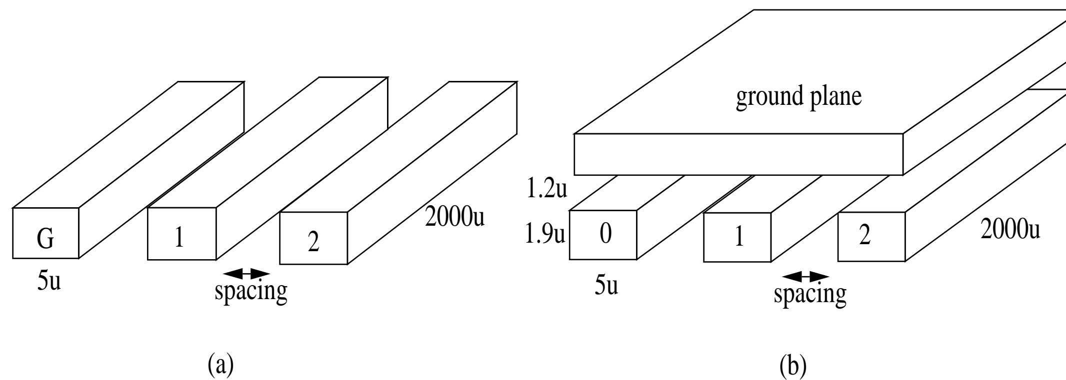
Differences in On-Chip Inductance Consideration

2. Due to the lack of highly conductive ground plane on chip, the mutual couplings between wires cover very long ranges and decrease very slowly with the increase of spacing.



Spacing	K_{12} of (a)	compared with 1um-spacing	K_{12} of (b)	compared with 1um-spacing
1u	0.73	100%	0.29	100%
10u	0.57	78%	0.034	11%
50u	0.54	74%	0.0059	2.0%
100u	0.53	72%	0.0038	1.3%

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Why the silicon substrate cannot be considered as a ground plane?

1. The resistivity of the lightly doped substrate layer is about two million times larger than aluminum.

2. The substrate is too far away from the high-speed buses or clock wires.

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Differences in On-Chip Inductance Consideration

3. The inductance of on-chip wires is not scalable with length.
   (Their self-inductance increases with length at *n log n* rate.)
   Unfortunately, no good approximation formula exists for mutual inductances of two parallel lines of unequal lengths or unequal dimensions.

Mutual inductance for two parallel, same-dimension lines of length l and spacing D is

$$\frac{\mu_o l}{2\pi}\left[\ln\left(\frac{2l}{D}\right) - 1 + \frac{D}{l}\right]$$

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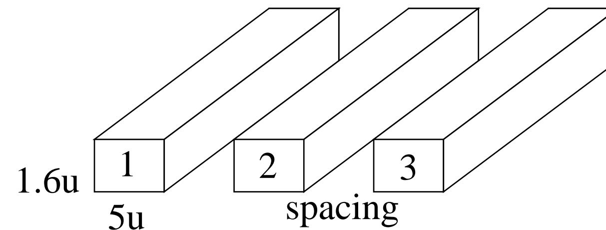
What makes it more difficult to consider inductance than capacitance?

1. Inductance has long range effects. Hence, it is difficult to determine the current return paths.



Spacing	L13 /u	C13 /u
2u	7.94 e-13	7.61 e-17
50u	7.806 e-13	0.98 e-17
100u	4.84 e-13	0.76 e-17

Table 1: Comparisons of L13 and C13

2. Inductance is not scalable.

3. Inductance results in many high frequency poles and zeros, making Reduced Order Model Approximation difficult.

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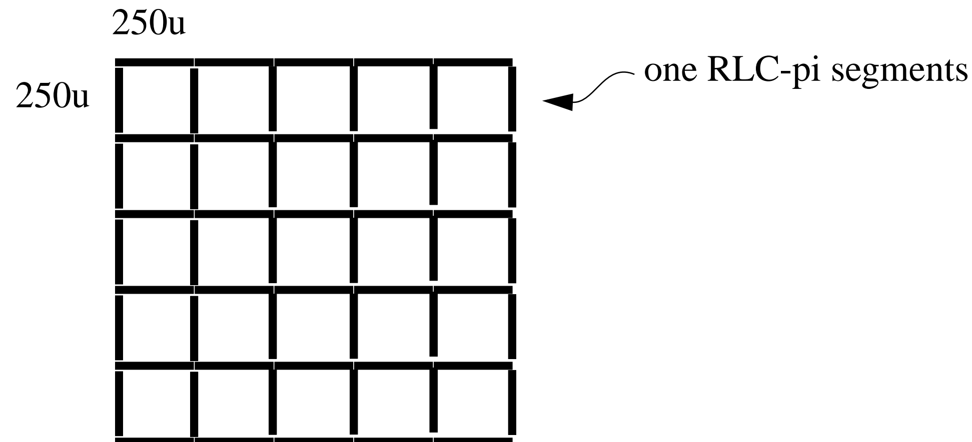
Power Grid Example



The ***L*** matrix after neglecting orthogonal coupling will still be of the dimension 6400, or 80*80, for a typical chip!

Simply discarding small mutual inductance terms can render *L* indefinite and result in an unstable circuit model.

13.7	8.595	5.375	5.34
8.595	13.7	5.34	5.375
5.375	5.34	13.7	8.595
5.34	5.375	8.595	13.7

eigen-values = [5.07, 5.14, 11.58, 33.01]

vs.

13.7	8.595	5.375	0
8.595	13.7	0	5.375
5.375	0	13.7	8.595
0	5.375	8.595	13.7

eigen-values = [16.92, 10.48, 27.67, -0.27]

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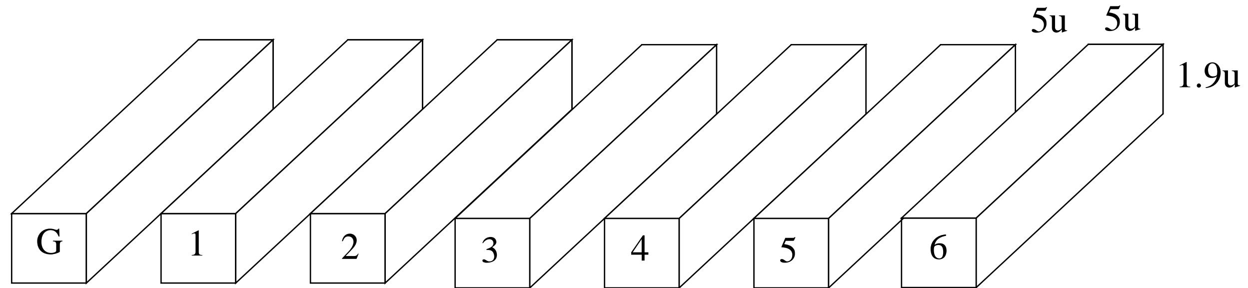
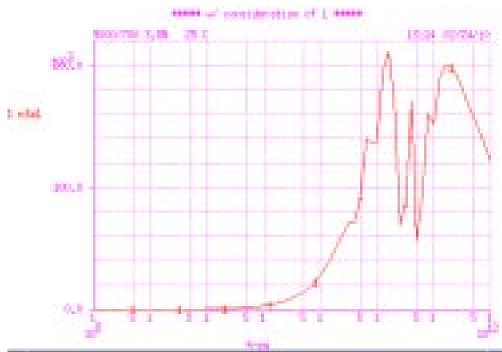
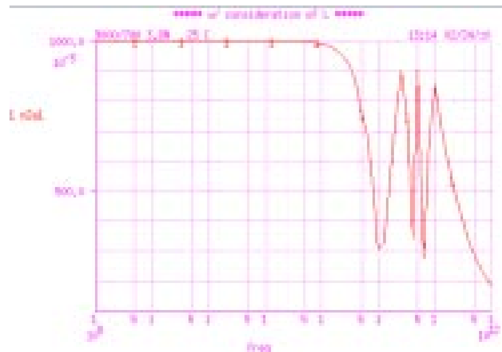
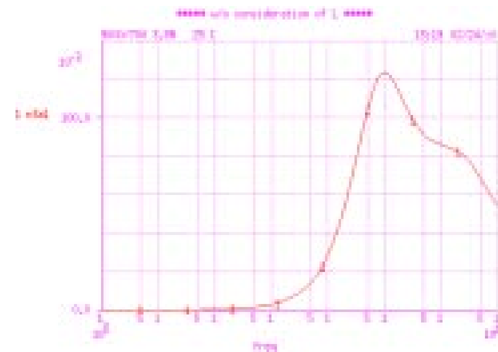


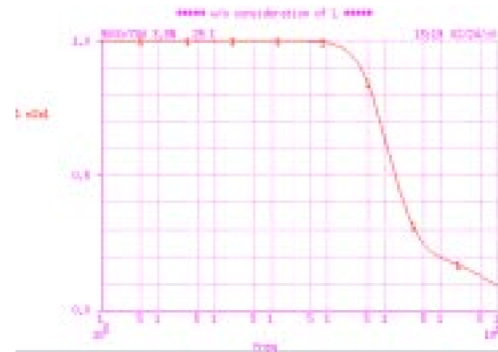
w/ consideration of L

w/o consideration of L









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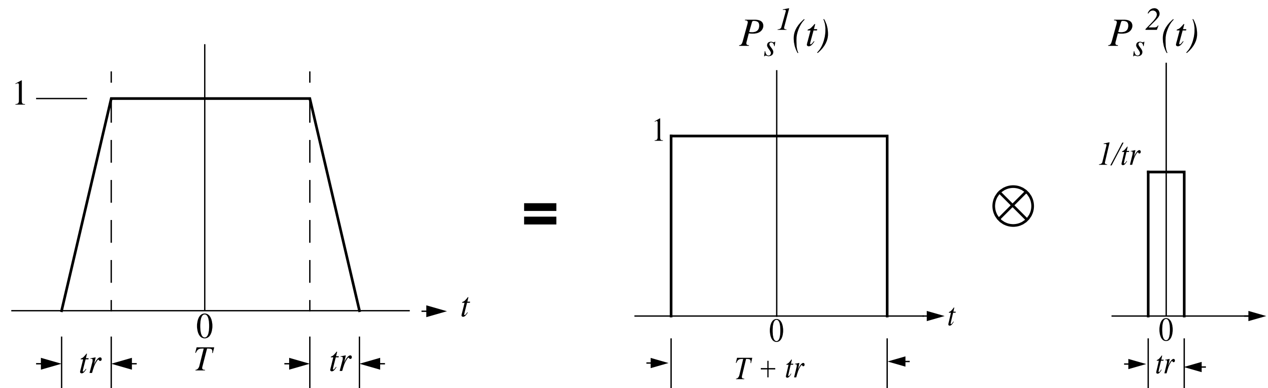
Significant Frequency of High-Speed Pulse



So,

$$P_{tr}(f) = (T + tr) \text{ sinc } f(T + tr) \ \text{ sinc } f(tr)$$

Or,

$$P_{tr}(z) = tr(r + 1) \text{ sinc } z(r + 1) \ \text{ sinc } z$$

where $r \equiv \frac{T}{tr}$, r normally falls in the range of $7 \le r \le 13$

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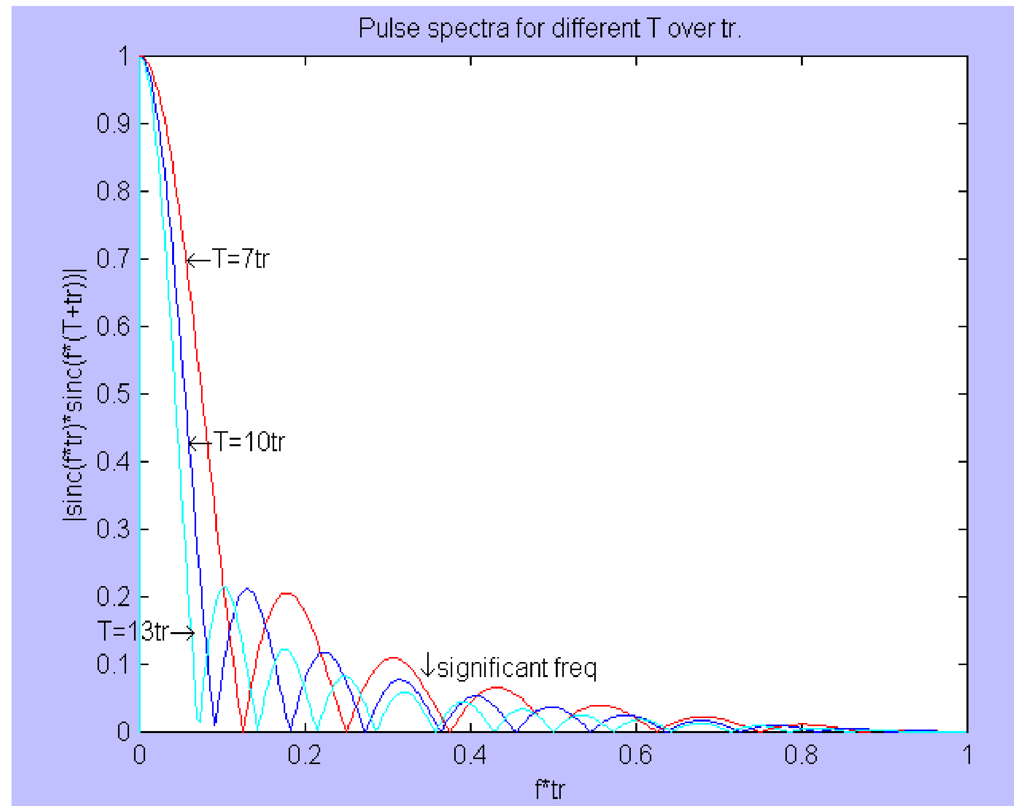
Pulse spectra for different T over tr



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Significant Frequency of High-Speed Pulse

Let

$$S(r) = \frac{\int_0^{0.34} |\operatorname{sinc} z(r+1) \quad \operatorname{sinc} z| \, dz}{\int_0^{\infty} |\operatorname{sinc} z(r+1) \quad \operatorname{sinc} z| \, dz}$$

$S(r)$ is a monotonic function.

$S(7) = 0.85$, $S(10) = 0.858$, $S(13) = 0.862$.

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Significant Frequency of High-Speed Pulse

Significant Frequency is defined as

$$f_s = \frac{0.34}{t_r}$$

Properties:

1. About 15% of the frequency components lie at frequencies higher than the significant frequency.

2. The magnitude of the pulse's spectrum at at frequency higher than the significant frequency is less than 10% of its maximum value. Beyond the significant frequency, the spectral amplitude rolls off much faster than 20 *dB/decade*.

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Inductance Calculation

Maxwell's equations:

$$\nabla\times\boldsymbol{E} = -\frac{\partial\boldsymbol{B}}{\partial t}$$

$$\nabla\times\boldsymbol{H} = \frac{\partial\boldsymbol{D}}{\partial t} + \boldsymbol{J}$$

$$\nabla\bullet\boldsymbol{B} = 0$$

$$\nabla\bullet\boldsymbol{D} = \rho$$

Maxwell's equations in the sinusoidal steady state:

$$\nabla\times\boldsymbol{E} = -j\omega\mu\boldsymbol{B}$$

$$\nabla\times\boldsymbol{H} = j\omega\varepsilon\boldsymbol{D} + \boldsymbol{J}$$

$$\nabla\bullet\boldsymbol{H} = 0$$

$$\nabla\bullet\boldsymbol{E} = \frac{\rho}{\varepsilon}$$

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Inductance Calculation (cont.)

Since $\nabla \bullet \boldsymbol{H} = 0$, $\boldsymbol{H}$ much be the curl of another vector.
Hence we introduce the vector potential $\boldsymbol{A}$, such that

$$\mu \boldsymbol{H} = \nabla \times \boldsymbol{A} \quad \text{and} \quad \nabla \bullet \boldsymbol{A} = 0.$$

With magneto-quasi-static assumption,

$$\mu \boldsymbol{J} = \mu \nabla \times \boldsymbol{H} = \nabla \times \nabla \times \boldsymbol{A} = \nabla(\nabla \bullet \boldsymbol{A}) - \nabla^2 \boldsymbol{A}$$

Therefore,

$$-\nabla^2 \boldsymbol{A} = \mu \boldsymbol{J}$$

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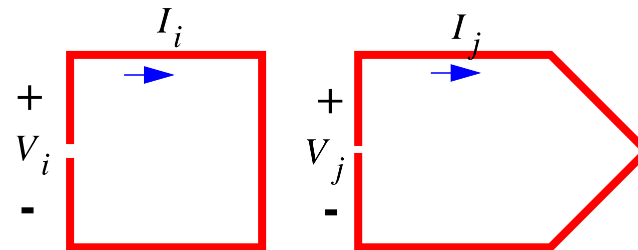
Inductance Calculation (cont.)

Green's function solution for the Poisson's equations:

$$\boldsymbol{A}(r) = \frac{\mu}{4\pi}\int_{V'}\frac{\boldsymbol{J}(r')}{|r-r'|}dv'$$



$$\boldsymbol{A}_{\boldsymbol{ij}} = \frac{\mu}{4\pi}\frac{I_j}{a_j}\oint_j\int_{a_j}\frac{d\boldsymbol{l}_j\, da_j}{r_{ij}} \qquad \psi_{ij} = \frac{1}{a_i}\oint_{\boldsymbol{i}}\int_{a_i}\boldsymbol{A}_{\boldsymbol{ij}} \bullet d\boldsymbol{l}_{\boldsymbol{i}}\, da_i$$

$$L_{ij} = \psi_{ij}/I_j = \frac{1}{a_i a_j}\frac{\mu}{4\pi}\oint_i\int_{a_i}\oint_j\int_{a_j}\frac{d\boldsymbol{l}_{\boldsymbol{i}} \bullet d\boldsymbol{l}_{\boldsymbol{j}}}{r_{ij}}\, da_i da_j$$

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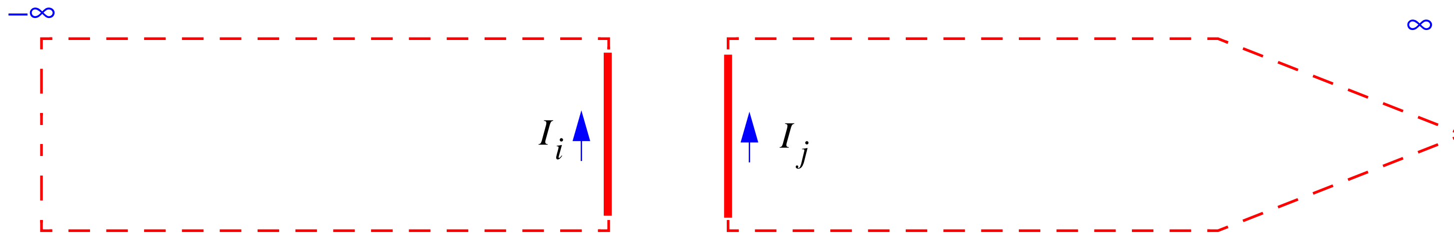
Partial Inductance

Partial Inductance (PEEC model) is the portion of loop inductance for a wire segment when its current returns via the infinity.



$$A_{ij} = \frac{\mu}{4\pi} \frac{I_j}{a_j} \int_j \int_{a_j} \frac{d\boldsymbol{l}_j \, da_j}{r_{ij}}$$

$$L_{ij} = \frac{1}{a_i a_j} \frac{\mu}{4\pi} \int_i \int_{a_i} \int_j \int_{a_j} \frac{d\boldsymbol{l}_i \bullet d\boldsymbol{l}_j}{r_{ij}} \, da_i da_j$$

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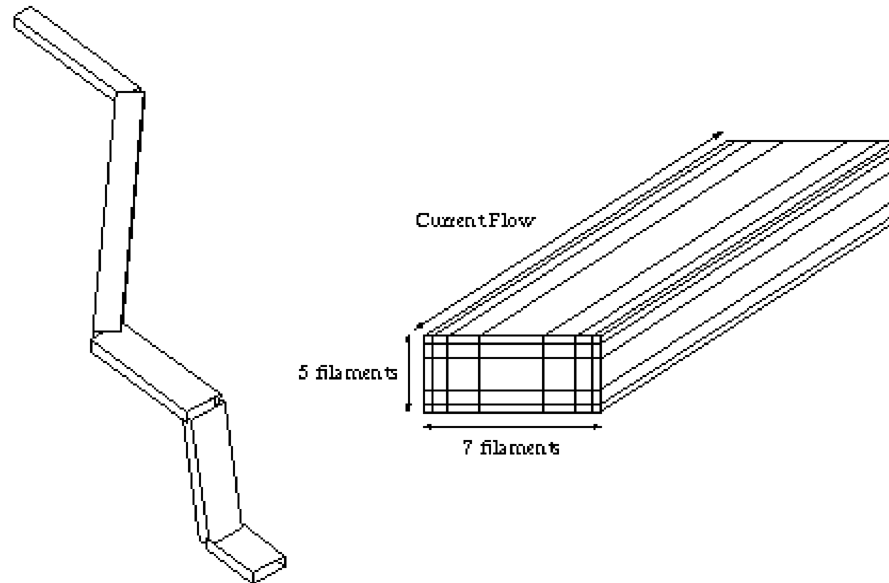
Partial Inductance Calculation

Partial Inductance calculation of an interconnect divided into multiple segments, each of which is a bundle of multiple filaments:



$$L_{ij} = \sum_{k=1}^{K} \sum_{m=1}^{M} \frac{\mu}{4\pi} \frac{1}{a_k a_m} \int_{b_k}^{c_k} \int_{a_k} \int_{b_m}^{c_m} \int_{a_m} \frac{dl_k \bullet dl_m}{r_{km}} \, da_k da_m$$

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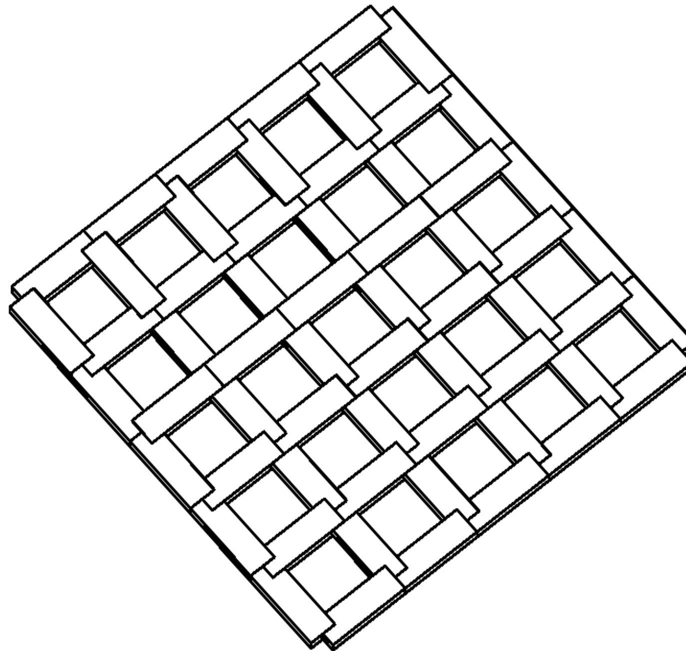
Partial Inductance Calculation (cont.)

Discretization of a ground plane



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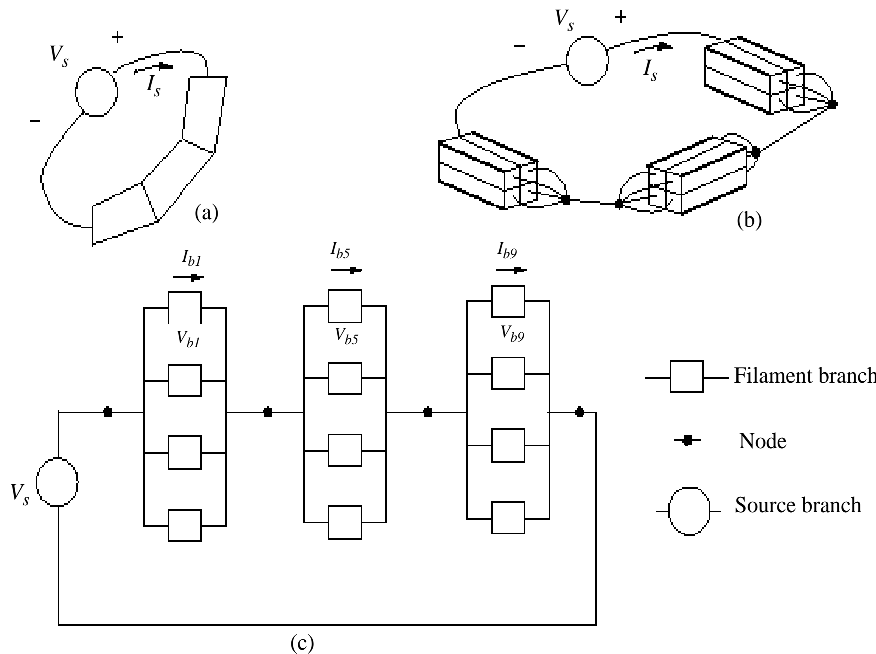
Partial Inductance Calculation (cont.)

$$V_i = \left(\frac{l_i}{\sigma a_i}\right) I_i + j\omega \sum_{j=1}^{b} \left(\frac{\mu}{4\pi} \int_i \int_{a_i} \int_j \int_{a_j} \frac{dl_i \bullet dl_j}{r_{ij}} da_i da_j \right) I_j$$



$$(\boldsymbol{R} + j\omega \boldsymbol{L}) \boldsymbol{I}_b = \boldsymbol{V}_b$$

$$\boldsymbol{A} (\boldsymbol{R} + j\omega \boldsymbol{L})^{-1} \boldsymbol{A}^t V_s = \boldsymbol{I}_s$$

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Properties of Partial Inductance

1. Partial self- and mutual- inductances are based on geometry only.
2. They may be solved by using a 2D/3D field solver such as Avanti's *Raphael* or MIT's *FastHenry*.
3. The return path or the current loop may be determined through SPICE simulations.
4. The partial self- and mutual- inductances *may be* frequency- and proximity- dependent.

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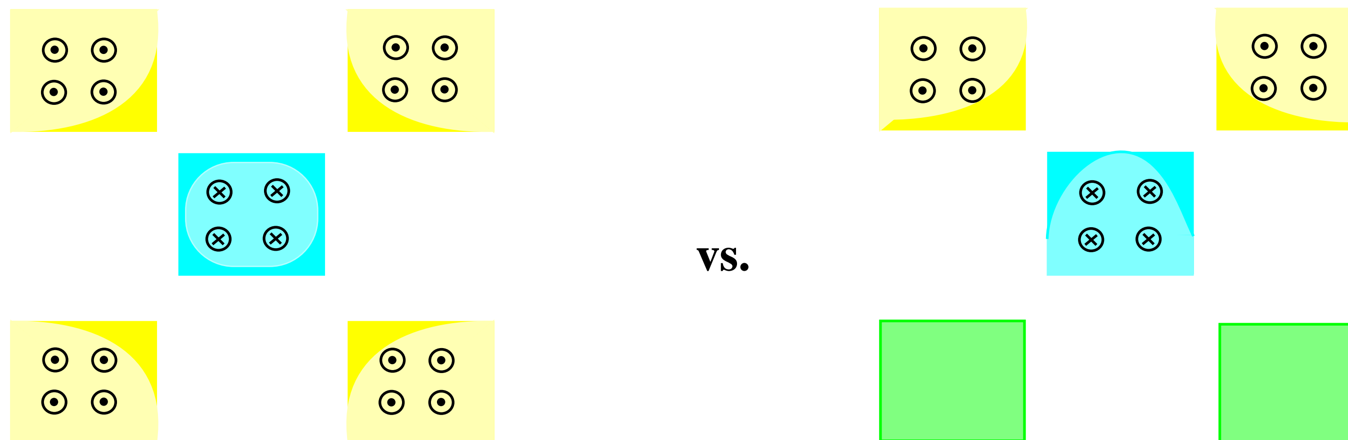
Proximity Effects

Depending on how the current flows among wires (**flow directions** and **current distributions**) at different **frequencies**, the current densities are different. This changes each wire's impedance, including resistance and inductance, at different frequencies.



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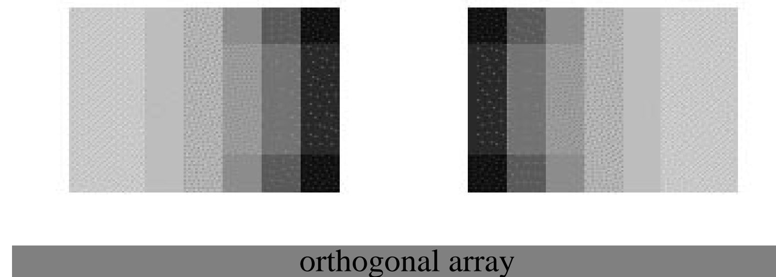
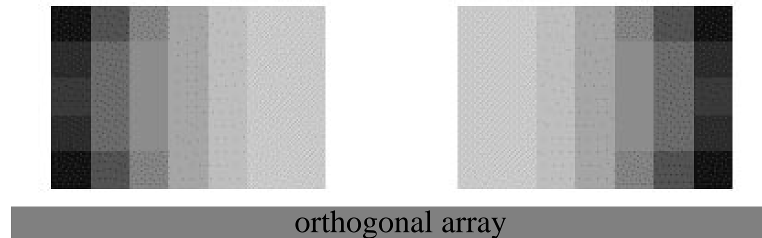
Proximity Effects (cont.)



Current density plot for odd-mode two-coupled conductors on top of an orthogonal array with width 2.5um, thickness 1.9um, spacing 1.2um, distance to orthogonal array 1.2um, and 2000um in length. The current density is higher (5%) at the near end of two-coupled conductors at 4GHz due to the current flowing in the opposite direction.



Current density plot for even-mode two-coupled conductors on top of an orthogonal array with width 2.5um, thickness 1.9um, spacing 1.2um, distance to orthogonal array 1.2um, and 2000um in length. The current density is higher (4%) at the far end of two-coupled conductors at 4GHz due to the current flowing in-phase.

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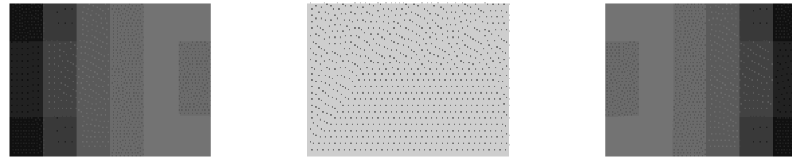
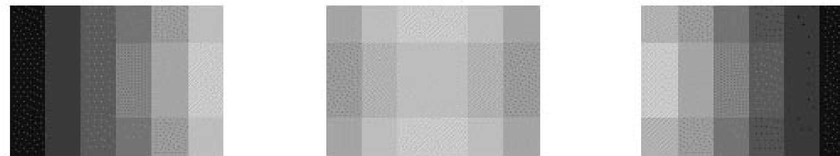
Proximity Effects (cont.)



Current density plot for three-coupled conductors on top of an orthogonal array with width 2.5um, thickness 1.9um, spacing 1.2um, distance to the ground plane 1.2um, and 2000um in length. The currents flow in the same phase in the three conductors. The current density of the center conductor is quite uniform due to the conflicting forces of the skin-effect pushing the current outward from the center and the proximity-effect given by the two outer conductors pushing the current inside toward the center. The maximum difference in current density is about 4% at 4GHz in this case.



Current density plot for three-coupled conductors on top of an orthogonal array with width 2.5um, thickness 1.9um, spacing 1.2um, distance to the orthogonal array 1.2um, and 2000um in length. The currents flow in the same phase in the outer two conductors but in the opposite phase in the center conductor. Interestingly, the current density can be differed by more than 7% in this case at 4GHz.

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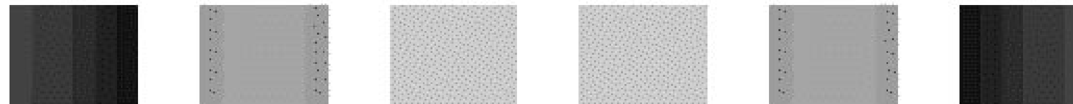
Proximity Effects (cont.)

Current density plot for six-coupled conductors on top of an orthogonal array with width 2.5um, thickness 1.9um, spacing 1.2um, distance to the ground plane 1.2um, and 2000um in length. The same-phase ac voltage is applied in all the conductors. The maximum difference in the current density is 8% in this case at 4GHz.



Current density plot for six-coupled conductors on top of an orthogonal array with width 2.5um, thickness 1.9um, spacing 1.2um, distance to the ground plane 1.2um, and 2000um in length. The same ac voltage is applied in the center four conductors while the outer two conductors grounded. This plot shows the current density of the conductors. The maximum difference in the current density is about 34% in these six conductors.

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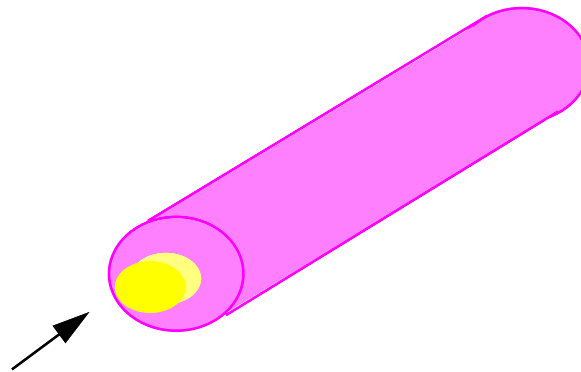
Skin Effects

Skin effect is the exponential increase of current concentration near the conductor surface as the frequency, the conductivity, and the permeability of the conductor are increased.

$$E_z = E_0 e^{-x/\delta} e^{-jx/\delta}$$

$$J_z = J_0 e^{-x/\delta} e^{-jx/\delta}$$



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Skin Depth

The skin depth is the depth of penetration into the conductor at which the magnitudes of the field and the current decrease to 1/*e* (about 36.9%).

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

permeability (μ), conductivity (σ)

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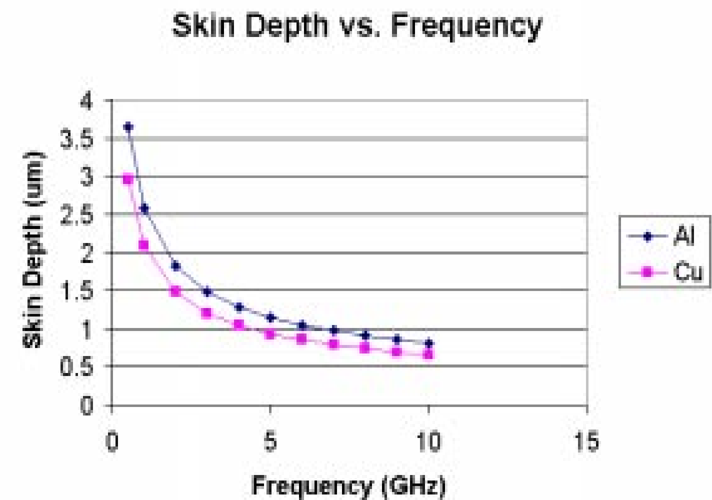
Skin Effects (cont.)

Skin Depth versus Frequency for Aluminum and Copper Interconnects

Frequency (GHz)	δ for Al (micrometer)	δ for Cu (micrometer)
0.5	3.651	2.955
1	2.581	2.089
2	1.825	1.478
3	1.490	1.206
4	1.291	1.045
5	1.154	0.934
6	1.054	0.853
7	0.976	0.790
8	0.913	0.739
9	0.860	0.697
10	0.816	0.661



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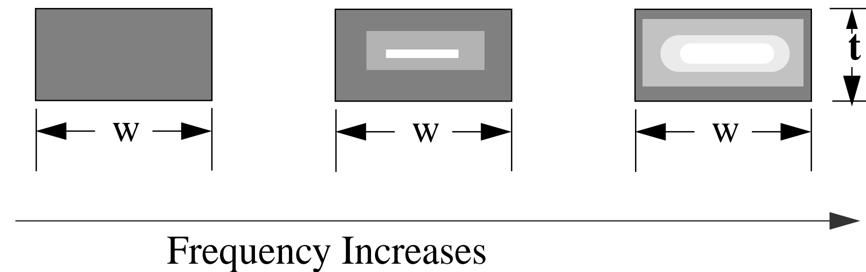
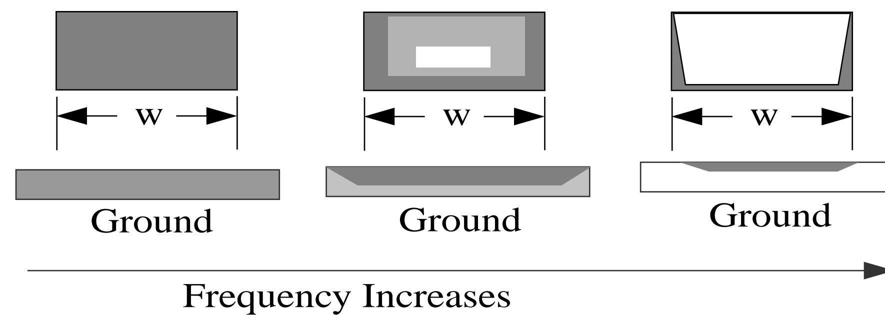
Skin Effects (cont.)

Current distribution versus frequency in an isolated conductor:



Current distribution versus frequency in a conductor over a ground plane:



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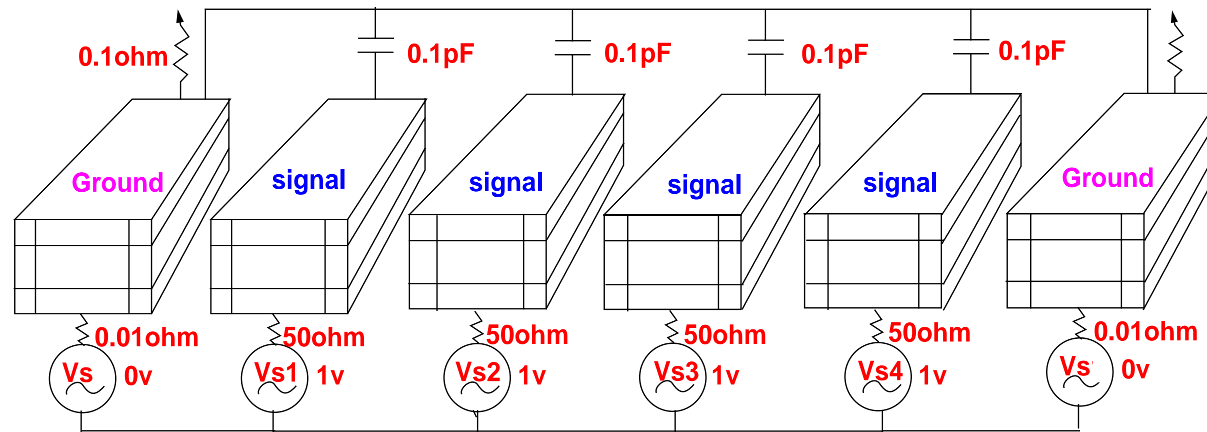
Cope with Proximity and Skin Effects using PEEC

By using fine filament approximations of wires. So, it is a trade-off between CPU time spent on SPICE simulations and accuracy.



Multiple single bar composition of each rectangular conductor in Raphael RI3 is used to model the skin-effect and proximity-effect induced current density on the six conductor case, for example. Current value is monitored during SPICE simulation of the formulated RLC deck of this six conductor case. All the other examples such as two conductors or three conductors are modeled and simulated in a similar fashion. In this case, the current density is monitored at the far end of the conductors.

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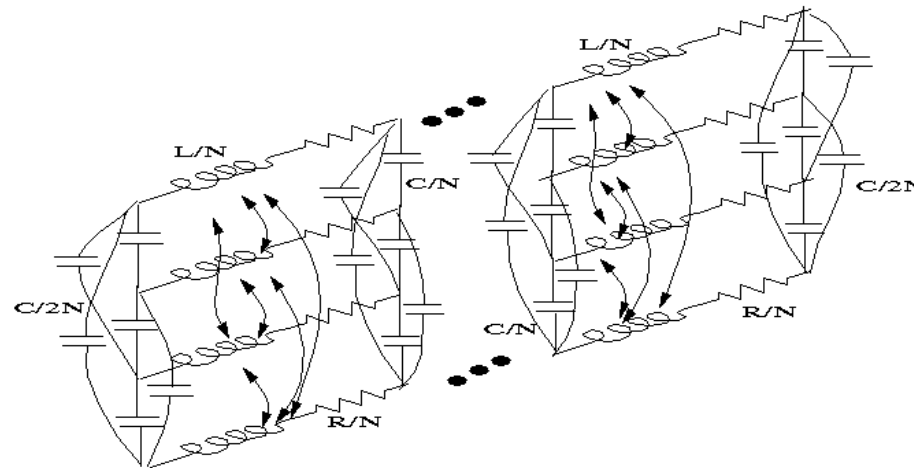
Circuit Modeling

1. Run Raphael RI3 to get the inductances of the multi-conductor system at the *significant frequency*.
2. Run Raphael RC2/RC3 to determine the p-u-l coupling capacitances.
3. Partition the multi-conductor system into *N* sections and form the RLC equivalent circuit with all couplings for each segment.



The equivalent RLC circuit for the four-wire structure with Half-sections for line termination.

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How many sections, N, or how short each section should be?

At and above the cutoff frequency $\omega_h = \frac{2}{\sqrt{LC}}$, the input impedance is purely imaginary, and no power of those frequencies can be delivered to the line. Therefore, we must let the cutoff frequency well above the highest frequency of interest, which determines the L and C, or the section length.

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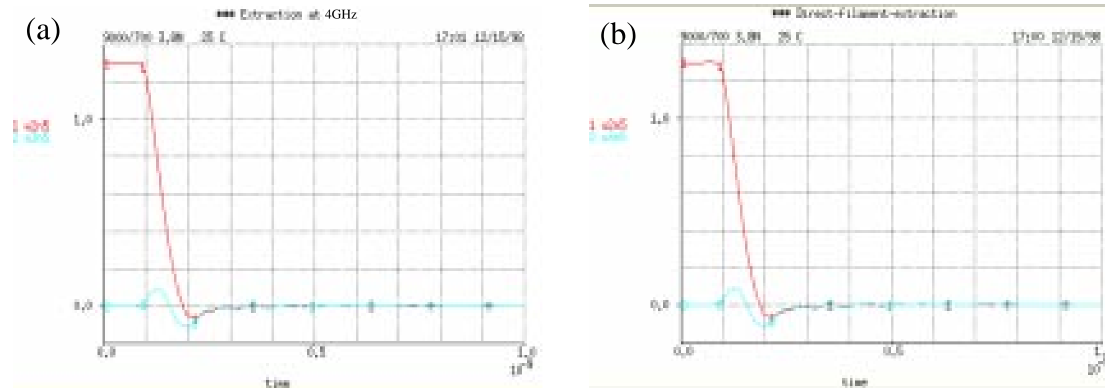
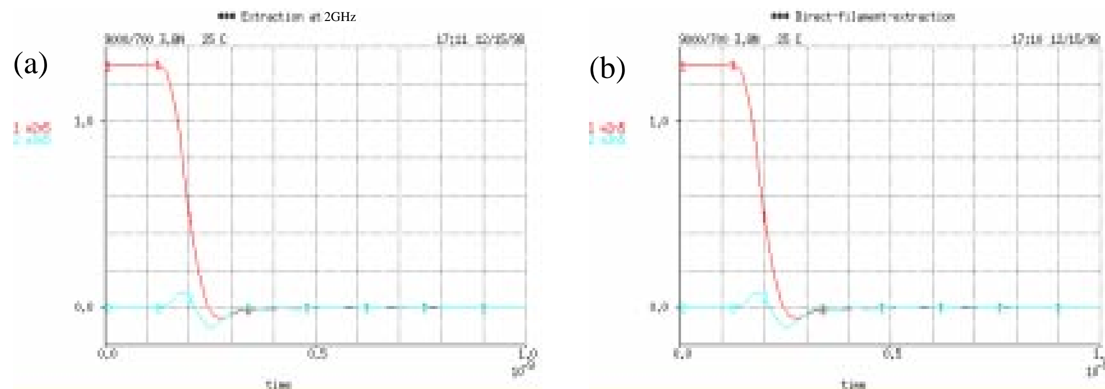
The resistances and inductances extracted at the significant frequency achieve an accuracy of frequency-dependent resistance and inductance:



Comparisons between waveforms at the far ends of wire2 and wire3 from the (a) extraction-at-4GHz circuit; (b) direct-filament-extraction circuit.



Comparisons between waveforms at the far ends of wire2 and wire3 from the (a) extraction-at-2GHz circuit; (b) direct-filament-extraction circuit.

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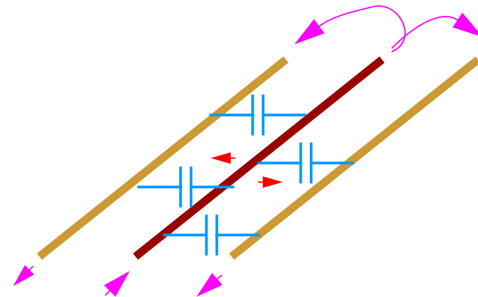
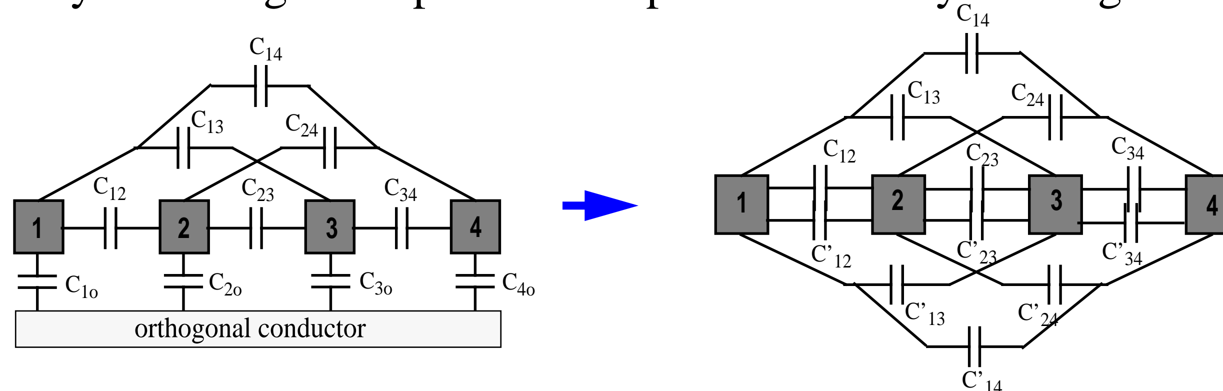
Circuit Modeling (cont.)

Common mistakes:

1. By assuming the inductances are scalable.
2. By conjecturing PEEC over-estimates the inductances since it ignores high frequency returns through coupling capacitors.



3. By assuming the capacitors coupled to other layers are grounded.



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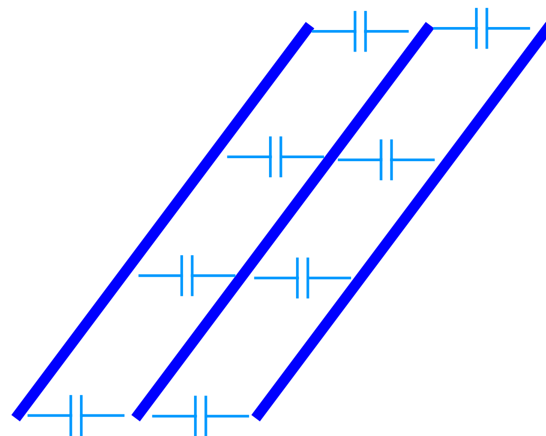
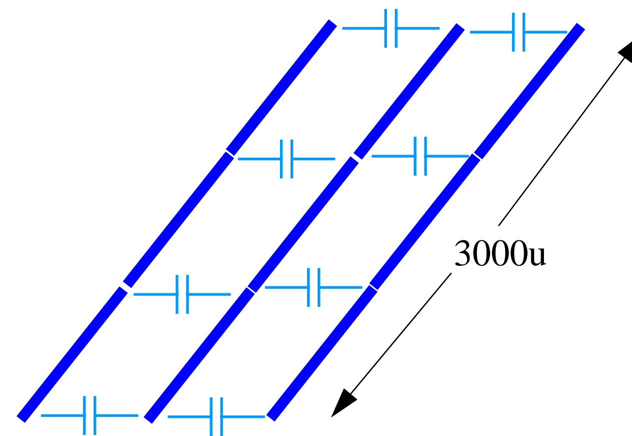
To verify the quasi-static assumption,
the following inductance extractions were compared



VS.



3 3-wire sections
3x3 L matrix

3x3 wire segments
9x9 L matrix

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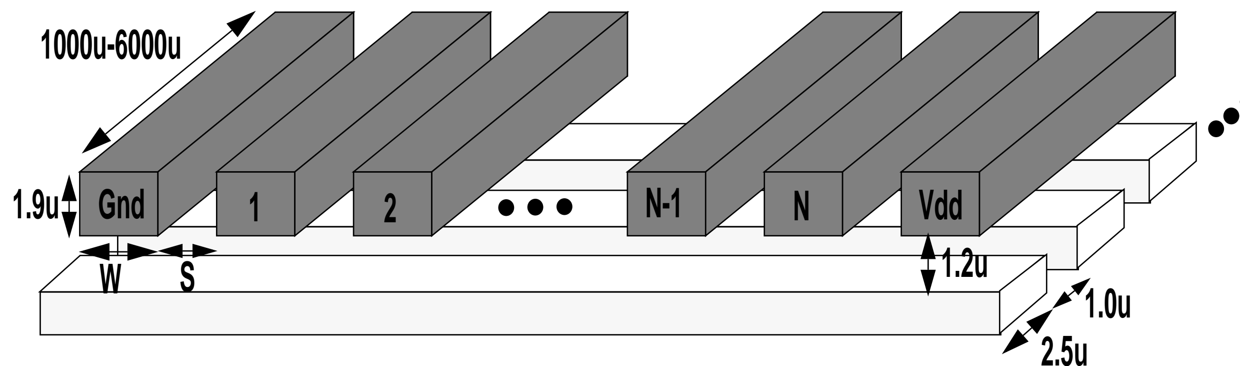
Inductance Impacts



An interconnect structure with N signal wires, 1000 μm to 6000 μm long, 1.9 μm thick, W of width, and sandwiched by Gnd and Vdd wires. The spacing between the wires is S. The gap to the orthogonal layer below is 1.2 μm.

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Inductance Impacts (cont.)

Cross-talk comparisons between the cases with and without the consideration of inductance:

Structures	with inductance	w/o inductance	% error
1000 μm -long	Z_{DRV} = 72 Ohm		
0.8um-wide 8-signal-wire	377 mV	340 mV	10%
2.5um-wide 8-signal-wire	393 mV	302 mV	23%
5.0um-wide 8-signal-wire	452 mV	259 mV	43%
2000 μm -long	Z_{DRV} = 46 Ohm		
0.8um-wide 8-signal-wire	457 mV	570 mV	25%
0.8um-wide 16-signal-wire	479 mV	604 mV	26%
2.5um-wide 8-signal-wire	531 mV	312 mV	41%
2.5um-wide 16-signal-wire	693 mV	326 mV	53%
5um-wide 8-signal-wire	619 mV	246 mV	60%
5um-wide 16-signal-wire	741 mV	269 mV	64%
4000 μm -long	Z_{DRV} = 46 Ohm		
0.8um-wide 8-signal-wire	664 mV	798 mV	20%
0.8um-wide 16-signal-wire	729 mV	891 mV	22%
2.5um-wide 8-signal-wire	482 mV	615 mV	28%
2.5um-wide 16-signal-wire	501 mV	677 mV	35%
5um-wide 8-signal-wire	607 mV	464 mV	24%
5um-wide 16-signal-wire	677 mV	533 mV	21%
6000 μm -long	Z_{DRV} = 46 Ohm		
0.8um-wide 8-signal-wire	764 mV	871mV	14%
2.5um-wide 8-signal-wire	559 mV	701 mV	25%
5um-wide 8-signal-wire	485 mV	567 mV	17%

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Inductance Impacts (cont.)

Interconnect delay comparisons between the cases with and without the consideration of inductance:

Structures	with inductance	w/o inductance	% error
1000 μm -long	Z_{DRV} = 72 Ohm		
0.8um-wide 8-signal-wire	6.0 ps	6.8 ps	13%
2.5um-wide 8-signal-wire	9.0 ps	1.8 ps	80%
5um-wide 8-signal-wire	11 ps	1.0 ps	91%
2000 μm -long	Z_{DRV} = 46 Ohm		
0.8um-wide 8-signal-wire	40.6 ps	27.2 ps	33%
0.8um-wide 16-signal-wire	43.1 ps	27.9 ps	35%
2.5um-wide 8-signal-wire	38.1 ps	6.6 ps	83%
2.5um-wide 16-signal-wire	44.2 ps	6.7 ps	85%
5um-wide 8-signal-wire	36.8 ps	3.3 ps	91%
5um-wide 16-signal-wire	41.3 ps	3.4 ps	92%
4000 μm -long	Z_{DRV} = 46 Ohm		
0.8um-wide 8-signal-wire	125 ps	105 ps	16%
0.8um-wide 16-signal-wire	127 ps	103 ps	19%
2.5um-wide 8-signal-wire	50.0 ps	26.7 ps	47%
2.5um-wide 16-signal-wire	67.0 ps	26.9 ps	60%
5um-wide 8-signal-wire	48.5 ps	13.6 ps	72%
5um-wide 16-signal-wire	61.0 ps	13.0 ps	79%
6000 μm -long	Z_{DRV} = 46 Ohm		
0.8um-wide 8-signal-wire	381 ps	329 ps	14%
2.5um-wide 8-signal-wire	96 ps	73 ps	24%
5um-wide 8-signal-wire	70 ps	36 ps	49%

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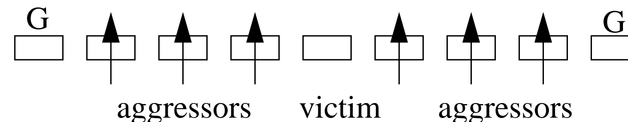
Summary of Inductance Impact Simulations

1. 0.8u-wide or narrower wires do not have significant inductance effects.
2. The worst case is all aggressors switch in the same direction



3. In general, with the inductance effects, signal rises faster but delay is longer. The most serious inductance impact is the high-Q ringing, where

$$Q \approx \frac{\sqrt{L/C}}{R_s + R} \qquad Overshoot = \exp\left(\frac{-\pi}{\sqrt{4Q^2 - 1}}\right)$$

   The rise times shorter than one-half $2\pi\sqrt{LC}$ incur the worst ringing.

4. The inductive crosstalk noise tops off at lengths of around 4000u to 6000u length.

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Purpose of Inductance Screen

Accurate and stable RLC delay and cross-talk estimations still rely on computation-intensive simulations. Determining which nets require the special consideration of inductance is important because designers may apply those RC delay and cross-talk prediction methods, proven to be fast and reliable, to as many nets as possible.

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Previous Work on Self-Inductance Screen

1. *A. Deutsch, et al,* "When are Transmission-Line Effects Important for On-Chip Interconnects?" IEEE Trans. MTT, Oct. 1997:

The error in delay or cross-talk prediction between RC and RLC modelings will exceed 20% if

$$C_L \ll C\,l$$

$$\frac{R\,l}{2\,Z_o} \leq 1$$

$$Z_{DRV} < n\,Z_o$$

However, due to the lack of a ground plane or mesh on chip, the inductive coupling may extend to very long range. Most on-chip wires may not be modeled as uniform RLC transmission lines. Hence, Z_o is not defined. In general, for about 100ps rise time, those lines shorter than 3000u may not be distributed elements.

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Previous Work on Self-Inductance Screen (cont.)

2. *Yehea I. Ismail, et al*,"Figures of Merit to Characterize the Importance of On-Chip Inductance," Proc. 35-th DAC, June 1998:

Condition for an interconnect of length l to consider inductance is

$$\frac{t_r}{2\sqrt{LC}} < l < \frac{2}{R}\sqrt{\frac{L}{C}}$$

where t_r is the signal rise time at the **input** of the driver.

However, the match-or-under-drive assumption used by the approach may not be true for future advanced high speed designs.

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Self-Inductance Screening Rules

Based on the simulations performed and the fact that the inductive effects decrease with the increase of length, it was concluded that designers need to consider the inductance of when

$$C_L < \frac{1}{8} C\, l \qquad (1)$$
$$l \le \frac{2}{R}\sqrt{\frac{L}{C}}$$
$$2\pi f_s L l > \frac{(Rl + Z_{DRV})}{2}$$

Under these criteria, the inductive reactance occupies more than one-third of the total reactance, and the delay and cross-talk errors, without considering inductance, exceeded 25%. When the values of Cl and C_L were close, such as in the 1000um-long structures, the inductance effects (e.g., oscillations) tended to show up. Therefore, under the conditions

$$C_L > \frac{1}{8} C\, l \qquad (2)$$
$$l \le \frac{2}{R}\sqrt{\frac{L}{C}}$$
$$2\pi f_s L l > \frac{(Rl + Z_{DRV})}{4}$$

the delay and cross-talk errors, without considering inductance, might exceed 25%.

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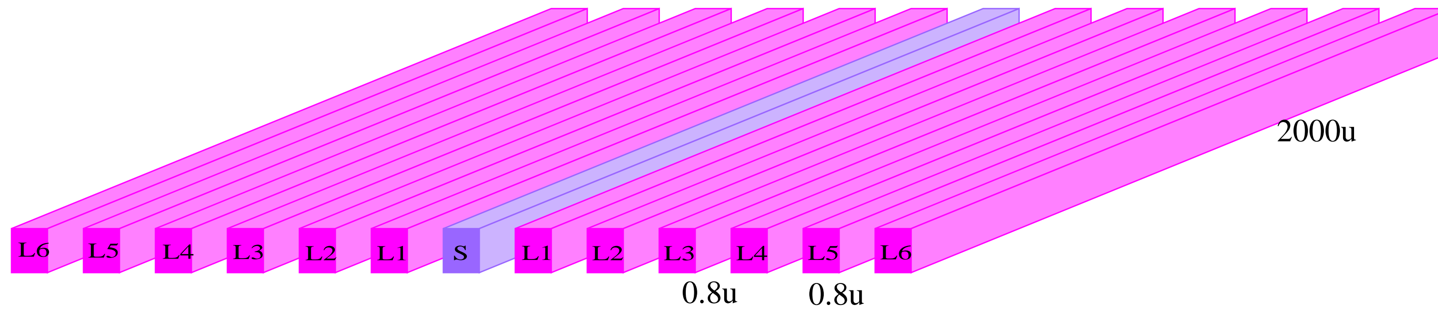
Mutual-Inductance Screening Rules

Distribution of High Frequency Return Currents



		L6	L5	L4	L3	L2	L1
1.9u thick	Loop Ind.	2.21 n	2.06 n	1.88 n	1.65 n	1.31 n	0.689 n
1K-1G Hz	% current	5.3%	5.6%	6.2%	7.0%	8.8%	17%
0.95u thick	Loop Ind.	2.56 n	2.41 n	2.23 n	2.00 n	1.68 n	1.12 n
1 GHz	% current	6.0%	6.4%	6.9%	7.7%	9.2%	13.8%
1.9u thick	Loop Ind.	2.20 n	2.05 n	1.87 n	1.63 n	1.30 n	0.680 n
10 GHz	% current	5.2%	5.6%	6.2%	7.1%	8.9%	17%
1.9u thick	Loop Ind.	1.75 n	1.51 n	1.30 n	1.06 n	0.767 n	0.400 n
100 GHz	% current	4.2%	4.9%	5.7%	7.0%	9.7%	18.5%

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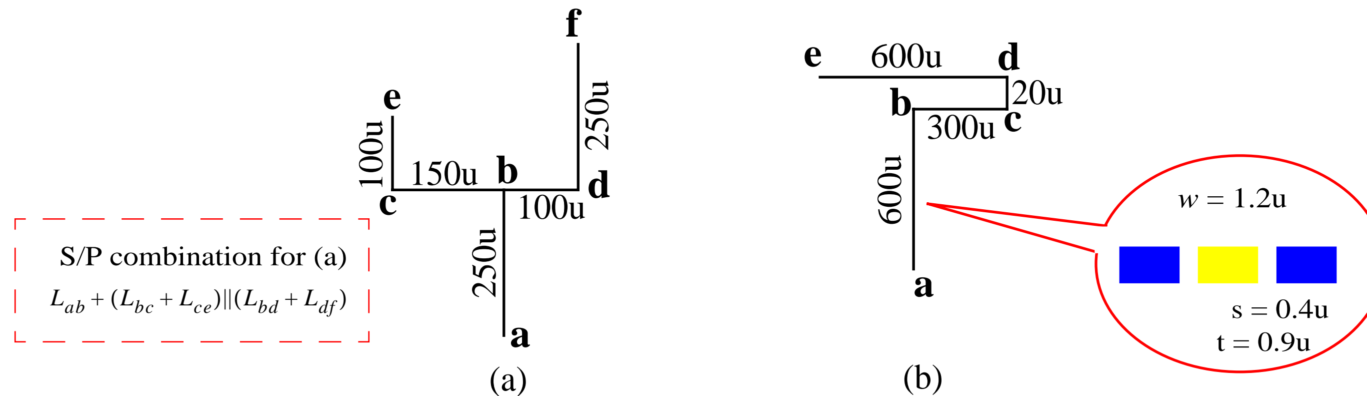
Mutual-Inductance Screening Rules (cont.)

Inductance Modeling for Cascaded Wire Segments



Two interconnect trees. Each segment of the trees is a three-same-width-wire multi-conductor system.

	Loop L from RI3	Effective Loop L from S/P combination	Error%
Fig. (a)	0.140 nH	0.145 nH	3.57%
Fig. (b)	0.517 nH	0.525 nH	1.55%

Linear Cascading Comparisons to demonstrate the effectiveness of *2x* shielding.

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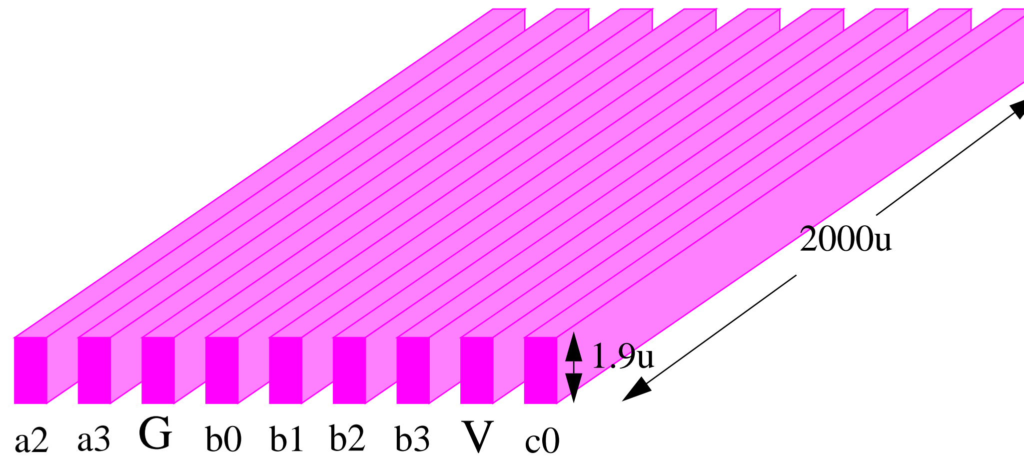

Drivers are Buf130 and receivers are Buf40 (CMOS 0.18u technology).

signal wires are 2.5u wide with 1.25u spacing	**Gnd/Vdd wire width**	**xtalk noise at a3**
b0-b3 switch up, c0 switches up	7.5u	0.73 mV
b0-b3 switch up, c0 quiet	7.5u	0.66 mV
b0-b3 switch up, e0 switches up	10.0u	0.48 mV
b0-b3 switch up; c0 quiet	10.0u	0.41 mV

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Mutual-Inductance Screening Rules (cont.)

1. In order to provide enough current return (shielding), the width of the return path should be at least *two* times the total width of all simultaneously switching signals using that return path.

2. Quiet signal wire is as good as a ground wire of equal width for high frequency current return (less than 5% differences on delay and xtalk seen when the vdd wire is replaced by a quiet signal wire in 0.8u case).

3. Low frequency currents may always find a ground wire (or ground wires) for return.

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Efficient Inductance Modelings

1. *The self-partially loop inductance for a trace on top of a ground plane or in-between ground planes depends only on the trace's geometry (length, width, and thickness).*

Partially-loop inductance is defined as the loop inductance assuming that currents return only through the ground plane(s).

2. *The mutual-partially loop inductance for two traces on top of a ground plane or in-between ground planes depends only on their geometry (lengths, widths, thicknesses, and spacing).*

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Efficient Inductance Modelings (cont.)

Table-based Inductance Extraction:

1. Run RI3 or FastHenry to determine the self-inductances for traces, microstrip- and strip-lines of several widths, lengths, and thicknesses. Store the results in a table.
2. Run RI3 or FastHenry to determine mutual-inductances for two-line traces, microstrip- and strip-lines of several lengths, widths, thicknesses, and spacings. Store the results in a table.
3. To determine the inductances of an arbitrary trace, microstrip- or strip-line, or of an arbitrary two-line traces, microstrip- or strip-lines, use interpolations, such as cubic spline, from the inductances of the closest line-structures predetermined in previous tables.

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Inductance Test Chip Benchmark

Objective:

1. Extract frequency-dependent R, C, and L from test structures
2. Compare measurement and simulation

Previous Works:

1. IBM Research Report (1995), A. Deutsch, et. al., IBM
2. IITC Poster (1999), R. J. Friar, et. al., U. of Texas at Austin
3. IEDM Paper (1999), B. Keveland, et. al., Stanford U.

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Benchmark Chip

6 Types of Test Tracks

- Microstrip line
- Coplanar waveguide
- Microstrip line under a power rail
- Coplanar split lines
- Horseshoe lines
- Meshes

Chip Size = 4800 um x 6270 um

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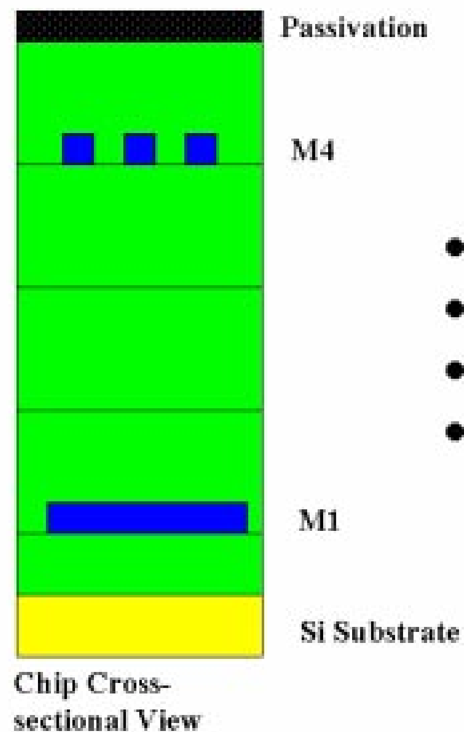
Chip Process



- HP 0.35um from MOSIS
- Back-end only
- Minimum Pitch = 1.4um
- Al / Oxide

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S-Parameter Measurement

Scattering Parameter

- Relates incident and reflected voltage waves
- 0 < S <1 for a passive system
  (good dynamic range for measurement)

Measurement System

- HP8510 Network Analyzer (45MHz ~ 20GHz)
  (upper range limited to ~10GHz by resonance)

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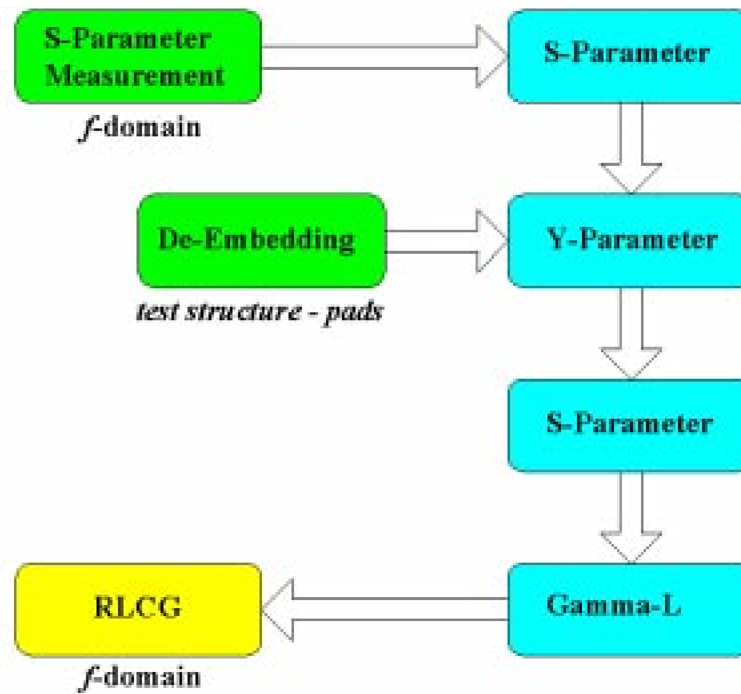
RLC Extraction Process



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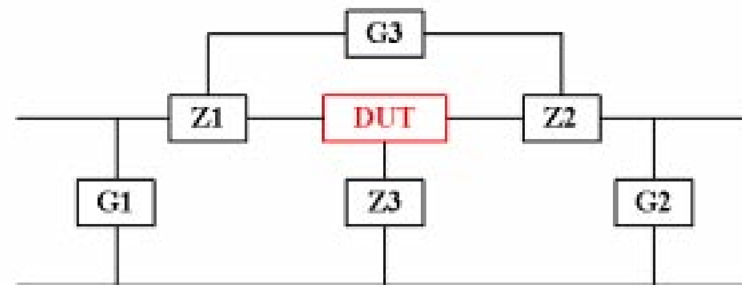
De-Embedding

1. Subtract shunt admittance from the open measurement. (G1 and G2)

2. Subtract series impedance from the through and short measurements. (Z1, Z2, and Z3)

3. Subtract coupling capacitance from the open measurement. (G3)



H. Cho, *et. al.*, "*A Three-Step Method for the De-Embedding of High Frequency S-Parameter Measurements*", IEEE Trans. on Electron Devices, Jan. 1991.

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RLC Extraction - I

Conversion to $\gamma\, l$

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1}$$

$$K = \left\{ \frac{\left(S_{11}^2 - S_{21}^2 + 1\right)^2 - (2S_{11})^2}{(2S_{21})^2} \right\}^{1/2}$$

$$Z^2 = Z_o^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2}$$

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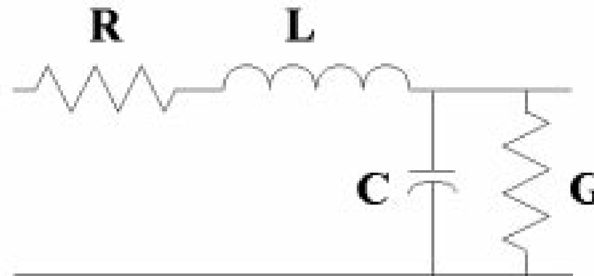
RLC Extraction - II

Conversion to RLC

$$R = \mathrm{Re}\{\gamma Z\}$$
$$L = \mathrm{Im}\{\gamma Z\}/\omega$$
$$C = \mathrm{Im}\{\gamma / Z\}/\omega$$



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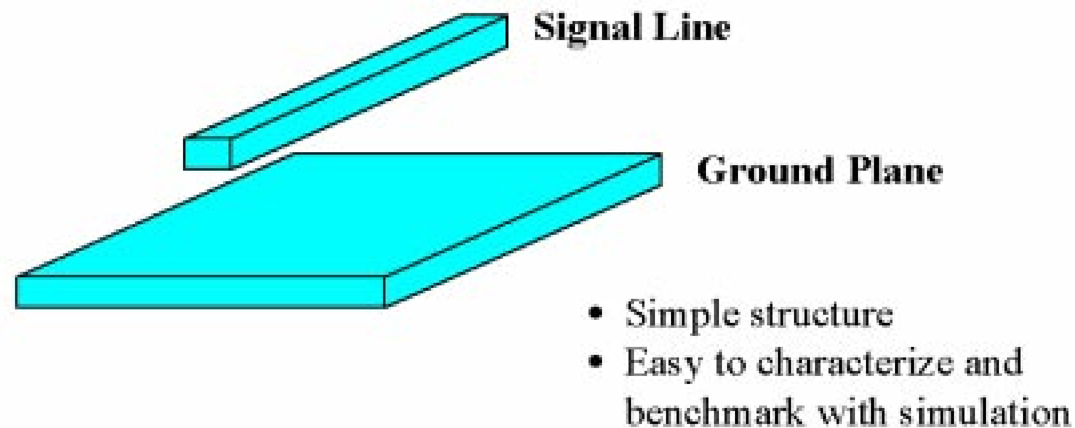
Microstrip Line

Signal line over a ground plane



- Simple structure
- Easy to characterize and benchmark with simulation

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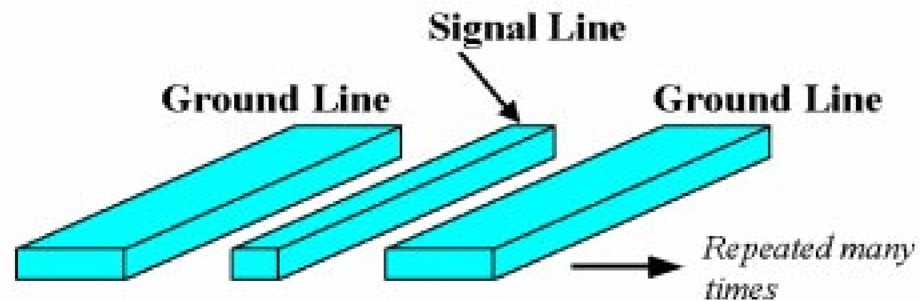
Coplanar Waveguide

Signal line bounded by ground lines

- Simple structure
- Easy to characterize and benchmark with simulation



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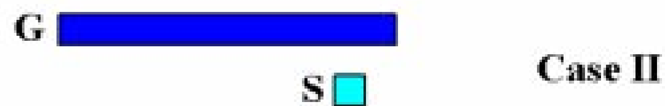
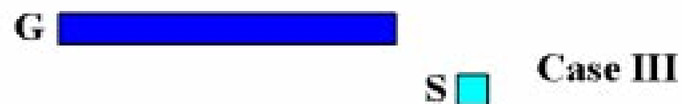
Microstrip Line Under Power Rail

Signal line position varies w.r.t. the power rail

Case I



Case II



Case III

- Is proximity of a signal line to ground important?

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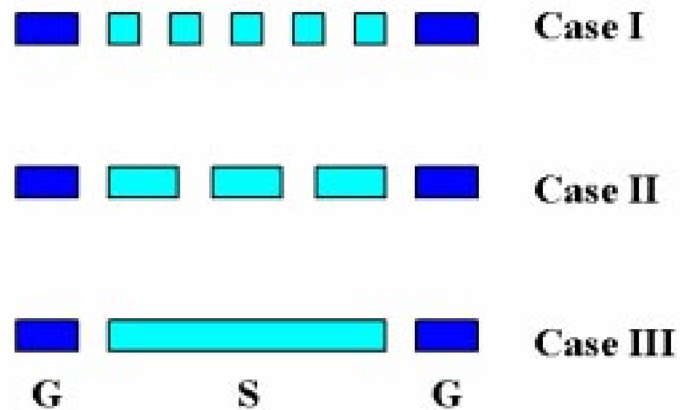
Coplanar Split Lines

Constant total width



- Are split narrow lines better than a wide line?

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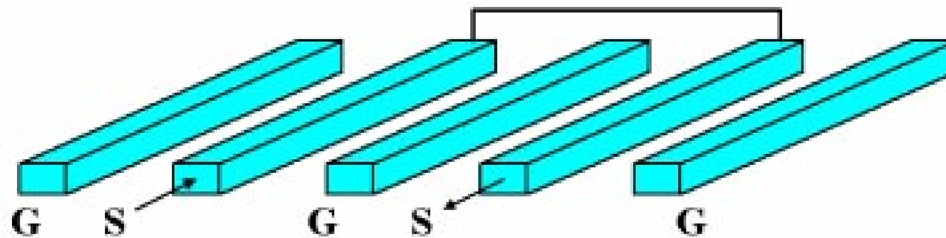
Horseshoe Lines

Signal line with U-turn

- In clock nets to match skew
- What's the impact of mutual inductance?



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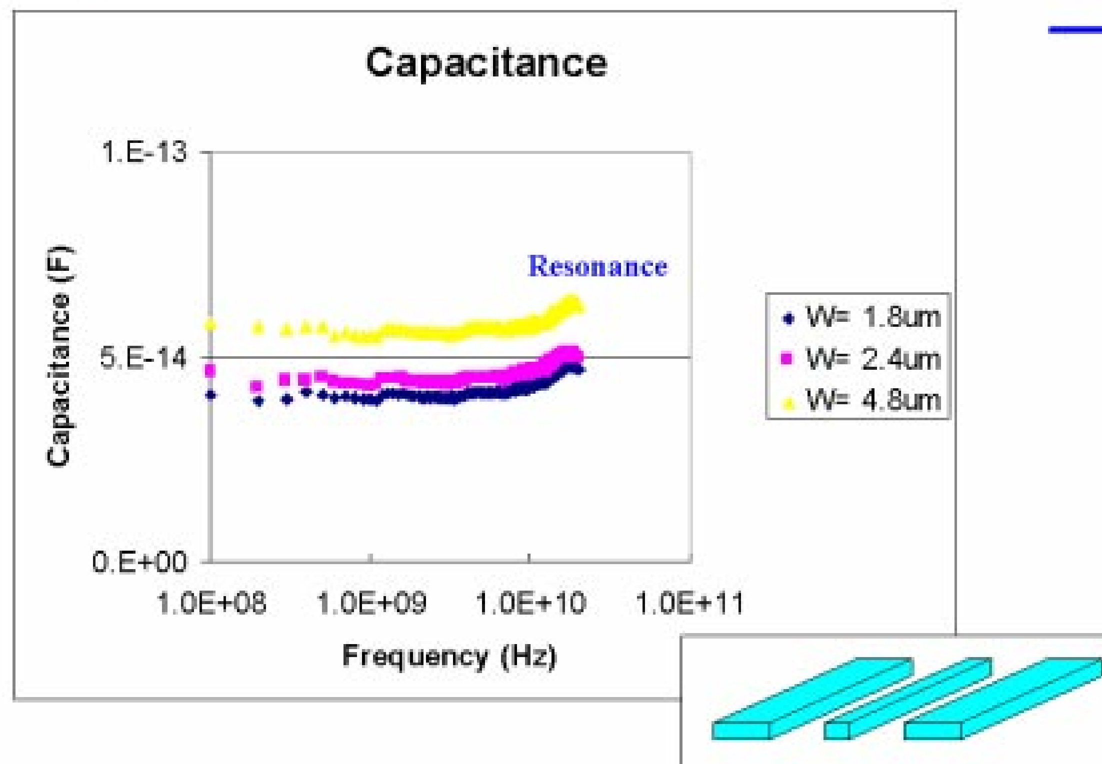
Coplanar Waveguide : C Data



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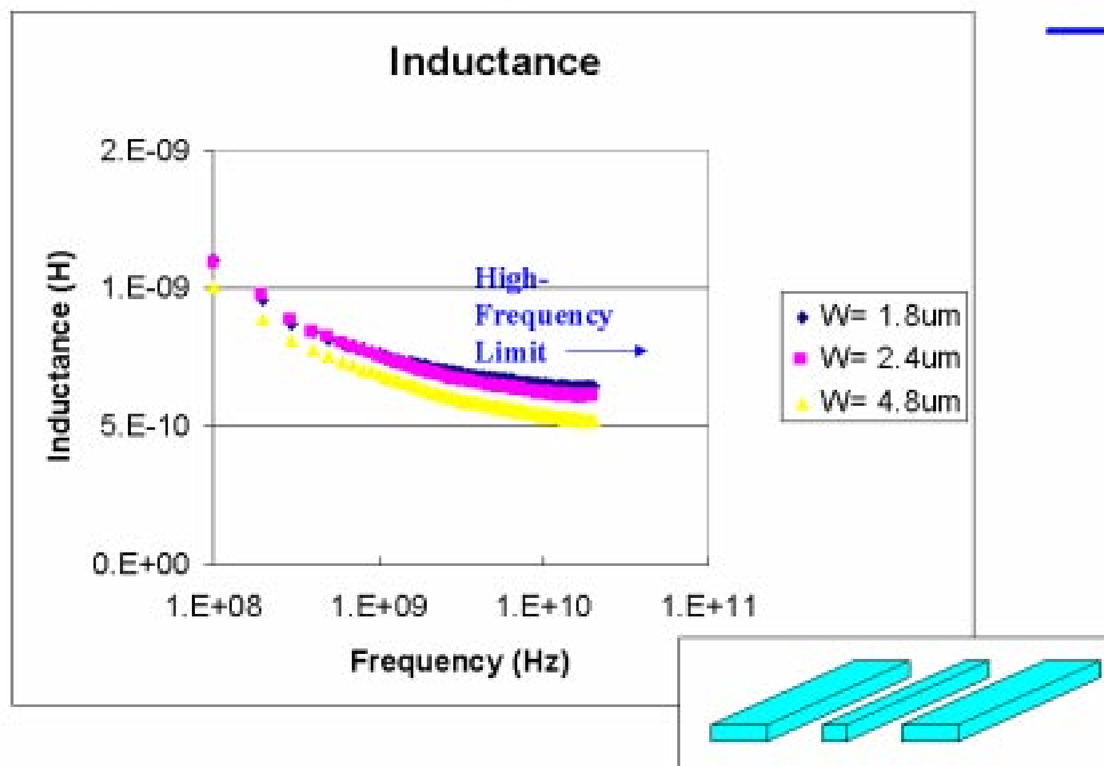
Coplanar Waveguide : L Data



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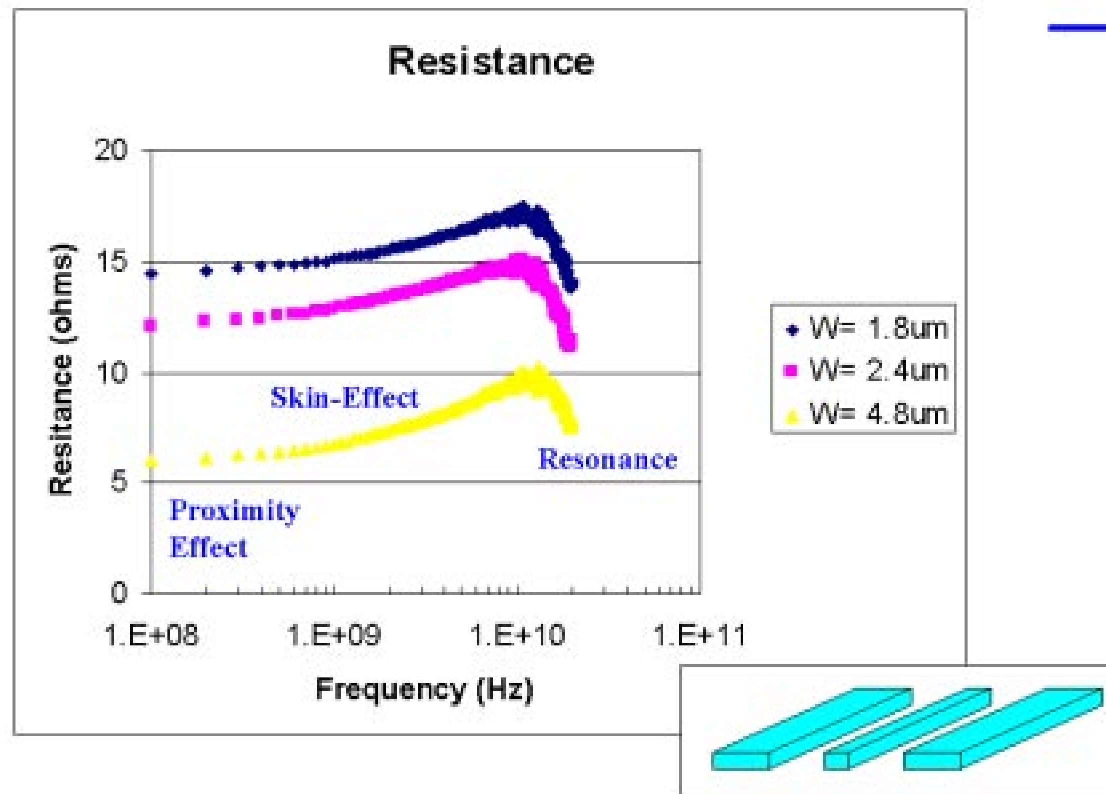
Coplanar Waveguide : R Data



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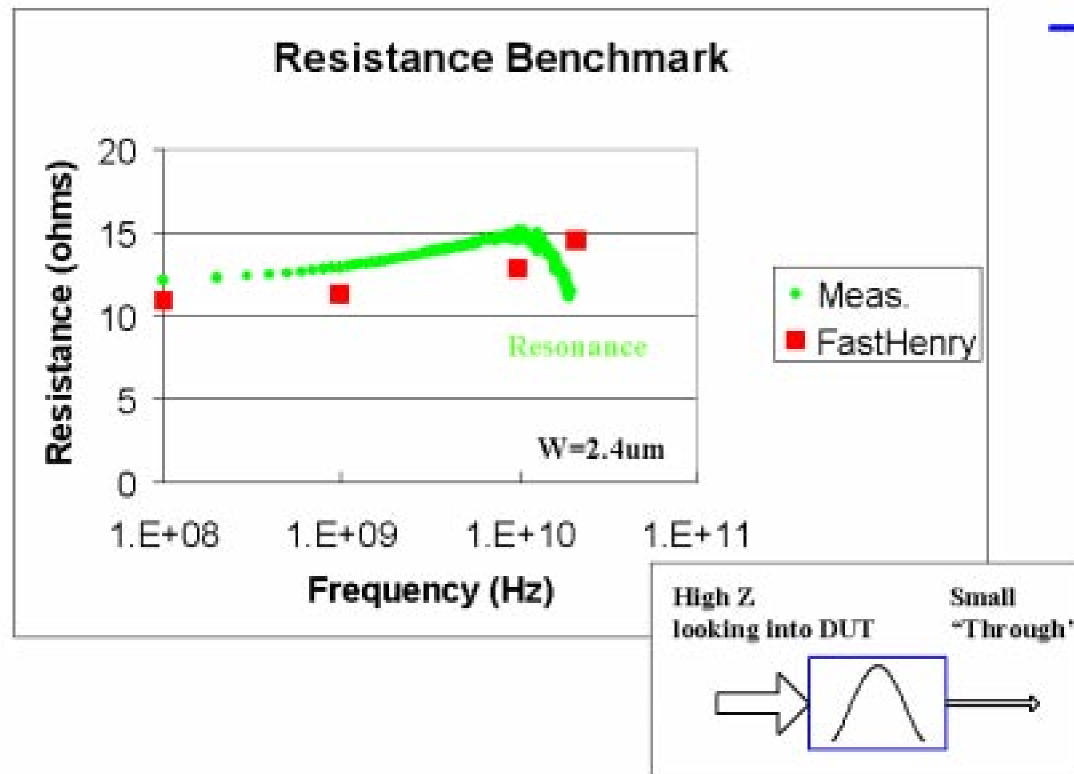
Coplanar Waveguide : R Benchmark



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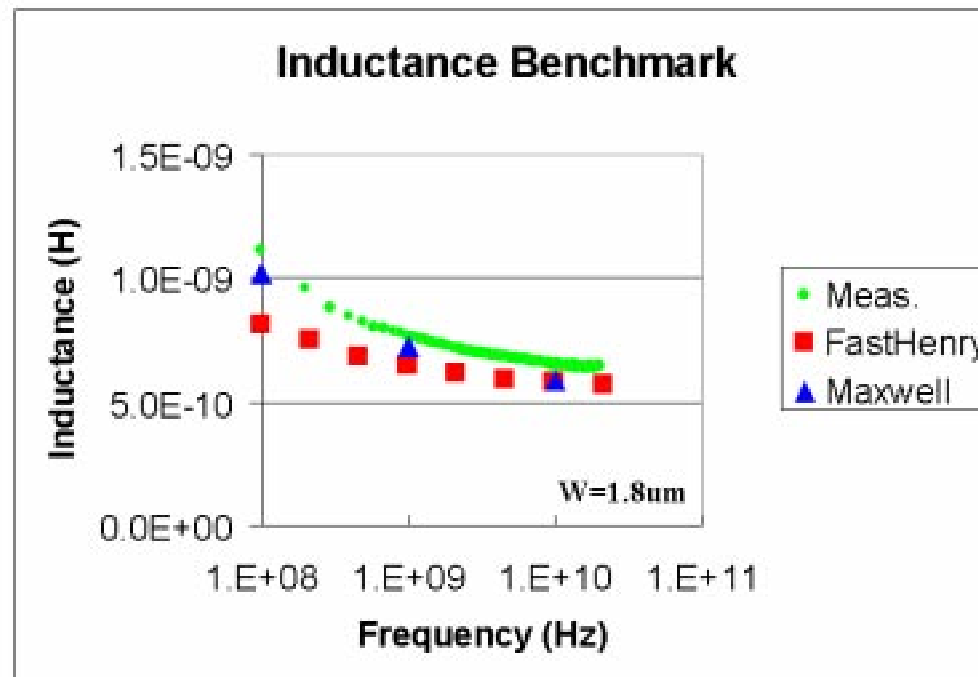
– Coplanar Waveguide : L Benchmark



FastHenry (MIT): 3D Quasi-Static Field Solver
Maxwell (AnSoft): 2-1/2D Full-wave Field Solver

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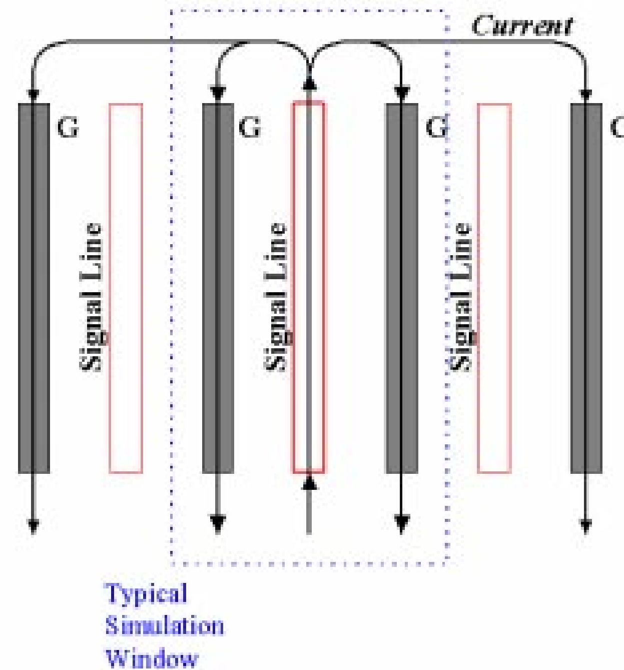
Coplanar Waveguide : Return Paths



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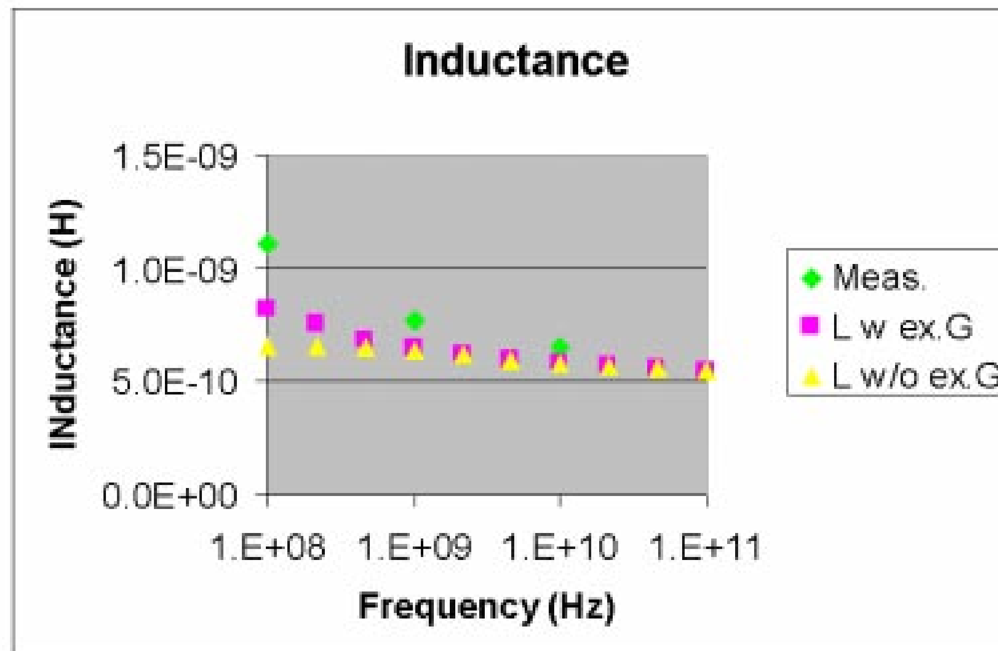
Coplanar Waveguide : Return Paths



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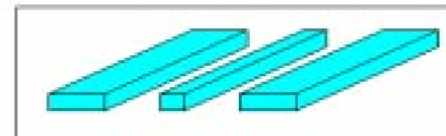
Coplanar Waveguide : Summary

- The measured R and L are in reasonable agreement with the simulated R and L.
- At low frequency the return current spreads over multiple ground lines, leading to slightly higher inductance.



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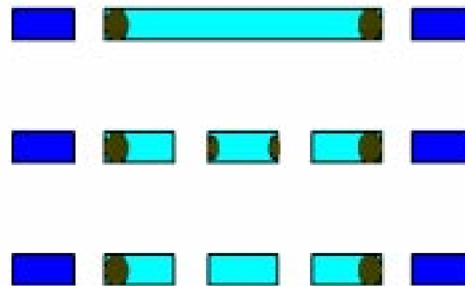
Coplanar Split Lines

Case	W	S	ΣW+ΣS
1 x 12um	12um	0um	12um
2 x 5.4um	5.4um	1.2um	12um
3 x 3.2um	3.2um	1.2um	12um
4 x 2.1um	2.1um	1.2um	12um

Wg=Ws=1.2um



Current in inner lines
or
Not?

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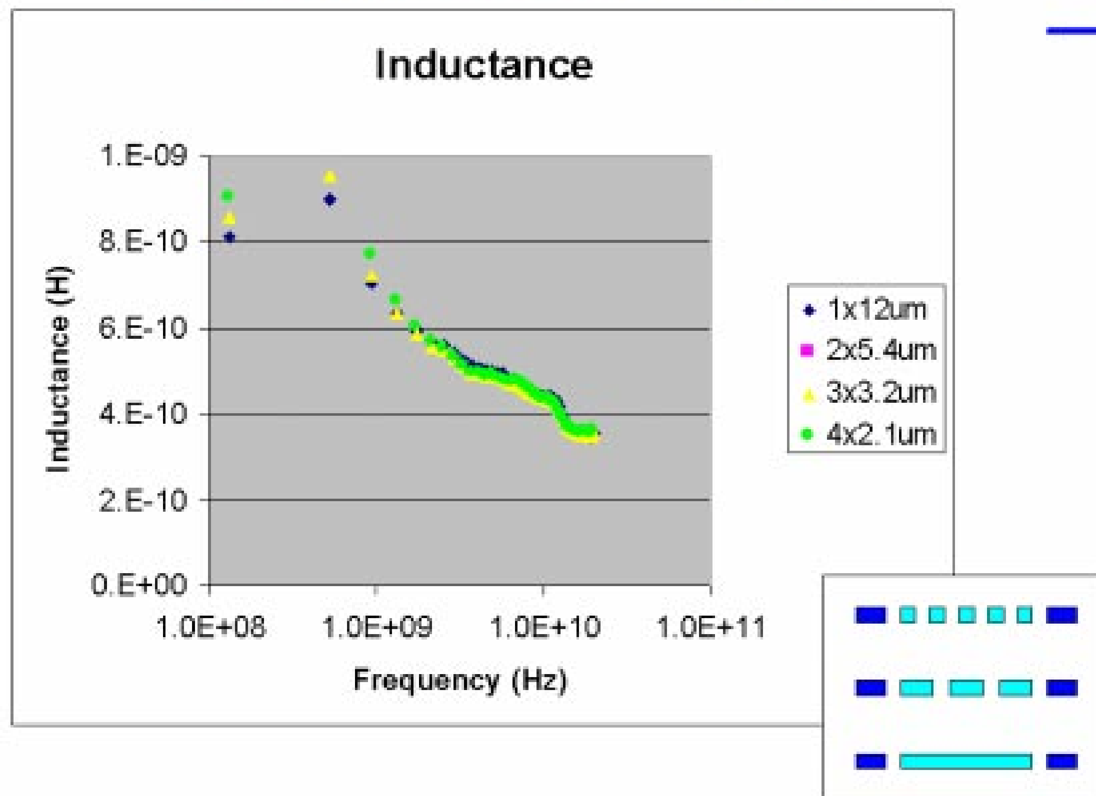
Coplanar Split Lines



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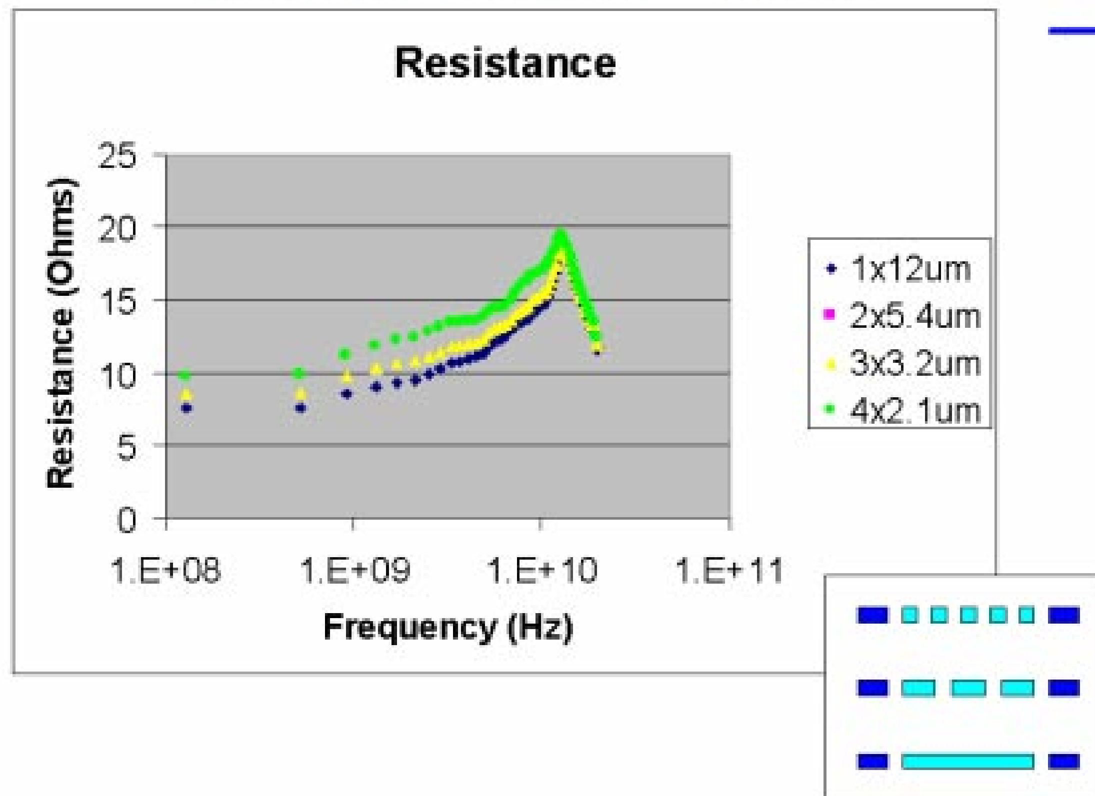
Coplanar Split Lines



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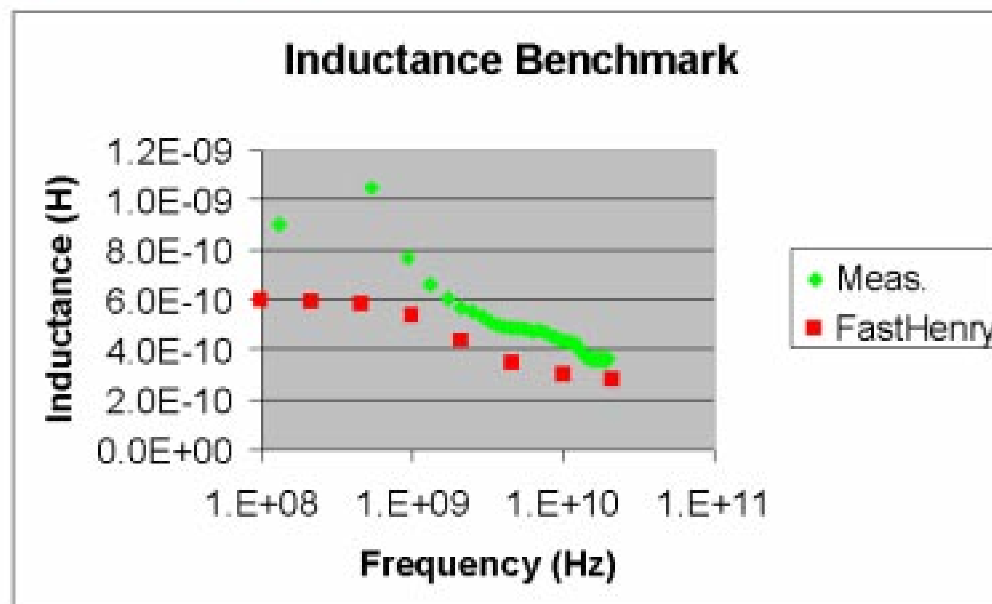
Split-Coplanar : L Benchmark



FastHenry (MIT): 3D Quasi-Static Field Solver

W=1.8um

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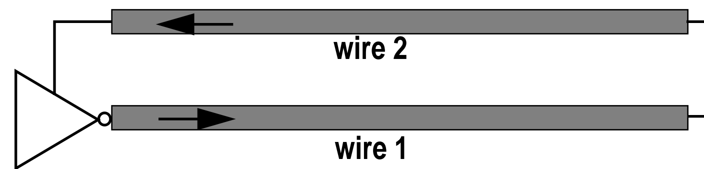
Techniques to Minimize Inductance Effects

1. Dedicated Ground Wires



$$L_{loop} = L_{11} - L_{12} + L_{22} - L_{21}$$

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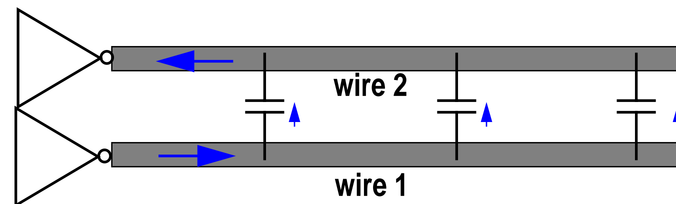
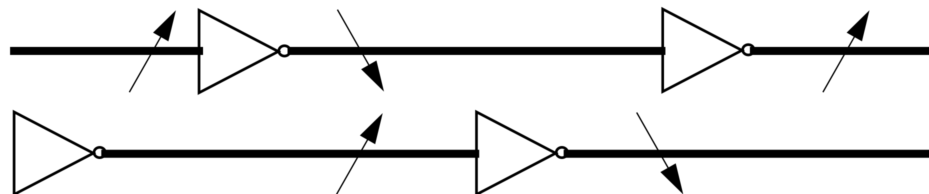
Techniques to Minimize Inductance Effects (cont.)

2. Differential Signals



Common mode noises, such as inductive, may be rejected.



But, the design suffers from longer delays due to Miller effect.

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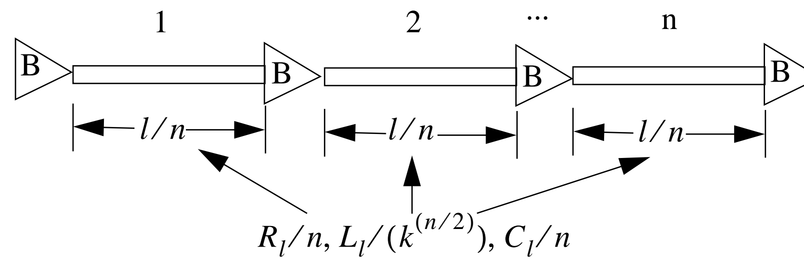
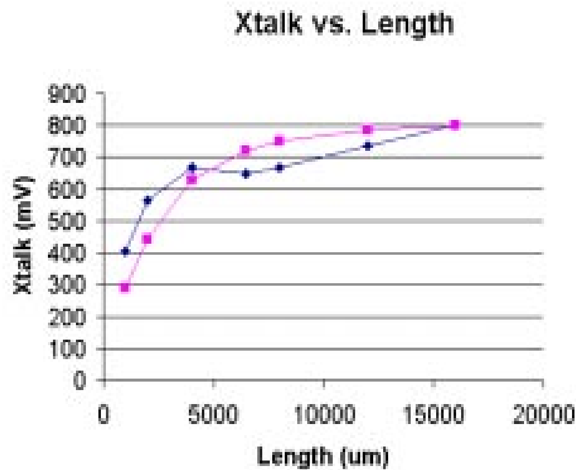
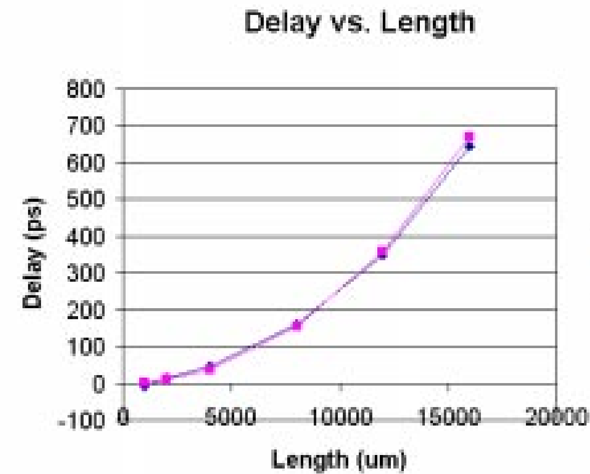
Techniques to Minimize Inductance Effects (cont.)

3. Buffer Insertion







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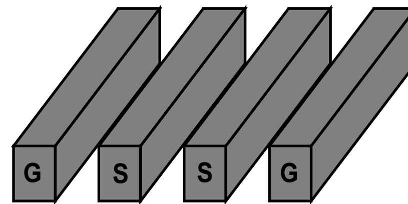
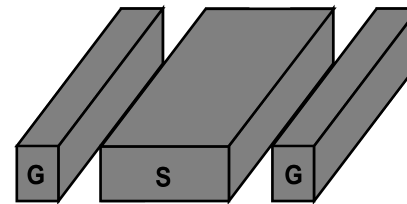
Techniques to Minimize Inductance Effects (cont.)

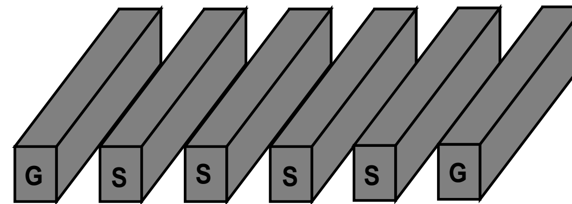
4. Splitting Wires



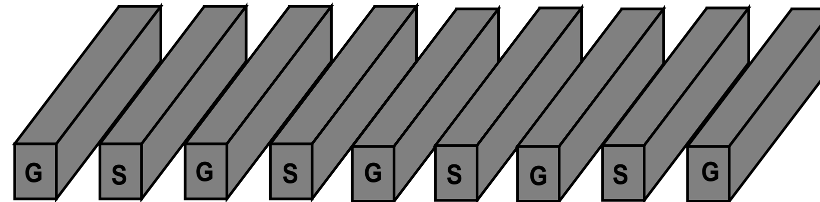
(a)



(b)



(c)



(d)

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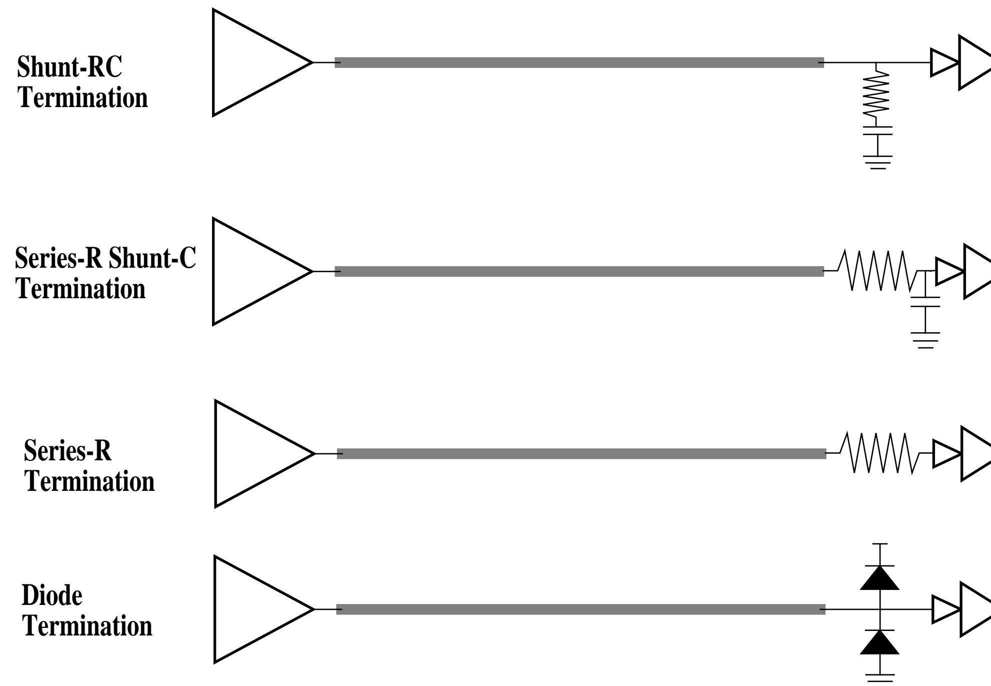
Techniques to Minimize Inductance Effects (cont.)

5. Terminations



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Shunt-RC Termination

R	C	Max. Noise	Wire Delay
none	none	552 mV	21.6 ps
90	0.1 pF	542 mV	28.7 ps
90	0.4 pF	637 mV	34.1 ps
90	0.8 pF	647 mV	37.1 ps
140	0.1 pF	513 mV	28.1 ps
140	0.4 pF	528 mV	30.0 ps
140	0.8 pF	540 mV	31.1 ps
190	**0.1 pF**	**477 mV**	**27.1 ps**
190	0.4 pF	514 mV	27.9 ps
190	0.8 pF	520 mV	28.5 ps

Series-R Shunt-C Termination

R	C	Max. Noise	Wire Delay
none	none	552 mV	21.6 ps
90	0.1 pF	457 mV	38.7 ps
90	0.4 pF	372 mV	65.1 ps
90	0.8 pF	307 mV	97.1 ps
140	0.1 pF	291 mV	39.3 ps
140	0.4 pF	246 mV	30.0 ps
140	0.8 pF	172 mV	117 ps
190	**0.1 pF**	**218 mV**	**45.3 ps**
190	0.4 pF	165 mV	85.9 ps
190	0.8 pF	111 mV	140 ps

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Series-R Termination

z_{DRV}	R	Max. Noise	Wire Delay
70	none	552 mV	21.6 ps
70	40	470 mV	22.4 ps
70	90	397 mV	23.6 ps
70	140	376 mV	24.3 ps
70	**190**	**350 mV**	**26.1 ps**
150	none	376 mV	18.9 ps
150	40	339 mV	19.6 ps
150	90	321 mV	20.3 ps
150	140	308 mV	20.9 ps
150	**190**	**295 mV**	**21.5 ps**

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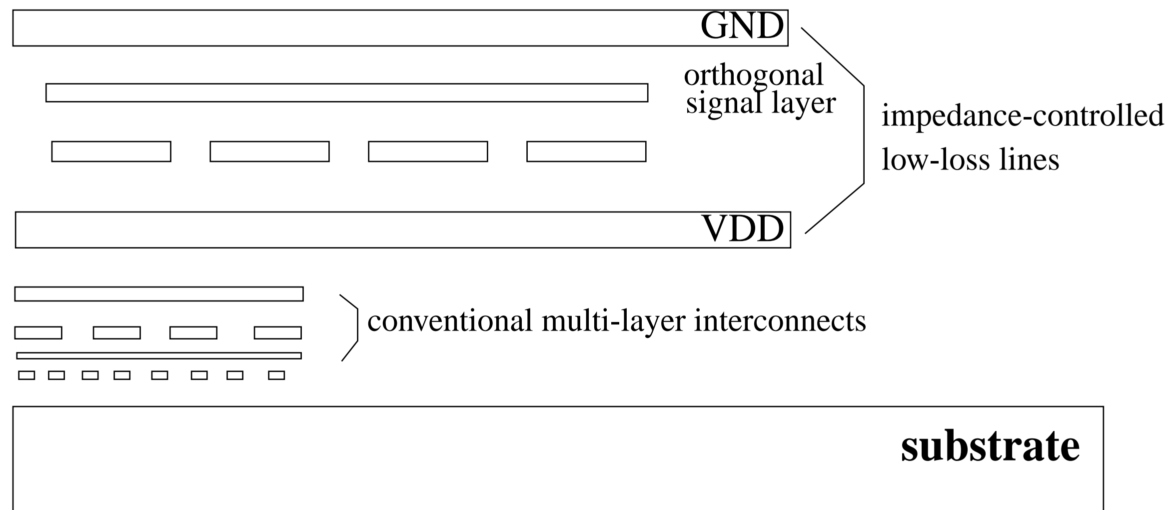
Techniques to Minimize Inductance Effects (cont.)

6. Continuous Power/Ground Planes

Continuous power/ground planes on-chip provides an impedance-controlled low-loss signal lines



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Summary

We discussed

1. the difference between on-chip inductance and off-chip consideration. The on-chip inductance is not scalable and non-orthogonal wires are almost all inductively coupled. Therefore, the on-chip interconnects may not be treated as transmission lines.
2. how to calculate inductance. We mention that partial inductance should be preferred and let the circuit simulator determine the return path.
3. the skin effect and the proximity effect.
4. the inductance impact on delay and cross-talk noise for several interconnect structures, which are mainly caused by over-drive and low resistance. The simulation results lead to the answer of the question “when do we need to consider inductance”.
5. several important design solutions to cope with inductance effects.
6. based on the correct understanding of on-chip inductance, the inductive coupling noise and oscillation caused by over-shoot may be effectively controlled in the future’s multi-GHz chips.

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