Signal Integrity for Gigascale SOC Design

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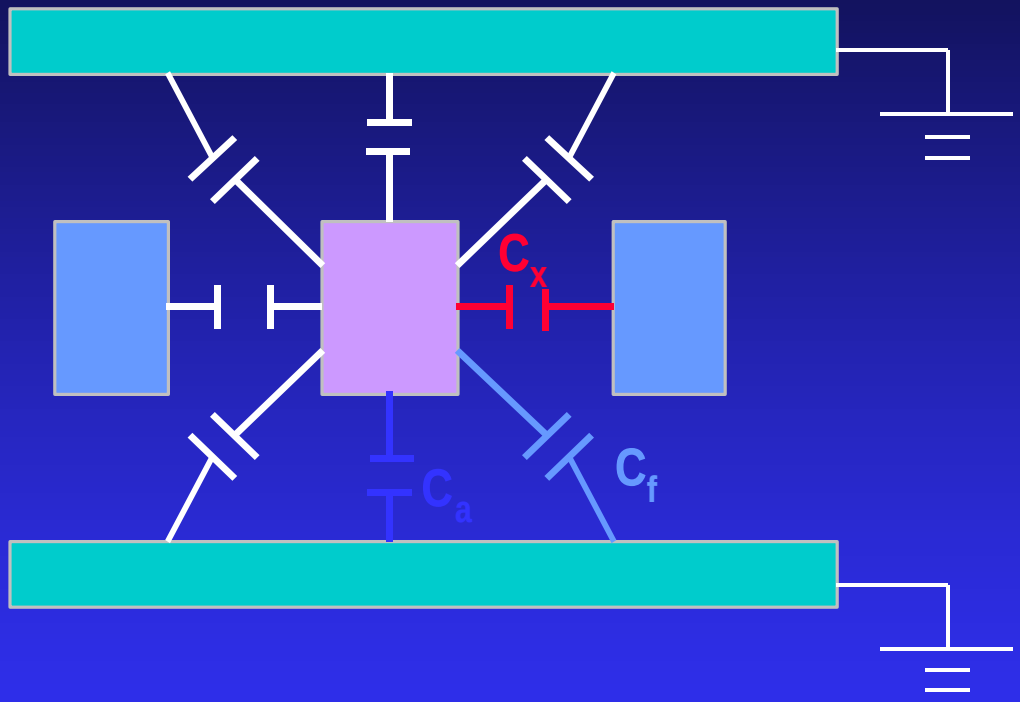
Outline

- Capacitive noise
  - Technology trends
  - Capacitance model and characteristics
  - Layout optimization
- Inductive noise
  - When inductance become important
  - Inductance model and characteristics
  - Layout optimization
- Automatic algorithm
  - SINO algorithm for both Cx and Lx noise

Interconnect Parameters from NTRS'97

Technology (um)	*0.25*	*0.18*	*0.15*	*0.13*	*0.10*	*0.07*
Res. r (uW/cm)	3.3	2.2	2.2	2.2	2.2	1.8
Dielectric constant	3.55	2.75	2.25	1.75	1.75	1.5
Min. wire width	0.25	0.18	0.15	0.13	0.10	0.07
Min. wire spacing	0.34	0.24	0.21	0.17	0.14	0.10
Metal aspect ratio	1.8:1	1.8:1	2.0:1	2.1:1	2.4:1	2.7:1
Via aspect ratio	2.2:1	2.2:1	2.4:1	2.5:1	2.7:1	2.9:1
Vdd (V)	2.15	1.65	1.35	1.35	1.05	0.75

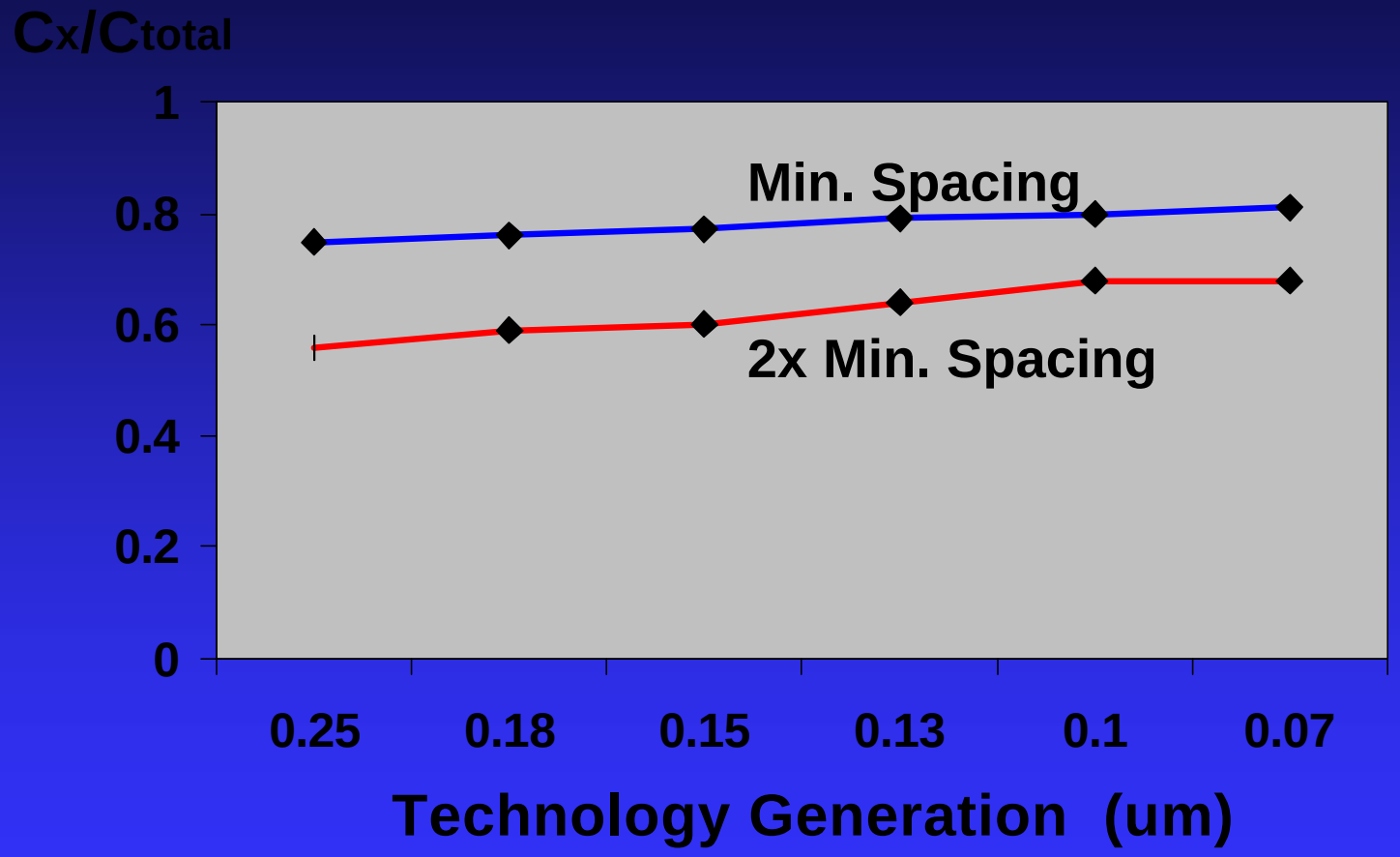
Interconnect Capacitance



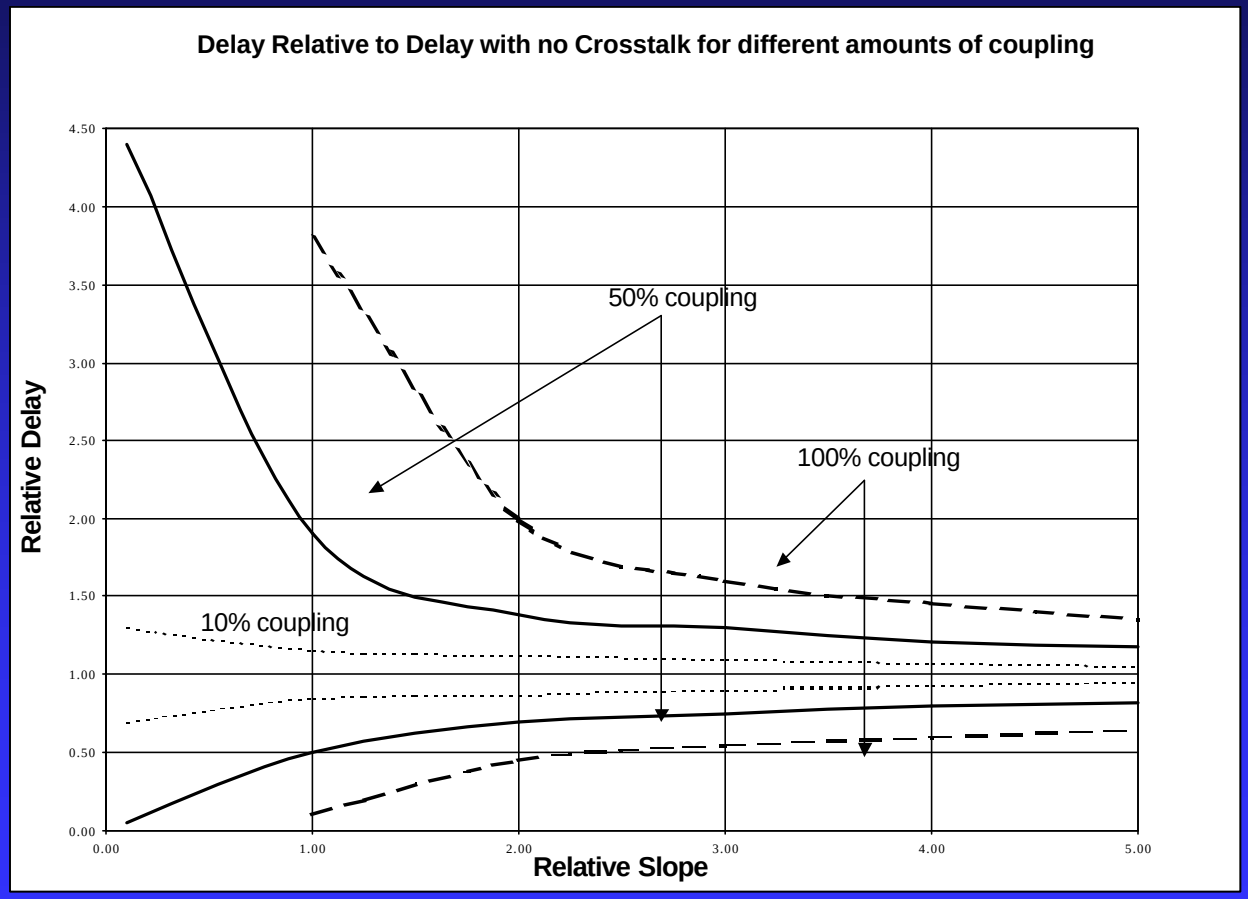
Derived Interconnect & Device Parameters

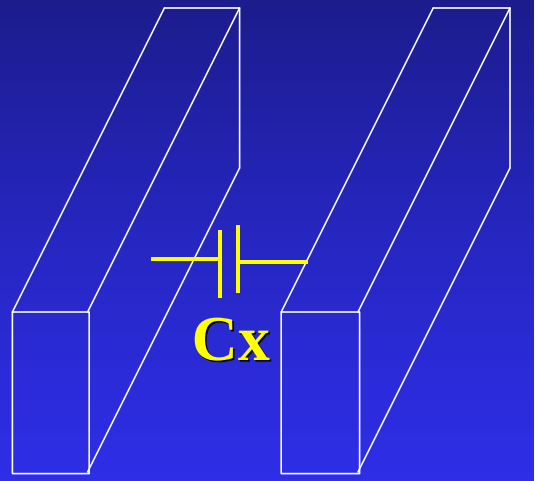
Technology (um)		*0.25*	*0.18*	*0.15*	*0.13*	*0.10*	*0.07*
2X min. width & spacing	Ca (aF/um)	29.0	21.2	16.2	12.0	14.4	8.56
	Cf (aF/um)	41.8	30.2	24.8	18.3	14.1	14.8
	Cx(aF/um)	71.0	58.3	49.4	42.8	45.3	41.6
5X min. width & spacing	Ca (aF/um)	73.5	53.6	40.6	30.0	26.6	19.5
	Cf (aF/um)	63.5	47.3	38.4	28.5	28.2	23.6
	Cx(aF/um)	18.3	16.9	15.4	14.8	16.5	16.7
Buffer input cap. (fF)		0.17	0.12	0.11	0.085	0.070	0.042
Buffer Rd (x10KW)		1.71	1.86	2.26	2.25	2.39	2.42
Buffer intrin. delay (ps)		70.5	51.1	48.7	45.8	39.2	21.9

Significance of Coupling Capacitance

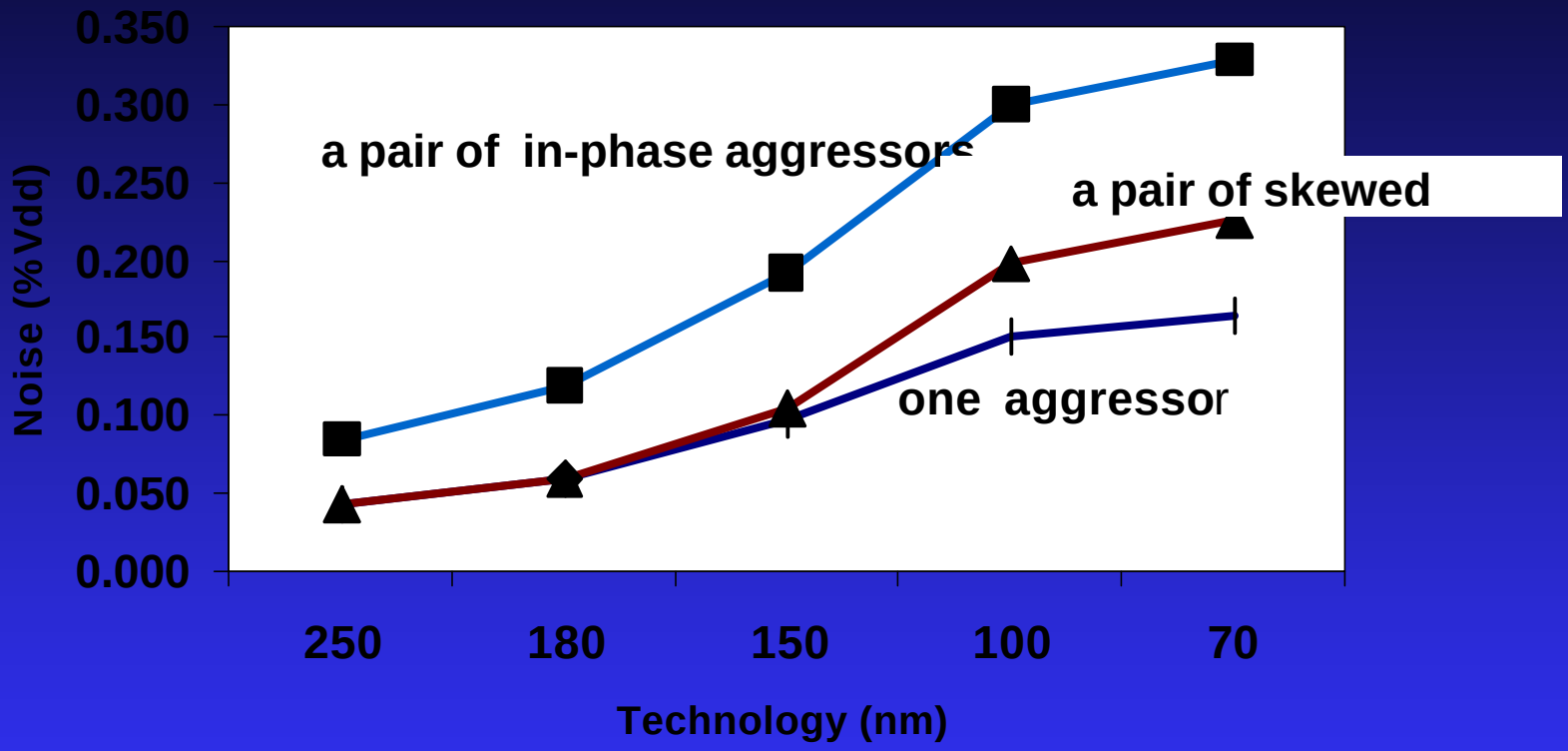


Delay Variations Due to Coupling Capacitance





Coupling Noise



Coupling noise from two adjacent aggressors to the middle victim wire with 2x min. spacing. Rise time is 10% of project clock period.

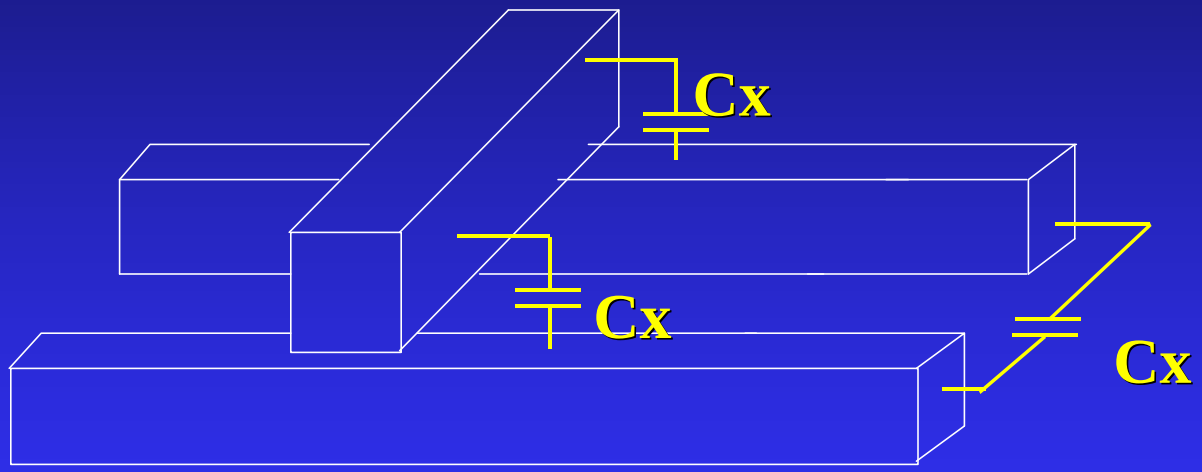
•Capacitive coupling depends strongly on both spatial and temporal relations!

Solution to Capacitance Computation

- Accurate solution to small structure
  - Numerical method based on Maxwell's equations
  - Raphael RC3, FastCap [Nabors-White, TCAD'91]
- Efficient solution to full chip
  - Using tables or empirical formulas
    - 2.5-D capacitance model [Cong-He-Kahng-et al,DAC'97]
  - Capacitance is **not** simply *A/d*
    - *A: area*
    - *d: distance*

Characteristics of Coupling Capacitance

- Coupling capacitance virtually exists only between adjacent wires or crossing wires



- Capacitance can be pre-computed for a set of (localized) interconnect structures
  - 2D or 2.5D capacitance model

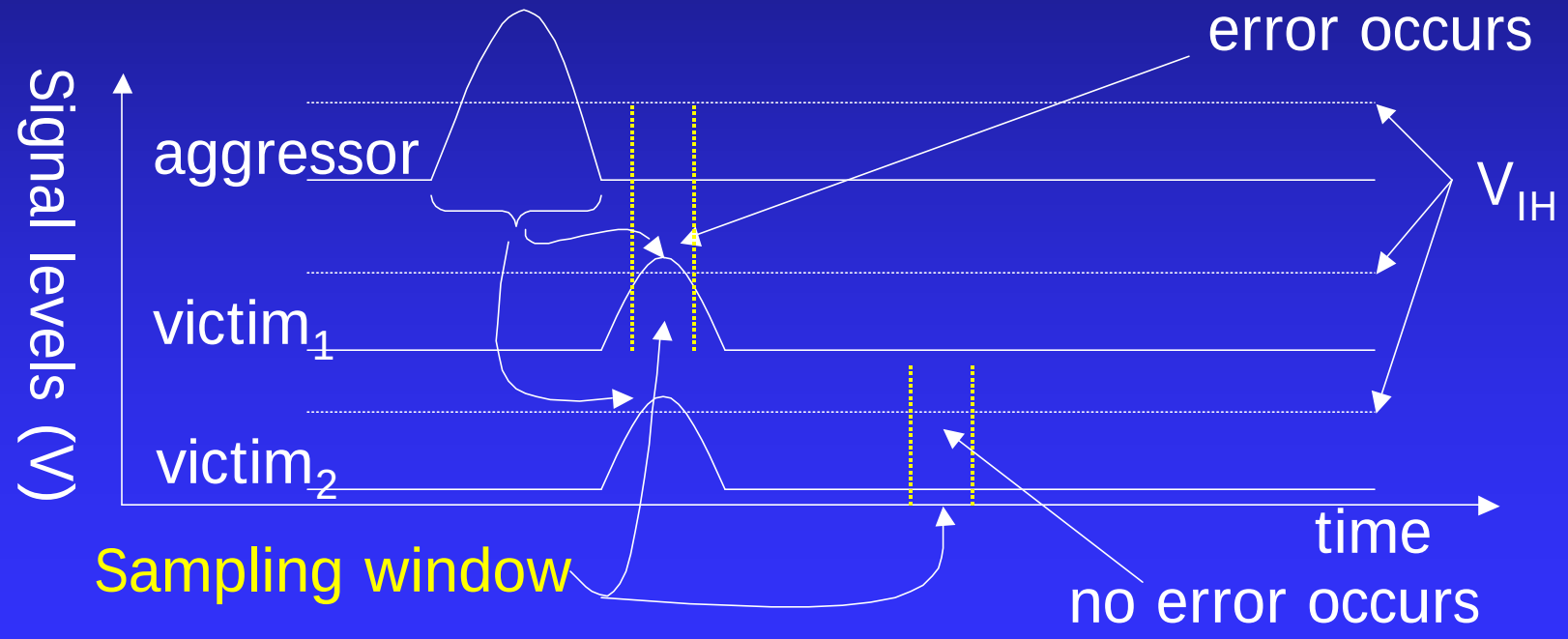
Layout to reduce impact of Cx

- Coplanar parallel interconnect structures with pre-routed Vdd and Gnd

- Noise avoidance technique:
  - Shield insertion
    - Shield is a wire directly connected to Vdd or Gnd

Timing Sensitivity

- Two nets are considered sensitive if a switching event on signal s_1 happens during a sample time window for s_2



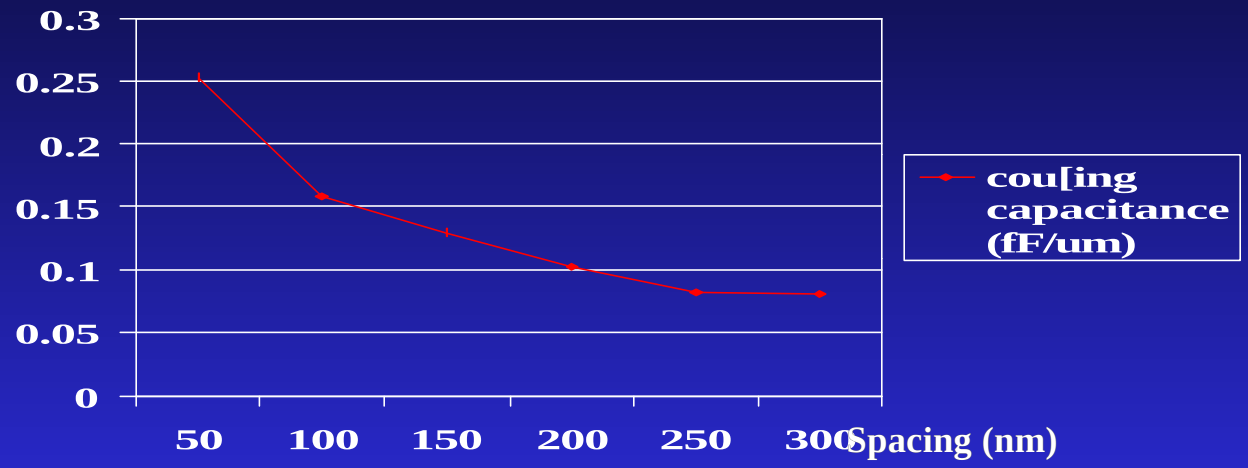
Layout to reduce impact of Cx

- Coplanar parallel interconnect structures with pre-routed Vdd and Gnd

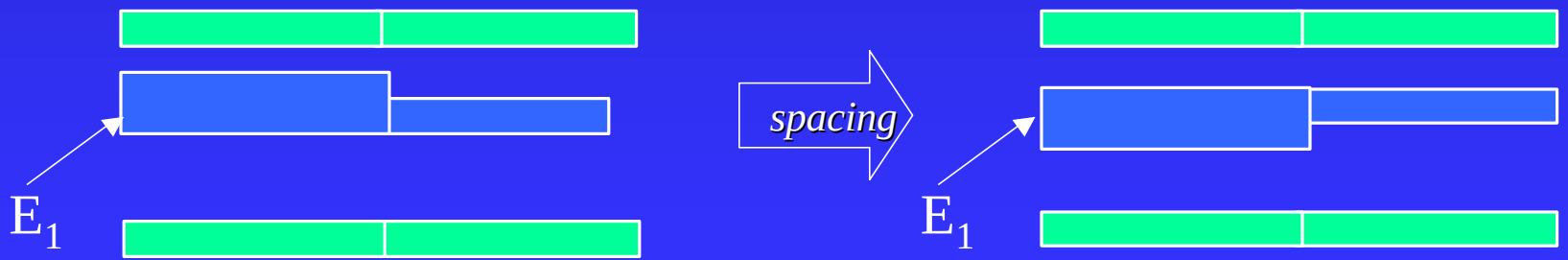
- Noise avoidance techniques:
  - Net ordering (track assignment / net placement)

Characteristics of Coupling Capacitance

- Coupling capacitance is highly sensitive to spacing

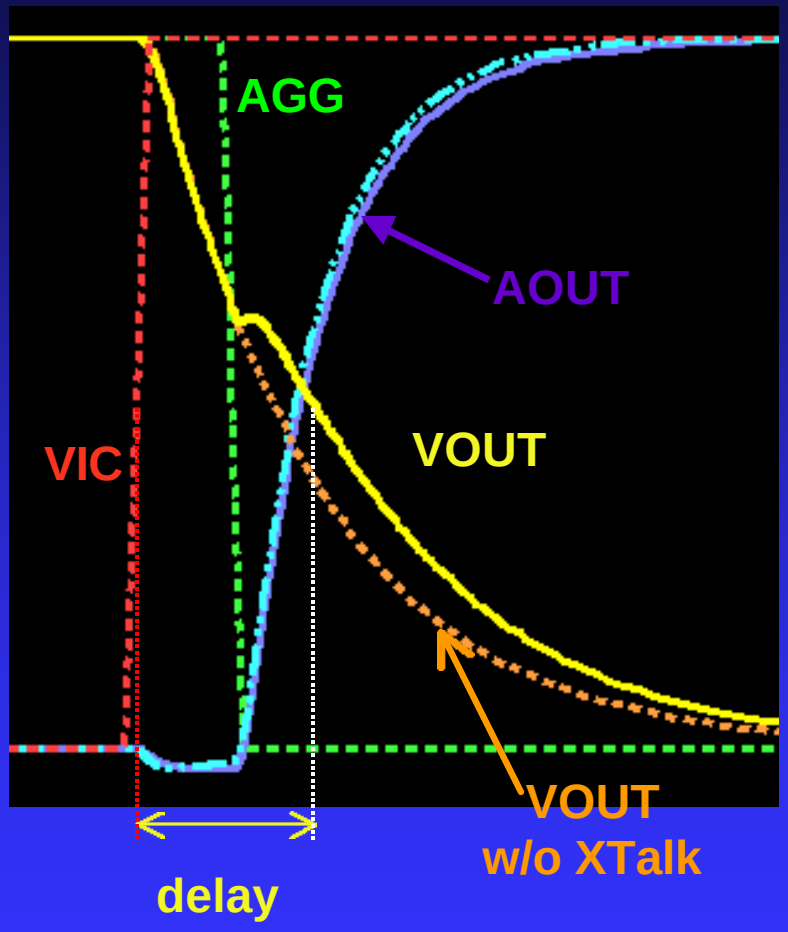


- Proper wire sizing and spacing may limit the impact of Cx by changing the ratio Cx/Ctotal



Relation between Delay and Noise

- T_max = T * ln (1/0.5-v) / ln 2
- T_min = T * ln (1/(o.5+v) / ln 2
- Typical values
  - V T_max/T T_min/T
  - 0.1 1.32 0.74
  - 0.15 1.51 0.62
  - 0.20 1.75 0.52



Noise estimation and filtering

- Rule of thumb:
  - Cx/C < threshold
- Devgan, ICCAD'97
  - V < (Rv + Rint / 2) * Cx / (1.25 Tr)
  - Tr: rising time for the aggressor
- Vittal et al, TCAD'99 (more accurate)
  - V = (Rv + Rint / 2) * Cx / {0.63Tr + Ra (Ca + Cx) + Rv (Cv + Cx) + Rint * Cx}

- To reduce Cx impact
  - Increase the driver size of victim
  - Decrease the driver size of aggressor
  - Or buffering
  - Need a global device size solution coupled with Time Analysis

Mini-Summary

- Capacitive crosstalk is localized
- Capacitive crosstalk affects both delay and signal integrity
- Capacitive crosstalk can be minimized by
  - Spacing (and wire sizing)
  - Device sizing
  - Net ordering
  - Shielding
  - Buffering

Outline

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- Inductive noise and layout optimization
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- Example: SINO algorithm for both Cx and Lx noise

Is RC Model still Sufficient?

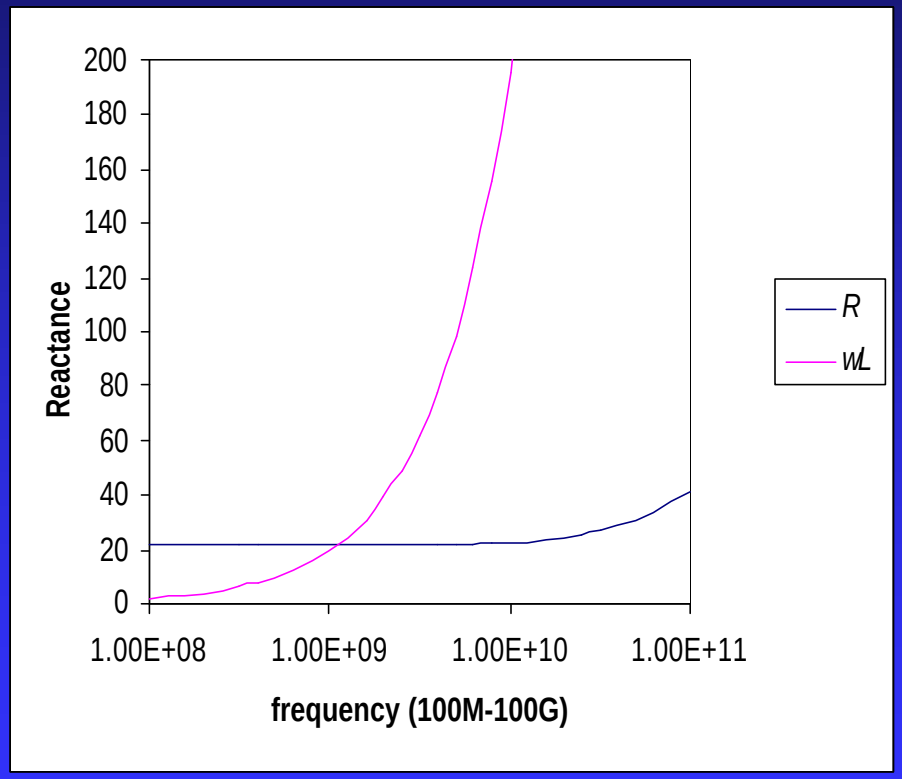
- Interconnect impedance is more than resistance
  - Z μ R +jwL
  - w μ $1/t_r$
- On-chip inductance should be considered
  - When wL becomes comparable to R as we move towards Ghz+ designs

Candidates for On-Chip Inductance

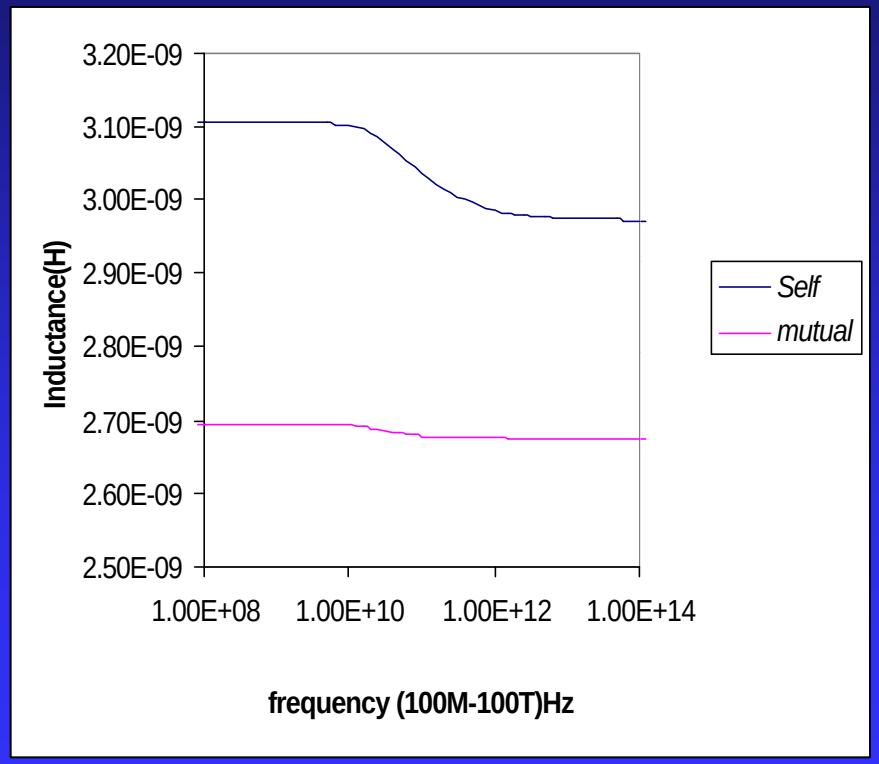
- Wide clock trees
  - Skews are different under RLC and RC models
  - Neighboring signals are disturbed due to large clock *di/dt* noise
- Fast edge rate (~100ps) buses
  - RC model under-estimates crosstalk
- P/G grids (and C4 bumps)
  - *di/dt* noise might overweight IR drop

Resistance vs Inductance

Length = 2000, Width = 0.8
Thickness = 2.0, Space = 0.8

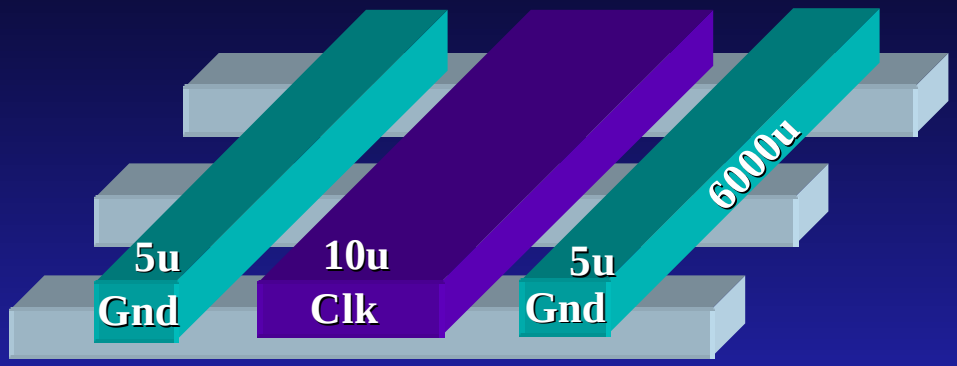


R and wL for a single wire

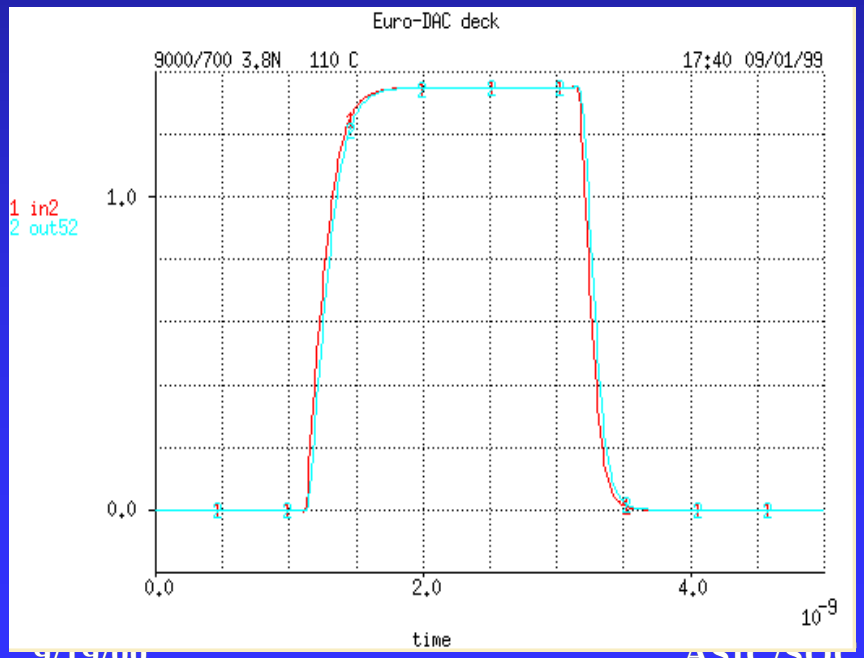


Ls and Lx for two parallel wires

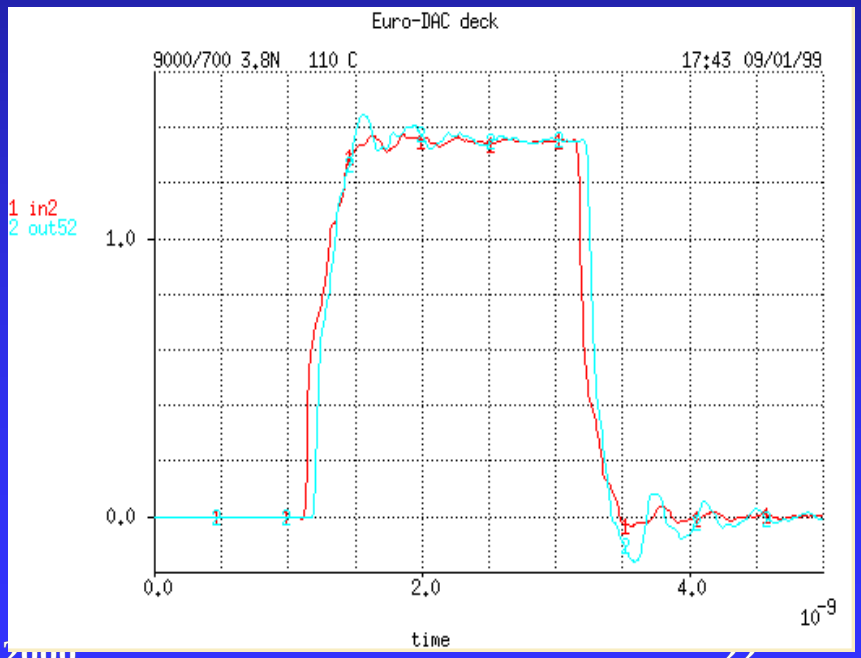
Impact of Inductance



RC model



RLC model



Inductance Extraction from Geometries

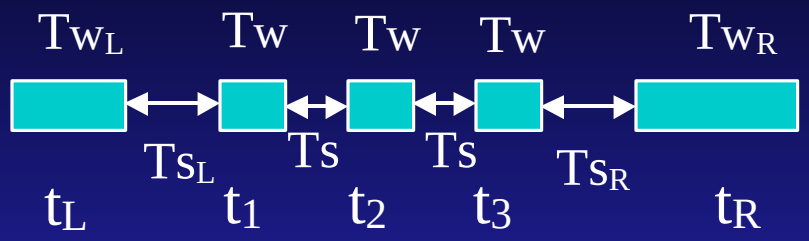
- Numerical method based on Maxwell's equations
  - Accurate, but way too slow for iterative physical design and verification
- Efficient yet accurate models
  - Coplanar bus structure [He-Chang-Shen-et al, CICC'99]
  - Strip-lines and micro-strip bus lines [Chang-Shen-He-et al, DATE'2K]
  - Used in HP for state-of-the-art CPU design

Definition of Loop Inductance

- The loop inductance is

$$L_{ij} = \frac{m}{4p} \bullet \frac{1}{a_i a_j} \bullet \frac{1}{I_i I_j} \oint_{loop_i} \int_{a_i} \oint_{loop_j} \int_{a_j} \frac{1}{r_{ij}} dI_i dI_j da_i da_j$$

Loop Inductance for N Traces

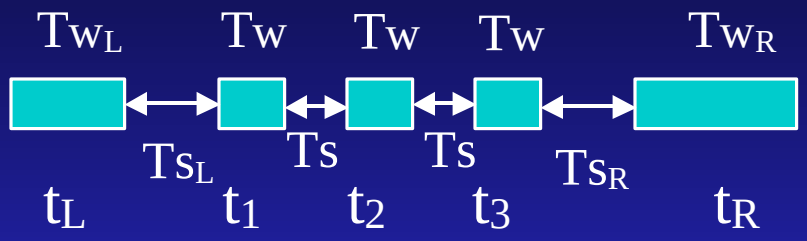


1.73	1.15	0.53
1.15	1.94	1.24
0.53	1.24	1.92

- Assume edge traces are AC-grounded
  - leads to 3x3 loop inductance matrix
- Inductance has a long range effect
  - non-negligible coupling between t_1 and t_3, even with t_2 between them

It is not sufficient to consider only a single net, as did by most interconnect modeling and optimization works

Table in Brute-Force Way is Expensive



1.73	1.15	0.53
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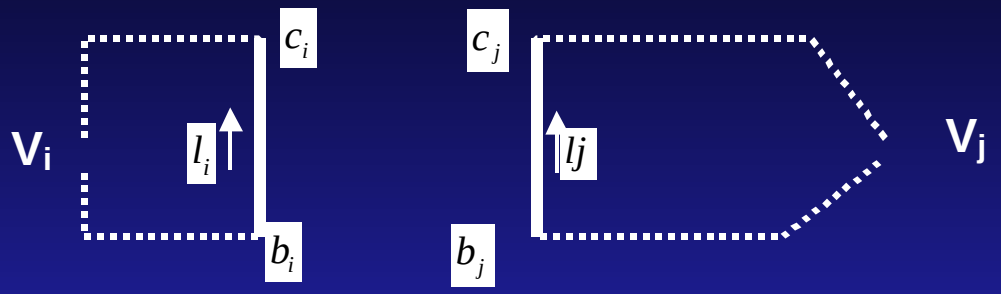
0.53	1.24	1.92

- Self inductance has nine dimensions:
  - (n, length, location,Tw_L,Ts_L,Tw,Ts,Tw_R,Ts_R)
- Mutual inductance has ten dimensions:
  - (n, length, location1, location2,Tw_L,Ts_L,Tw,Ts,Tw_R,Ts_R)
- Length is needed because inductance is not linearly scalable

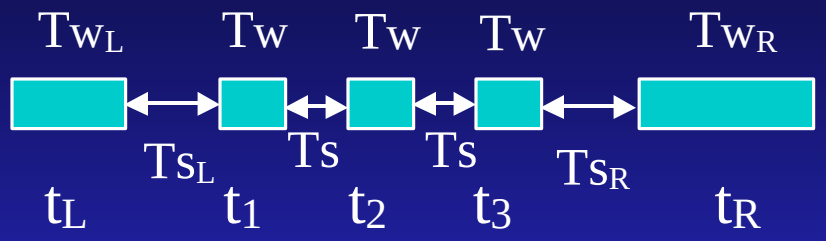
Definition of Partial Inductance



- Partial inductance is the portion of loop inductance for a segment when its current returns via the infinity
  - called partial element equivalent circuit (PEEC) model
- If current is uniform (no skin effect), the partial inductance is

$$L_{ij} = \frac{m}{4p} \bullet \frac{1}{a_i a_j} \bullet \int_{b_i}^{c_i} \int_{a_i}^{} \int_{b_j}^{c_j} \int_{a_j}^{} \frac{dl_i dl_j}{r_{ij}} da_i da_j$$

Partial Inductance for N Traces

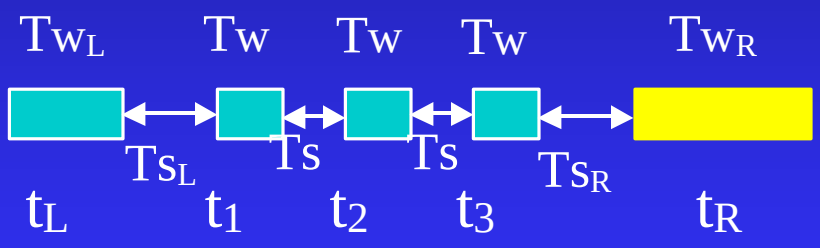


6.17	5.43	5.12	4.89	4.66
5.43	6.79	6.10	5.48	5.04
5.12	6.10	6.79	6.10	5.33
4.89	5.48	6.10	6.79	5.77
4.66	5.04	5.33	5.77	6.50

- Treat edge traces same as inner traces
  - lead to 5x5 partial inductance table
- Partial inductance model is more accurate compared to loop inductance model
  - Without pre-setting current return loop

Foundation I

The self inductance under the PEEC model for a trace depends only on the trace itself (w/ skin effect for a given frequency).



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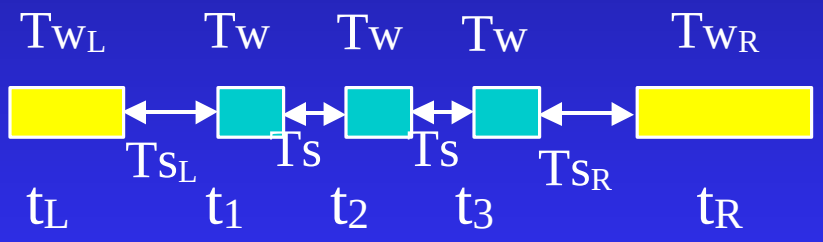
4.89	5.48	6.10	6.79	5.77
4.66	5.04	5.33	5.77	6.50

6.50

Foundation II

The mutual inductance under the PEEC model for two traces depends only on the traces themselves (w/ skin effect for given frequency).



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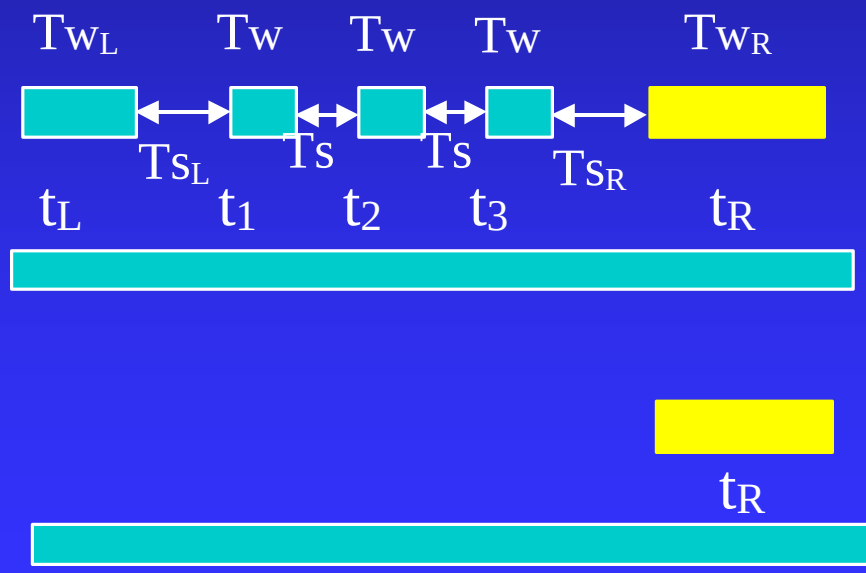
5.43	6.79	6.10	5.48	5.04
5.12	6.10	6.79	6.10	5.33
4.89	5.48	6.10	6.79	5.77
4.66	5.04	5.33	5.77	6.50

6.17	4.66
4.66	6.50

Foundation III

The self loop inductance for a trace on top of a ground plane depends only on the trace itself (its length, width, and thickness)

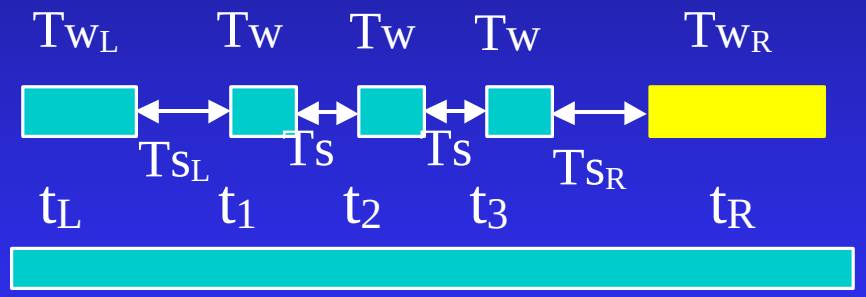


4.8	2.5	1.3	0.7	0.14
2.5	5.5	2.9	1.5	0.7
1.3	2.9	5.7	2.9	1.3
0.7	1.5	2.9	2.5	2.5
0.14	0.7	1.3	2.5	4.8

4.8

Foundation IV

The mutual loop inductance for two traces on top of a ground plane depends only on the two traces themselves (their lengths, widths, and thickness)



4.8	2.5	1.3	0.7	0.14
2.5	5.5	2.9	1.5	0.7
1.3	2.9	5.7	2.9	1.3
0.7	1.5	2.9	2.5	2.5
0.14	0.7	1.3	2.5	4.8

4.8	0.14
0.14	4.8

Validation and Implication of Foundations

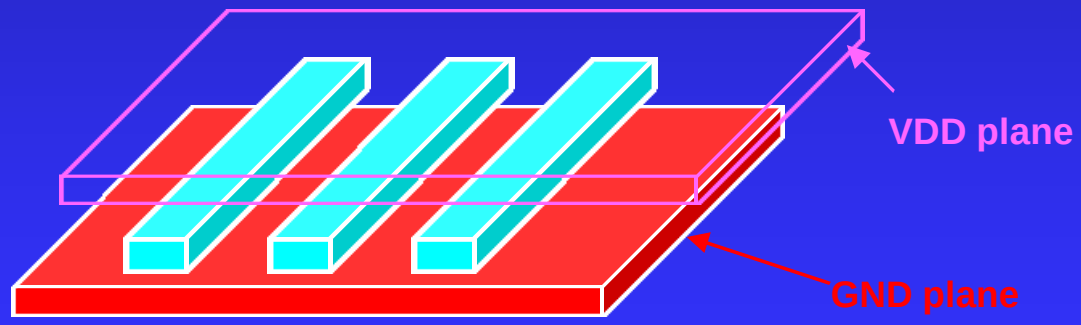
- Foundations I and II can be validated theoretically
- Foundations III and IV were verified experimentally
- Problem size of inductance extraction can be greatly reduced w/o loss of accuracy
  - Solve 1-trace problem for self inductance
    - Reduce 9-D table to 2-D table
  - Solve 2-trace problem for mutual inductance
    - Reduce 10-D table to 3-D table

More Recent Results

- Extension from parallel bus to random nets
  - Arbitrary locations, lengths, thickness, and etc.
  - Typically within 3% of numerical computation
  - Developed as a web-based tool
    - http://eda.ece.wisc.edu/WebHenry

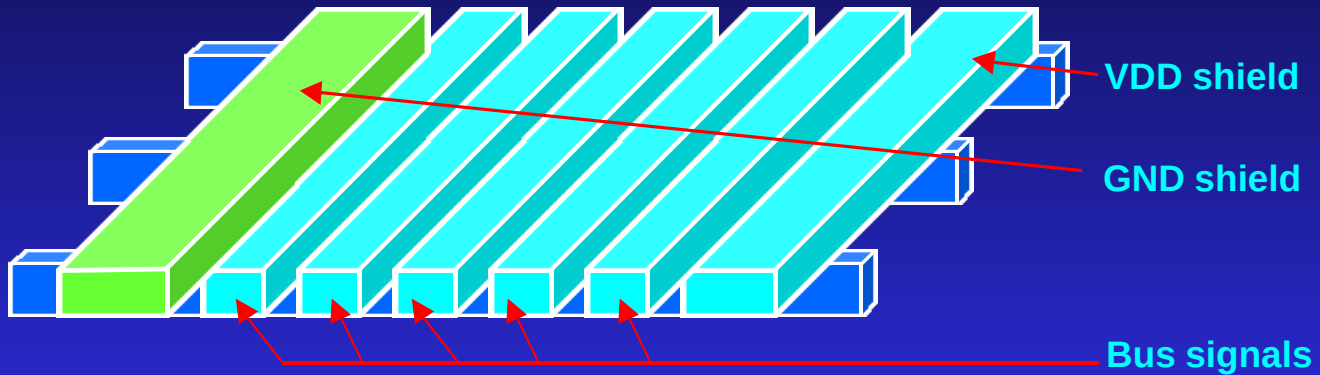
Inductance Minimization

- Reference plane
  - wiring layers sandwiched between power planes



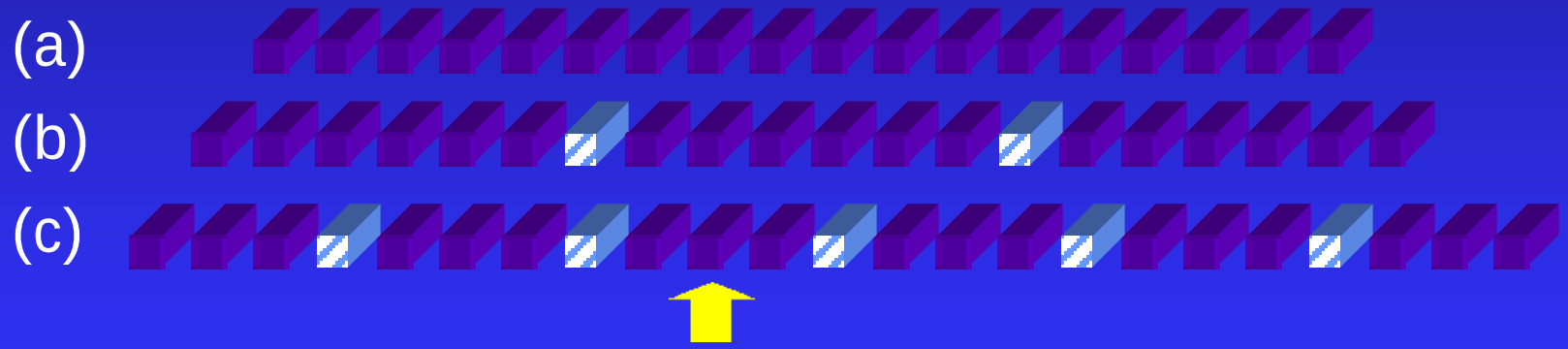
Inductance Minimization

- Coplanar shields



Characteristics of Coupling in 18-Bit Bus

# of Shields	Noise (% of Vdd)
0 (a)	0.71V (55%)
2 (b)	0.38V (29%)
5 (c)	0.17V (13%)



- Lx coupling between non-adjacent nets is non-trivial
- Shielding is effective to reduce Lx coupling

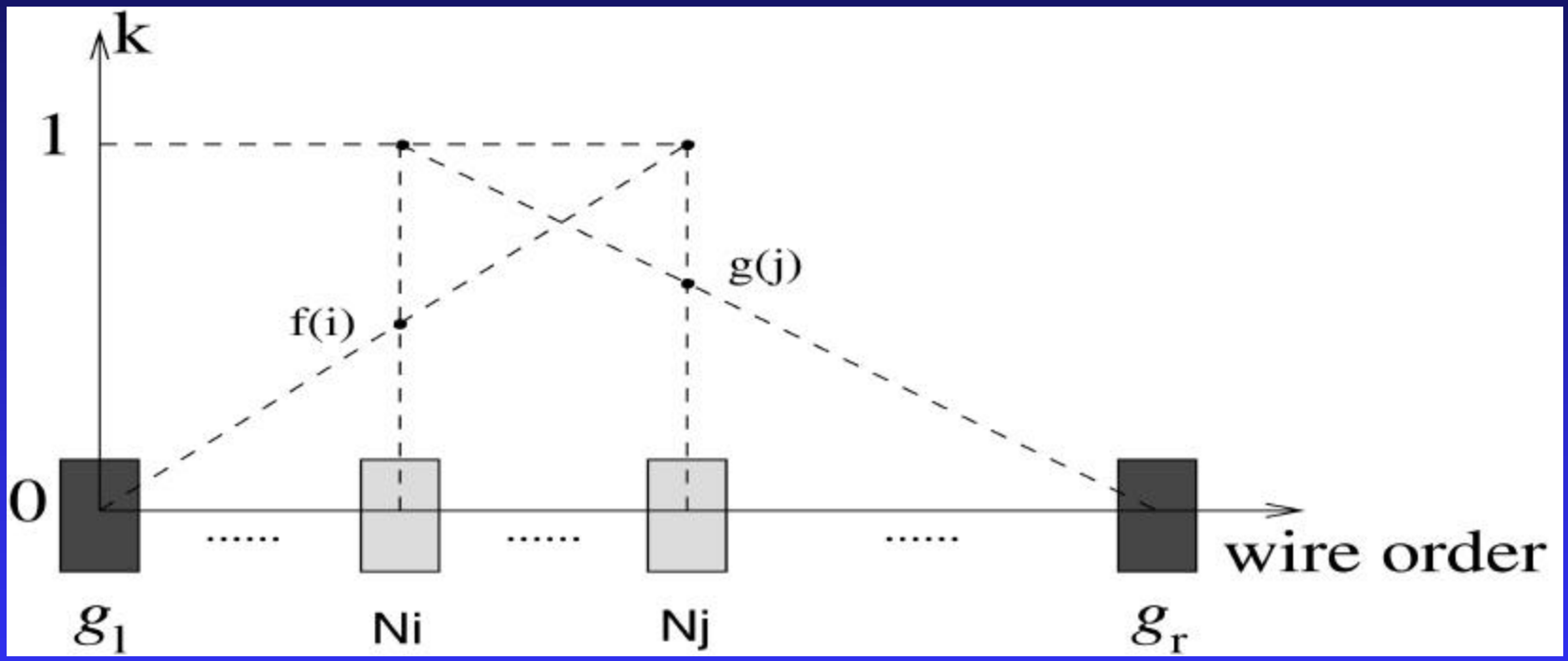
Figure of Merit of Inductive Coupling

- Inductive coupling coefficient defined as

$$K = Lij / \sqrt{L_i \bullet L_j}$$

- A formula-based Keff model has been developed
  - High fidelity between formula and noise voltage [He-Xu, 2000]

Illustration of K_{eff} Computation
[XuHe,2000]

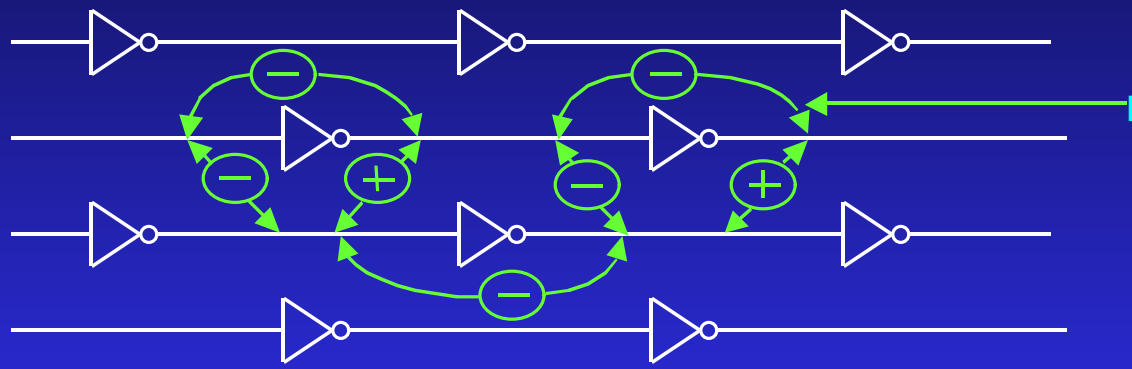


$$K_{eff}(i,j) = (f(i) + g(j)) / 2$$

$$f(i) = (N_i - g_l)/(N_j - g_l);\ g(j) = (g_r - N_j)/(g_r - N_i)$$

Inductance Minimization

- Staggered inverters/buffers



- Differential signals
  - Nets with opposite switching signals can be placed adjacent to each other
    - Decrease Lx noise at the cost of a higher Cx noise

Mini-Summary

- Inductive crosstalk is globalized
- Inductive crosstalk affects both delay and signal integrity
- Inductive crosstalk is not sensitive to
  - Spacing (and wire sizing)
  - Net ordering
- Inductive crosstalk can be minimized by
  - Shielding
  - Buffering
  - Ground plane
  - Differential signal
  - Signal termination

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  - Layout optimization
- Inductive noise and layout optimization
  - When inductance become important
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- Example: SINO algorithm for both Cx and Lx noise

SINO Problem [He-Lepak, ISPD2K]: Simultaneous Shield Insertion and Net Ordering

- Coplanar parallel interconnect structures with pre-routed Vdd and Gnd

- Noise avoidance techniques:
  - Net ordering (track assignment / net placement)
  - Shield insertion
    - Shield is a wire directly connected to Vdd or Gnd

SINO/NF Problem

- Given: An initial placement P
- Find: A new placement P' via simultaneous shield insertion and net ordering such that:
  - P' is capacitive noise free
    - Sensitive nets are not adjacent to each other
  - P' is inductive noise free
    - Sensitive nets do not share a block
  - P' has minimal area
- Equivalent to one-shield-one-signal
  - When all nets are sensitive to one another

SINO/NB Problem

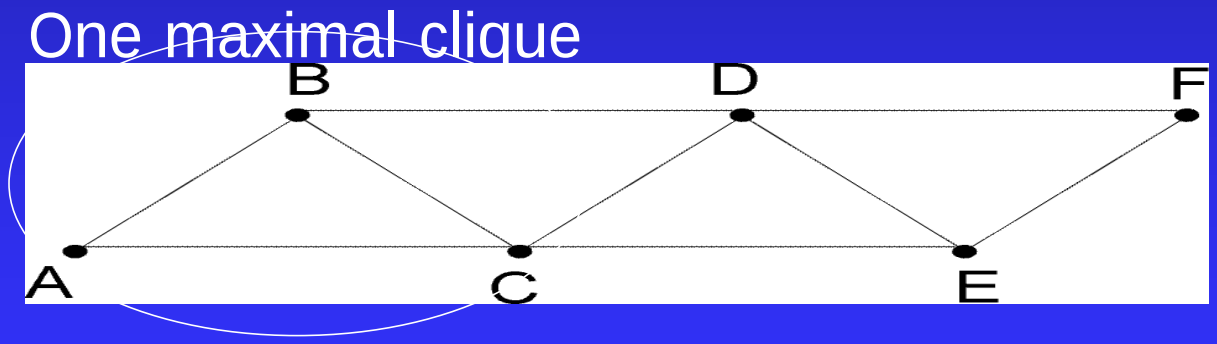
- **Given: An initial placement P**
- **Find: A new placement P' via simultaneous shield insertion and net ordering such that:**
  - **P' is capacitive noise free**
  - *All nets in P' have inductive noise less than a given value*
  - **P' has minimal area**

Properties of SINO Problems

- Theorem: The optimal SINO/NF problem is NP-hard
- Theorem: The optimal SINO/NB problem is NP-hard
- Theorem: The maximum clique in the sensitivity graph is a lower bound on the number of blocks required for all SINO/NF solutions

Sensitivity Graph for SINO Problem

- Graph indicating which nets are sensitive to one-another (vertices=nets, edges=nets are sensitive)



Sensitivity graph with clique size = 3

Greedy Shield Insertion

- Shield Insertion (SI)
  - Insert shield when a Cx or Lx violation occurs
  - Results depend strongly on the initial placement
- Net Ordering + Shield Insertion (NO+SI)
  - First remove Cx coupling by net ordering, then perform shield insertion for Lx
  - Results depend weakly on the initial placement

Separated NO+SI—simultaneous algorithm works better

Graph Coloring SINO (GC)

- Our implementation: Greedy-based GC
- Can solve with other GC methods as well
- Main contributions of SINO-GC:
  - Provide lower bound measurements for SINO/NF
  - Comparative reference point

Simulated Annealing SINO (SA)

- Cost Function is a weighted sum of:
  - Number of Cx violations
  - Number of Lx violations
  - Inductance Violation Figure (quantizes level of inductive noise)
  - Area of Placement
- Random Moves
  - Combine two random blocks in placement P
  - Swap two (arbitrary) random s-wires in P
  - Move a single random s-wire in P
  - Insert a shield wire at a random location in P

Quality of SINO/NB Solutions

	SINO/NF	SINO/NB			
K_{thresh}	Graph Coloring	Greedy SI	NO+SI	GC	SA
Net Sensitivity Rate: 10%					
1.0	3.2 (2.0)	5.0	2.8	2.0	1.8
2.0		4.2	1.2	2.0	1.0
Net Sensitivity Rate: 30%					
1.0	6.0 (3.8)	13.2	4.4	4.2	3.0
2.0		13.2	2.8	3.8	2.0
Net Sensitivity Rate: 60%					
1.0	13.6 (8.2)	22.4	5.4	8.2	5.0
2.0		22.4	4.0	8.2	3.4

Max. clique size in the sensitivity graph

# of shields is fewer than lower bound for SINO/NF

CPU time is much less than existing net ordering algorithms

Mini-Summary

- SINO is effective to achieve signal integrity
- Ongoing work:
  - Post-routing (GR) optimization for signal integrity
    - Considering net ordering, shielding, differential signals, staggered inverters, and etc.
  - Progress can be found at http://eda.ece.wisc.edu