Chip and Package Power Supply Noise Analysis for SoC Design

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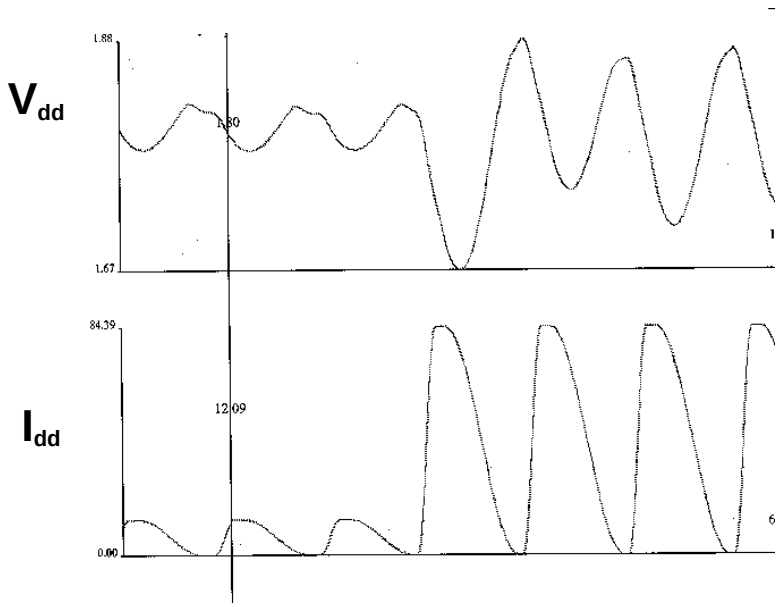
International Technology Roadmap for Semiconductors

Year	Gate Length (nm)	Chip Frequency (GHz)	Maximum Power (Watt)	Supply Voltage (Volt)
2001	65	1.7	130	1.1
2002	53	2.3	140	1.0
2003	45	3.1	150	1.0
2004	37	4.0	160	1.0
2005	32	5.2	170	0.9
2006	28	5.6	180	0.9
2007	25	6.7	190	0.7
2010	18	11.5	218	0.6
2013	13	19.3	251	0.5
2016	9	28.8	288	0.4

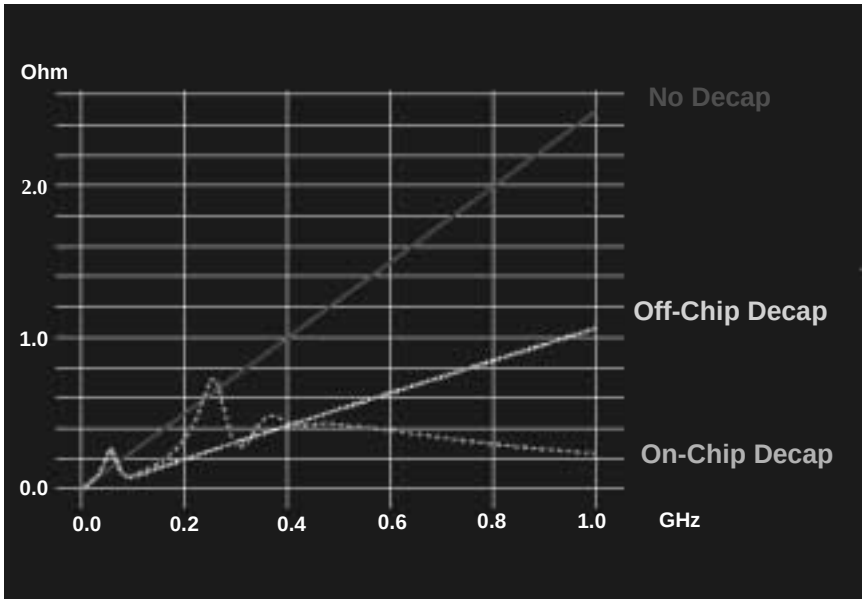
Power Supply Noise $\Delta V = IR + L\ \Delta I / \Delta t$



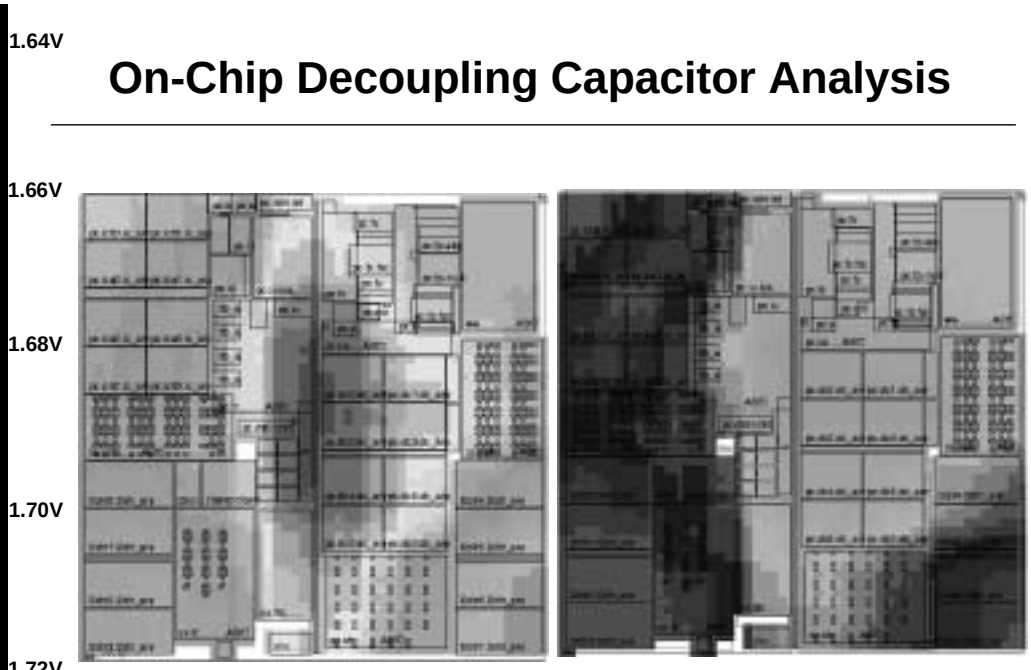
Power Supply Noise Issues

- How much is total Vdd drop?
- How much is on-chip IR drop?
- How much is off-chip L dI/dt drop?
- What is the on-chip Vdd distribution?
- Where are the hot spots?
- Which design parameters can be changed to minimize the noise?
- Do we need on-chip decoupling capacitors?
- How much decoupling capacitance is needed?
- Where should the decoupling capacitors be placed?

Package Impedance Frequency Response



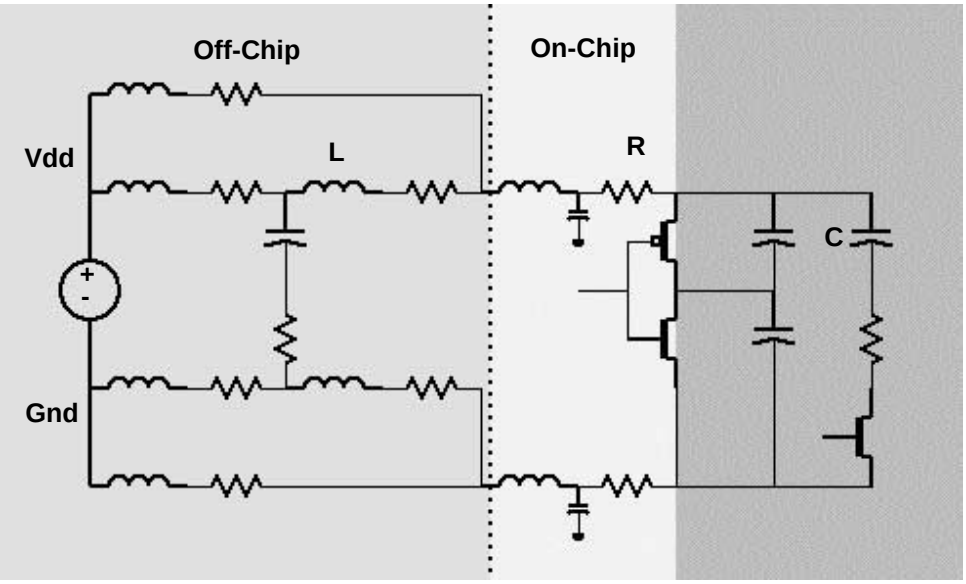
On-Chip Decoupling Capacitor Analysis



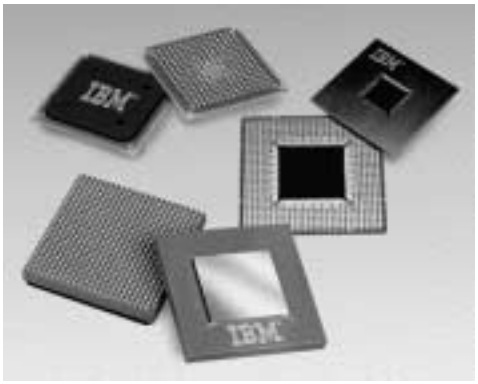
Without On-Chip Decap
(1.640V - 1.700V)

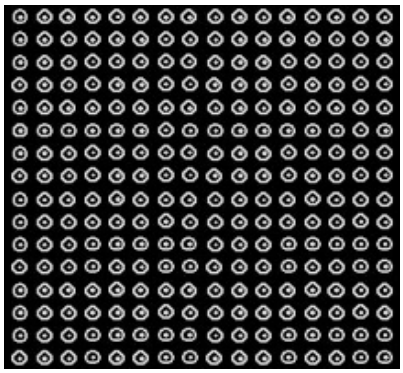
With On-Chip Decap
(1.680V - 1.726V)

Power Supply Distribution Model

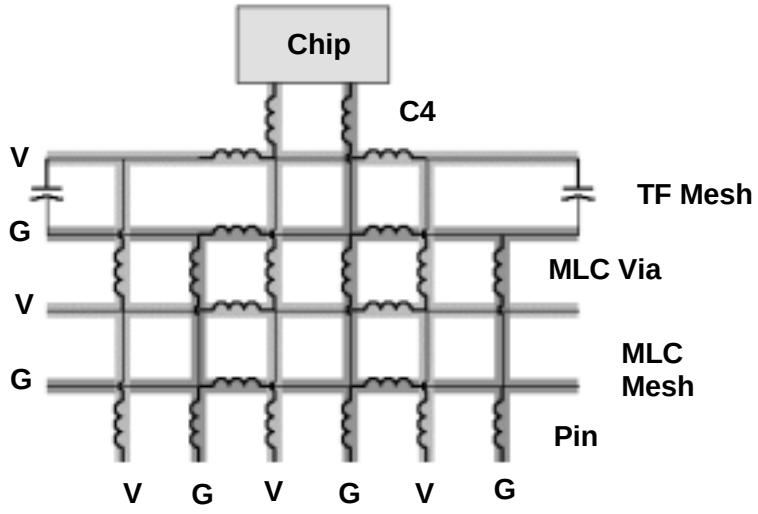


Package Model Partition

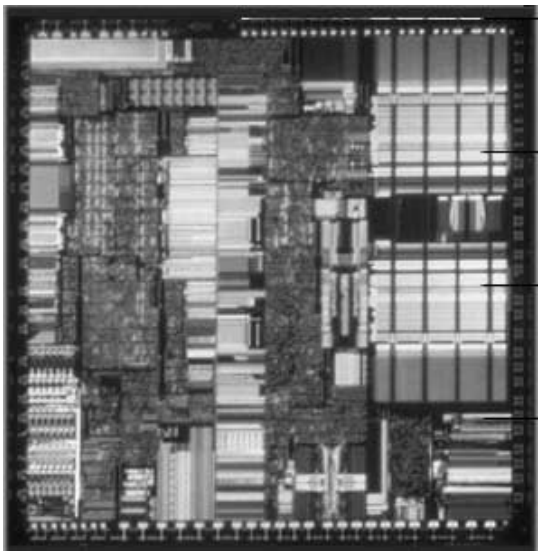




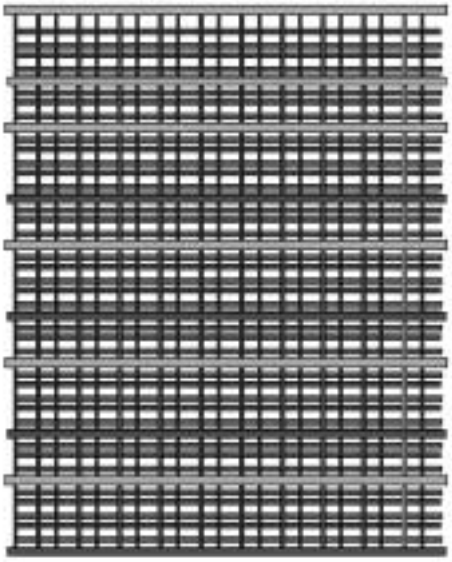
Package Model Cross Section

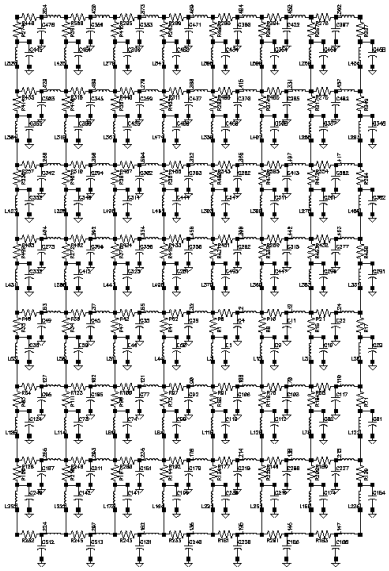


Chip Model Partition

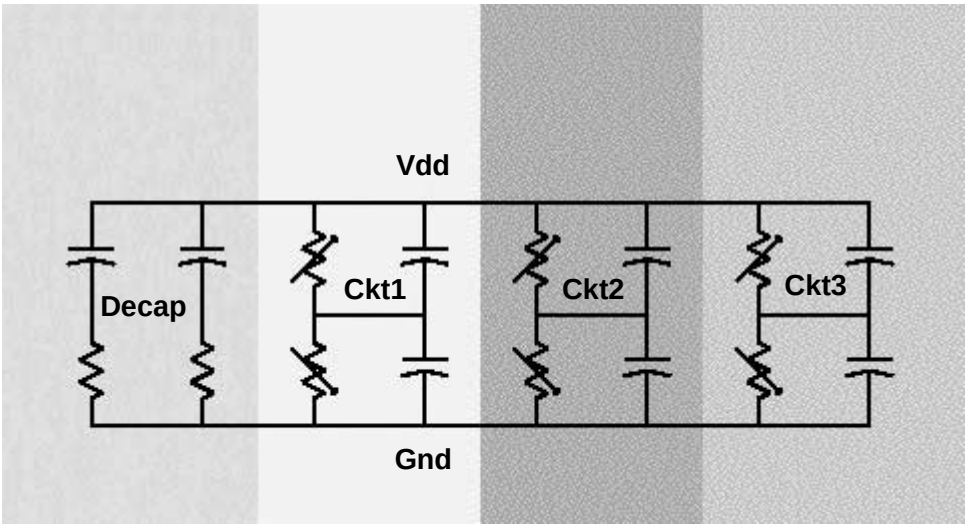


On-Chip Power Bus Structure





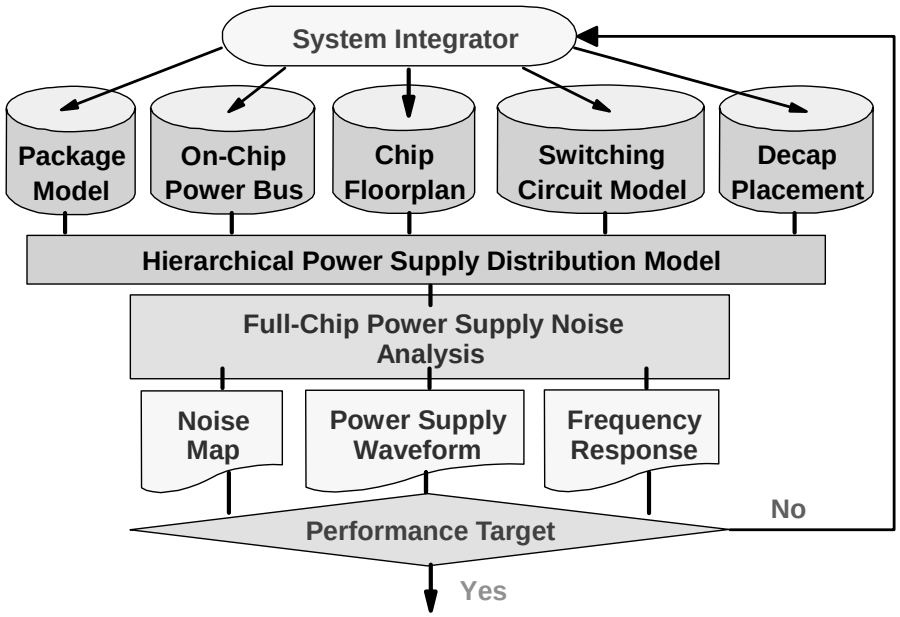
Equivalent Switching Circuit



On-Chip Decoupling Capacitors

- Built-in decoupling capacitors
  - N-well capacitor
  - Non-switching circuit capacitor
- Added decoupling capacitors
  - Thin-oxide capacitor
  - Trench capacitor

Integrated Model and Design Flow



Dual-Chip Power Supply Noise Analysis

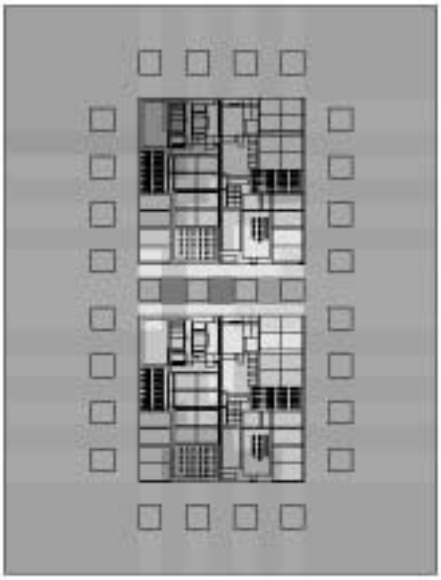
1.66V

1.73V

1.80V

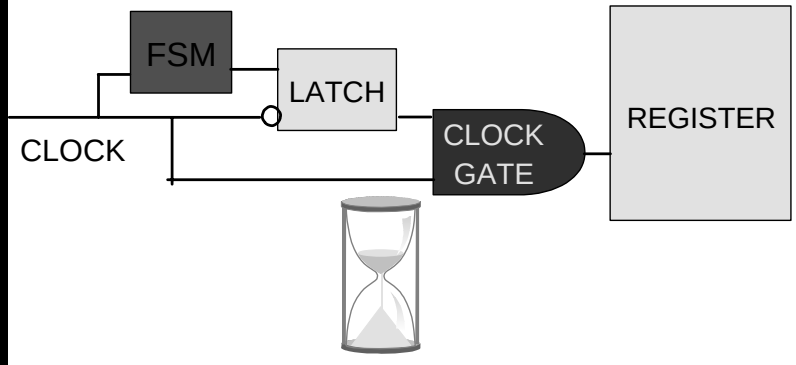
1.87V

1.94V



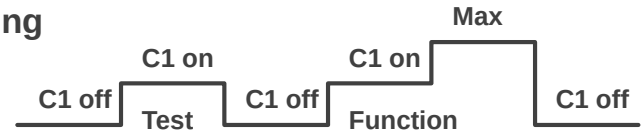
Clock Gating and Its Effect on Transient Power Supply Noise

- A Potential Show Stopper

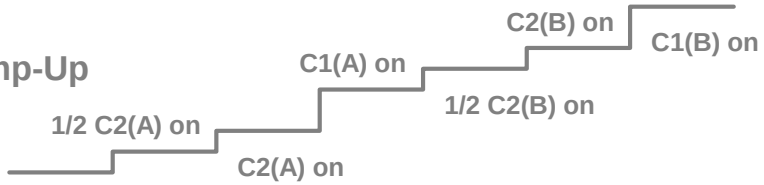


Transient Noise Analysis

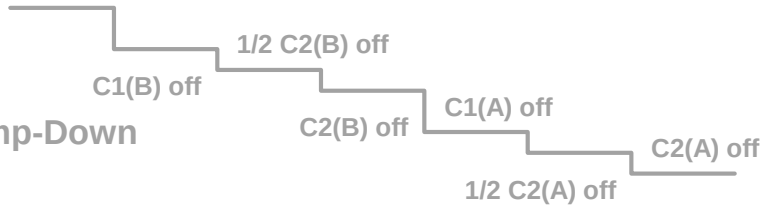
Clock Gating



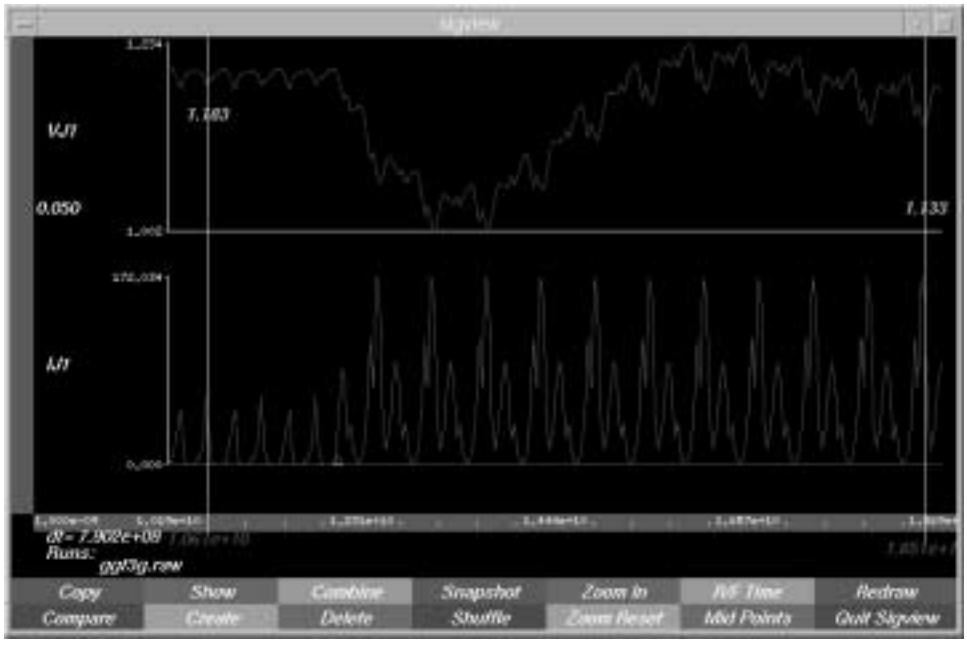
Power Ramp-Up



Power Ramp-Down



Hold-to-Maxave Transient Vdd



Bulk-CMOS and SOI Noise Analysis

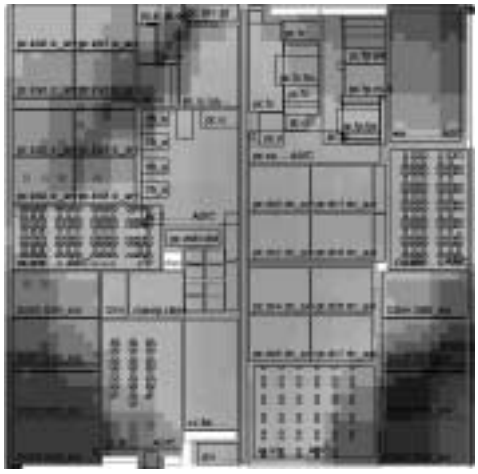
1.68V

1.70V

1.72V

1.74V

1.76V



With N-Well (Bulk)
(1.718V - 1.767V)

Without N-Well (SOI)
(1.680V - 1.726V)

C4 Current and Electromigration Analysis

100mA

75mA

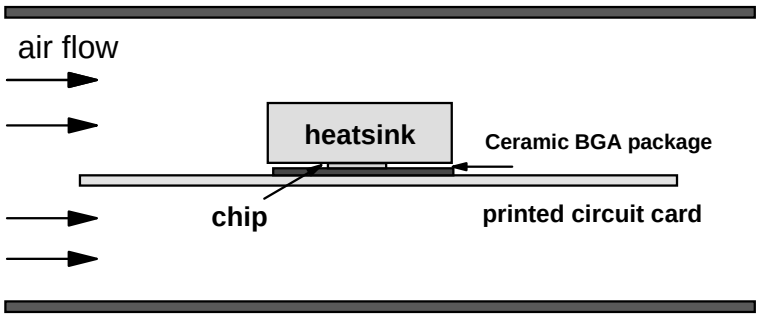
50mA

25mA

0mA

On-Chip Temperature Gradient Analysis

- Based on thermal fluid dynamics model.
- Use on-chip power distribution as boundary condition.
- 3°C for a 25W chip with uniform power distribution.
- 12°C for a 25W chip with nonuniform power distribution.



Power Supply Noise Analysis Summary

- Build chip and package power distribution model.
- Simulate switching activities and calculate thermal power.
- Control steady-state noise under 10% of nominal Vdd.
- Model circuit transitions from idle power to peak power and evaluate their noise impact.
- Analyze transient noise due to clock gating, power ramp-up, and switching near resonant frequency.
- Optimize on-chip decoupling capacitor placement to minimize power supply noise.
- Balance thin-oxide and thick-oxide decap usage to reduce tunneling current, leakage power, and burn-in cost.