Clocktree RLC Extraction with Efficient Inductance Modeling

Norman Chang, Shen Lin, Lei He*, O. Sam Nakagawa, and Weize Xie
Hewlett-Packard Laboratories, Palo Alto, CA 94303, USA
*ECE Dept., University of Wisconsin, Madison, WI 53706, USA

Abstract

In this paper, we present an efficient yet accurate inductance extraction methodology and also apply it to clocktree RLC extraction. We first show that without loss of accuracy, the inductance extraction problem of n traces with or without ground planes can be reduced to a number of one-trace and two-trace subproblems. We then solve one-trace and two-trace subproblems via a table-based approach. We finally validate the linear cascading assumption that enables us to apply our inductance extraction approach to clocktree RLC extraction and optimization.

I. Introduction

Due to faster clock frequencies, shorter rise times, and metal of lower resistivity (i.e. Cu), inductance effects of on-chip interconnects can no longer be ignored [1-2]. In particular, the inductance extraction is much needed for the clocktree modeling and simulation for high-frequency CPU designs [3]. This is due to the common design techniques of using much wider wires (can be sometimes more than 10um in width) in clocktree routing to carry strong and fast-switching clock signals. The inductance effect in clocktree is worsen due to the fact that large driver and therefore smaller source impedance is used to drive the clocktree. To illustrate the importance of including inductance in the clocktree simulation, we simulate a simple yet realistic configuration in Figure 1 without and with the inductance. The delays from the output of the clock buffer to the sink node are 28.01ps and 47.6ps respectively without and with the consideration of inductance. The waveforms are displayed in Figure 2 and Figure 3. We can see that inductance effect is significant and needs to be considered to better estimate the skew in high-speed clocktrees.

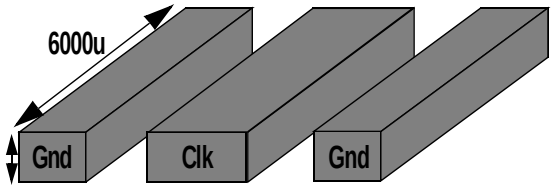

Figure 1:A co-planar waveguide clock net structure with wires of 6000um long, 2um thick, 10um wide for the clock signal, and 5um wide for the Gnd wires. The spacing between adjacent wires is 1um. The clock buffer has about 40ohm driving resistance. An orthogonal signal layer is assumed to be below.

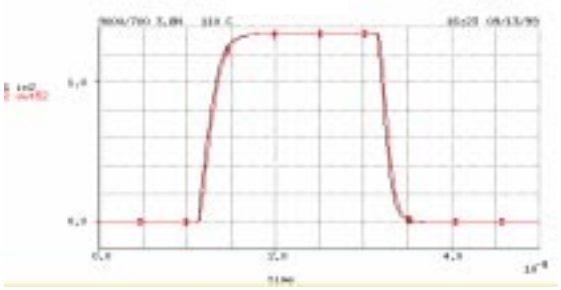

Figure 2:Waveforms at the output of the clock buffer and at the sink without inductance, i.e. RC netlist only.

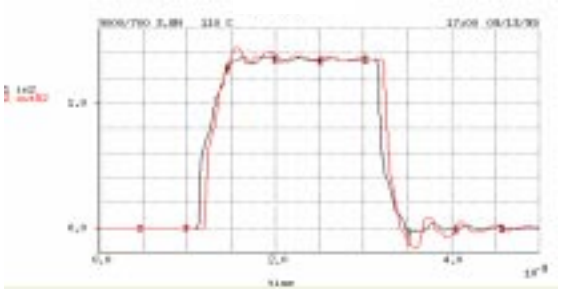

Figure 3:Waveforms at the output of the clock buffer and at the sink with inductance. The delay impact of overshoot and undershoot due to inductance may be observed.

A table based approach for on-chip inductance extraction combined with a fast generation of statistically-based RC models have been described in [4-5]. However, no ground planes were considered there. In this paper, we extend the approach described in [5] to model efficiently microstrip and stripline configurations often encountered in a clocktree design. We also experimentally validate an RLC-segment-based linearly cascaded method, which enables us to apply our inductance extraction approach to clocktrees.

The paper is organized as follows: In Section II, we review and extend the two basic foundations described in [5] which allow us to reduce the problem size of inductance extraction without loss of accuracy. In Section III, we propose a table-based inductance extraction methodology based on the two extended foundations. Linearly cascaded method is described in Section IV. In Section V, we apply this efficient inductance modeling method to clocktree RLC extraction. Section VI concludes this paper.

II. **Foundations for Inductance Extraction**

A. Foundations for Partial Inductance in Co-planar Traces

There are multiple metal layers in a VLSI technology. We assume that wire traces in adjacent layers are orthogonal, and extract the inductance for a *block*, which contains *n* traces (T1, T2,..., Tn) of same lengths in the same layer N (see Figure 4). In addition, we also assume that the two outside traces, T1 and Tn, are dedicated AC grounded traces. When the block size is three, it is a coplanar-waveguide, which is one of the three basic forms for transmission line, and is often used for clock tree in high-speed designs. When the block size is large, it models the bus structure with outside ground traces that can be used for shielding or for both shielding and power supply at the same time. Because traces are orthogonal in adjacent layers, traces in layer N+1 and layer N-1 will not affect the inductance of traces in the current layer N [7]. However, there may be parallel traces or ground planes in layer N+2 and/or layer N-2 which can affect the inductance in layer N. We consider wide ground traces which can be treated as a local ground plane in layer N+2 and/or N-2.

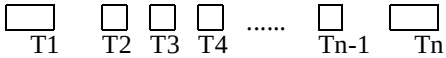

Figure 4:The cross-section view for a block of n traces, where T1 and Tn are dedicated AC grounded traces.

Note that the capacitive coupling is a *short-range* effect in the sense that for a block, only the mutual capacitance between adjacent traces are important while the rest of the mutual capacitance may be ignored. Therefore, for any trace, it is sufficient to solve the trace and its two adjacent traces via numerical extraction. In other words, we are able to reduce the *n*-trace capacitance problem to a number of 3-trace subproblems. The on-chip inductive coupling, however, extends to a *long-range* as shown and proven in [5]. Without specifying which traces are ground traces, we may compute partial inductance (denoted as L_P) under the PEEC model [7-9] and let the SPICE determines return path at simulation. Under the PEEC model, we have proposed the following foundations for the partial inductances:

Foundation 1 Self Lp of a trace is *solely* decided by the trace (its length, width and thickness).

Foundation 2 Mutual Lp of two traces is *solely* decided by the two traces (their lengths, widths and thicknesses, and the spacing between them).

The above two foundations have been proven in [5] without the consideration of the ground plane(s) in the layers below or above. With ground plane (either continuous or densely mesh), the traces become microstrip- or strip-lines. In the following, we propose new foundations for microstrip- and strip-lines based on *Raphael RI3* inductance extractions.

B. Foundations for Loop Inductance in Microstrip- and Strip-lines

Foundation 3 Self-loop inductance Ll of a microstrip- or strip-line is *solely* decided by the line (its length, width and thickness) by assuming current returns through the ground plane(s).

Foundation 4 Mutual-loop Ll of two microstrip- or strip-lines is *solely* decided by the two lines (their lengths, widths and thicknesses, and the spacing between them) by assuming currents return through the ground plane(s).

For on-chip interconnects, the spacing between a line to the ground plane is very close to a same-layer line spacing. In this situation, the majority of return current will come through the ground plane(s), validating the assumptions needed by Foundations 3 and 4. Our *Raphael RI3* simulations also indicate that more than 90% current of a microstrip-line returns through the ground plane at frequency 1GHz and above. An even higher percentage of current will return via ground planes for strip-lines. Therefore, we are still able to build the self inductance table with two dimensions

(width and length), and the mutual inductance table with four dimensions (two widths, spacing and length), but the loop inductance rather than the partial inductance is pre-computed and stored for each structure of the microstrip- or strip-line. Because the loop inductance has taken the effect of power/ground planes into account, there is no need to explicitly model the inductance for power/gound planes for the final RLC model. Figure 5 presents example to illustrate Foundations 3 and 4.

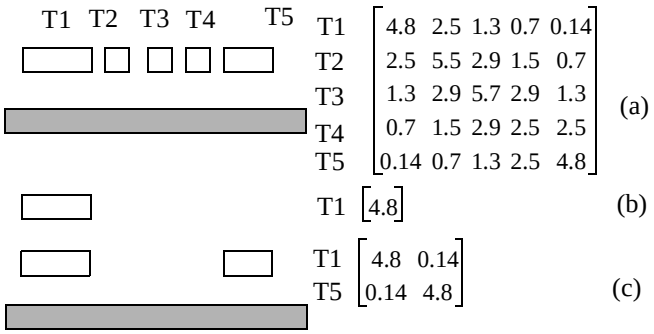

Figure 5:Loop inductance (in unit of 0.1nH) for (a) an array in layer N with a ground plane in layer N-2, (b) trace T1 only, and (c) two traces T1 and T5. From (b), one can observe that Foundation 3 is valid. From (c), we prove that Foundation 4 holds.

III. **Table-based Inductance Extraction**

Foundations 1-4 enable us to reduce the *n* trace inductance problem into 1-trace subproblems to solve the self Ll, and into 2-trace subproblems to solve the mutual Ll. There is *no* loss of accuracy during the reduction. We propose to build tables via numerical inductance extraction for self and mutual inductances.

There are two parts in the table-based inductance extraction. One is to pre-compute inductance tables. We assume that each layer has a nominal thickness, and build tables for different layers. The self inductance table has two dimensions: width and length. The mutual inductance table has three dimensions: widths for two traces and the spacing between them. The 3D inductance extraction tool RI3 [6,9] is invoked to solve a block of two traces with or without ground plane(s) in layer N+2/N-2 for different combinations of lengths, widths, and spacings. The resulting self and mutual inductance is stored in tables. Note that only 2-trace subproblems need to be solved, because results to 1-trace subproblems are parts of results to 2-trace subproblems. In addition, the inductance depends on the skin depth, which is a function of frequency [1]. We run RI3 under the significant frequency. The significant frequency is defined as $0.34/t_r$, where t_r is the minimum rising/falling time [1].

The other part of the table-based inductance extraction is table lookup. For each trace in a block, we obtain a self inductance from tables for a given layer, length and width. For any combination of two traces Ti and Tj, we obtain a mutual inductance from tables for a given layer, widths, and spacing between Ti and Tj under specified N+2/N-2 environment. A bi-cubic spline algorithm [10] is used to interpolate/extrapolate inductance that is not given in the table.

IV. **Inductance Modeling for Cascaded Wire Segments**

The discussion in the previous sessions assumed isolated multi-conductor systems with or without ground plane(s). The inductive couplings from other neighboring wires to the systems or vice versa are ignored. If there is no ground plane or ground mesh on chip, the inductive coupling (or return paths) may extend to very long range. Their couplings will be significant and may not be ignored. Hence, it is difficult to model the inductance for cascaded multi-conductor wire segments of a net. In this session, we will show from *Raphael RI3* inductance extraction results that if a signal wire is guarded by two ground wires of *at least equal width* either on left and right in the same layer or on the layers above and below with or without local ground plane(s), then this kind of multi-conductor systems may be linearly cascaded to determine the total effective loop inductance. In other words, the total loop inductance is the serial or parallel combination of the loop inductances of the cascaded segments determined individually. This conclusion indicates that those two guarded ground wires completely shield the inductive coupling from one multi-conductor system to its environment. This conclusion is important while applying the structure to high-speed clock design and will be discussed in the next session.

To show this linear cascadability, we performed *Raphael RI3* extraction to determine the loop inductances of the two interconnects in Figure 6(a) and Figure 6(b). Each segment is composed of a three-wire multi-conductor system where a center signal wire is sandwiched by two ground wires. Their widths *w* are equal. The loop inductances thus determined are compared with the results determined by serially or parallely

combining the loop inductance of each segment. For example, the loop inductance to be compared for Figure 6(a) is $L_{ab} + (L_{bc} + L_{ce}) \| (L_{bd} + L_{df})$, where each L is a loop inductance, determined independently from the others.

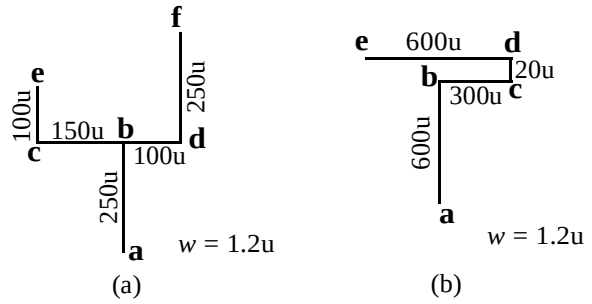

Figure 6: Two interconnect trees. Each segment of the trees is a three-same-width-wire multi-conductor system.

The comparisons are summarized in Table I. We would observe difference on the results if the inductive coupling going beyond each multi-conductor system, especially when significant portions of the systems are near-by. From the results in the table, we see the discrepancy is small (only about 3.5%), and hence we have the linearly cascadable conclusion. Our examples with different spacings and lengths also support this conclusion. Since the width of each ground wire is the same as that of the signal wire and the shielding will improve if wider ground wires are used, we then have the *at least equal width* conclusion.

	Loop *L* from RI3	Eff. Loop *L* from S/P combination	Error %
Fig. 6(a)	0.140 nH	0.145 nH	3.57%
Fig. 6(b)	0.517 nH	0.525 nH	1.55%

TABLE I . Linear Cascading Comparisons to demonstrate the effectiveness of clock net shielding.

V. **Application of Efficient Inductance Modeling in Clocktree RLC Extraction**

Several recent papers [3,11] have pointed out that it is importan to use RLC model (rather than RC model) for clocktree. In the following examples, we will illustrate the efficiency of our inductance modeling, and discuss how to generate RLC SPICE decks for a clocktree. Our experiments show that the difference in terms of clock skew may be more than 10% between RLC model and RC model. If the clock signal has significant overshoot/ undershoot due to the inductance effect, the result can be even more devastating.

Figure 7 shows the schematic for a buffered clock H-tree. We consider two types of interconnect configurations along the clocktree: co-planar waveguide design in Figure 8 and microstrip configuration in Figure 9. It's a common practice to have a local ground plane to shield the inductive coupling from adjacent layers [2]. We zoom into a segment, say segment *i*, between adjacent levels of clock buffers of the H-tree in Figure 7 and extract RLC for the segment.

We extract the resistance, capacitance, and inductance separately for each segment as shown in Figure 7. Capacitance and inductance are generated by looking-up the pre-characterized capacitance and inductance tables as discussed in [4-5] and in previous sections. Resistance is calculated analytically [4]. Depending on the clocktree shielding configurations as in Figure 8 or Figure 9 for an individual segment, corresponding inductance values are obtained via interpolation from the inductance table. As experimentally proven in Section IV, we can formulate a RLC netlist for the whole passive portion of a clocktree between two levels of the clock buffers using cascaded segment method. However, we still need the following assumptions to complete the RLC netlist formulation for the whole clocktree.

First, the inductance (self or mutual) is not scalable with length as shown in [1]. Both self and mutual inductance are super-linear functions of the trace length. For example, if a segment length changes from 1000um to 2000um, the self- and mutual-inductances increase by about 2.2-2.4 times. Therefore, we tend to underestimate the inductance for a segment like segment *i* in Figure 7. This is because that all the segments such as *i, o, j, p, k,* etc. are all connected so the inductance should be extracted from the whole connectivity if there are no alternative return paths. However, based on experiments in Section IV, we can neglect the mutual couplings

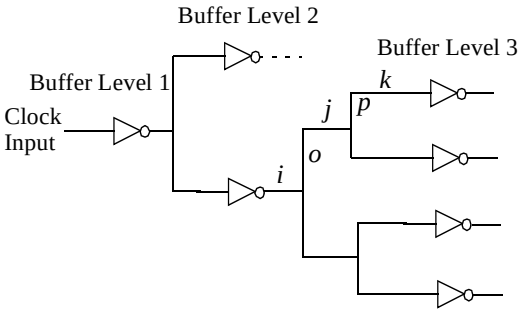

Figure 7:Example Clock Buffer H-tree Schematic

between different segments such as between *i* and *j*, or *i*

and *k*. Furthermore, there can be regular connections to the near by ground nodes (such as ground C4 bumps) from the shielding ground wire and therefore providing shorter return paths. Hence, our assumption on extracting inductance for each segment separately and then cascading them together along the path to formulate the RLC netlist is experimentally valid.

Second, how do we include the coupling effect from the other signal wires outside of a clocktree segment as shown in Figure 9? In our efficient inductance models, we can easily construct the RLC netlist for a N parallel wires as in Figure 8 or Figure 9. Therefore, the coupling effect, mainly inductive coupling of other signals next to the clocktree can be taken care of by simply adding them in the clocktree simulation.

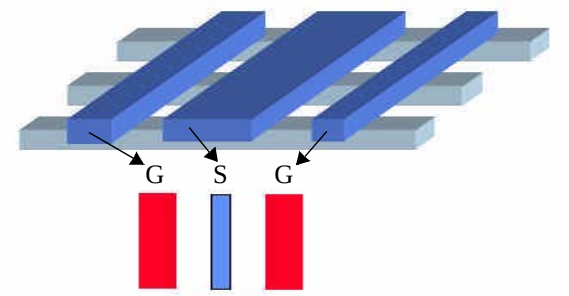

Figure 8:Co-planar waveguide configuration as a basic building block for clocktree signal distribution.

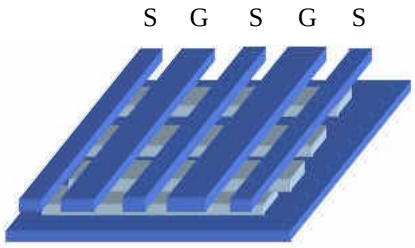

Figure 9:Microstrip configuration as another basic building block for clocktree signal distribution.

Since inductance is not sensitive to process variation as shown in [5], we can combine the nominal inductance with the statistically generated RC [4] in the formulation of RLC netlist to study process variation for clock skew.

VI. **Discussions and Conclusions**

In this paper, we have presented an efficient table-based inductance extraction methodology for on-chip microstrip- and strip-lines, which is an extension to [5]. We showed that the inductance extraction may be decomposed into one-line or two-line sub-problems without the need to consider other wires in the environment. We also have applied it to clocktree RLC extraction by cascading RLC-segments determined individually. We validated linear cascading assumpation via a number of simulation experiments.

VII. **Acknowledgments**

We would like to thank the help and stimulating discussions from E. Berta, G. Blair, and S. Wells.

VIII. **References**

[1] J. Lillis, C.K. Cheng, S. Lin, and N. Chang, “Interconnect Analysis and Synthesis,’’ Nov., John Wiley & Sons Inc., 1999.

[2] S. Morton, ‘‘On-Chip Inductance Issues in Multiconductor Systems,’’ ACM/IEEE DAC, 1999.

[3] P. Restle, A. Ruehli, and S. Walker, ‘‘Dealing with Inductance in High-Speed Chip Design’’, ACM/IEEE DAC, 1999.

[4] N. Chang, V. Kanevsky, O. S. Nakagawa, K. Rahmat, and S.-Y. Oh, “Fast Generation of Statistically-based Worst-Case Modeling of On-Chip Interconnect”, IEEE ICCD 1997.

[5] L. He, N. Chang, S. Lin, and O. S. Nakakawa, ‘‘Efficient Inductance Modeling for On-chip Interconnects’’, IEEE CICC, 1999.

[6] Raphael User Manual, Avant! Corporation

[7] A.E. Ruehli, ”Inductance Calculation in a Complex Integrated Circuit Environment,” IBM Journal of Res. & Dev., 1972.

[8] A.E. Ruehli, ”Equivalent Circuit Models for Three-Dimensional Multiconductor Systems,” IEEE Trans. on MIT, 1974.

[9] M. Kamon, M.J. Tsuk, J. White, ”Fasthenry: a Multipole-Accelerated 3D Inductance Extraction Program,” IEEE Trans. on MIT, 1994.

[10]W. Press, S. Teukolsky, W. T. Vetterling and B. P. Flannery, “Numerical Recipes in C,” Cambridge University Press, 1992.

[11]K. Bernstein, et al, ‘‘High Speed CMOS Design Styles’’, Kluwer Academic Publishers, 1998.