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Analysis and Justification of a Simple, Practical 2 1/2-D Capacitance Extraction Methodology *

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Abstract

This paper addresses post-routing capacitance extraction during performance-driven layout. We first show how basic drivers in process technology (planarization and minimum metal density requirements) actually simplify the extraction problem; we do this by proposing and validating five "foundations" through detailed experiments with a 3-D field solver on representative $0.50\mu m$, $0.35\mu m$ and $0.18\mu m$ process parameters. We then present a simple yet accurate 2 1/2-D extraction methodology directly based on the foundations. This methodology has been productized and is being shipped with the Cadence Silicon Ensemble 5.0 product. We conclude that the 2 1/2-D approach has sufficient accuracy for current and near-term process generations. An extended abstract of this paper can be found in the proceedings of *ACM/IEEE Design Automation Conference*, Anaheim, CA, June 9-13, 1997.

*This work is partially supported by Cadence under the 1996 California MICRO Program. Lei He did much of this work as an intern at Cadence in the summer of 1996, and is now working on his Ph.D degree at UCLA. A. B. Kahng is currently a visiting scientist at Cadence. Correspondance of this work can be addressed to ak@cadence.com and helei@cs.ucla.edu.

1 Introduction

In deep-submicron VLSI, complex 3-dimensional interconnect structures pose a difficult challenge for parasitic capacitance extraction. Many extraction approaches exist, including 1-D, 2-D and 2 1/2-D analytic models [11, 2, 4, 12, 13, 5, 6, 1, 18] as well as 2-D and 3-D field solvers [10, 15, 14, 9, 7, 8]. These techniques span a wide range of cost-accuracy regimes.

- 1-D analysis uses (per-unit length) total capacitance, equivalent to (per-unit area) area capacitance and (per-unit length) edge capacitance when some wire width is assumed.
- 2-D analysis uses (per-unit area) area capacitance and (per-unit length) lateral+fringing capacitance, where geometries on neighboring layers are at best probabilistically modeled.
- 2 1/2-D analysis (sometimes called "2-D, 3-Body" analysis) uses (per-unit area) area capacitance and (per-unit length) lateral and fringing capacitances, where geometries on one or more neighboring layers are explicitly modeled but then lumped additively into "above" and "below" corrections to the coupling calculation.
- 3-D analysis uses numerical techniques (finite-element as in [10] and Ansoft's products, or finite-difference as in [15, 14] and TMA Raphael) to solve Laplace's equation for potential distribution, then applies Gauss's theorem to yield charge distribution, then applies $Q = [C]V$ to determine self- and mutual capacitances of all conductors. Boundary-element numerical techniques [9] can exploit the flatness and rectilinearity of IC geometries. In addition, multipole algorithms [8] has been recently reported.

However, an effective design flow requires a *principled* matching of the parasitic extraction methodology to the actual requirements for accuracy and runtime.

Our discussion will focus on the difficult task of post-routing capacitance extraction during performance-driven layout design. Such an extraction must be accurate: correlation with "final" verification engines is needed for design convergence. Such an extraction must also be fast: it may be performed dozens of times on full-chip layout, and thousands of times on critical signal nets, during the iterative loop (placement, routing, extraction, delay calculation, timing/noise analysis) of layout design. Simple 1- and 2-D extraction may not suffice in deep-submicron design. First, wire aspect ratios (thickness divided by width) are becoming larger (e.g., they have reached 1.0 in $0.50\mu m$ logic processes and 1.5 in $0.35\mu m$ logic processes, and will reach 2.5 in $0.18\mu m$ logic processes [17]) so that lateral and fringe couplings become much more significant. Second, increased packing densities, lower supply voltages, and use of dynamic logic for performance optimization all lead to much tighter signal integrity margins, so previously second-order details such as crossover and crossunder couplings must be modeled. At the same time, full 3-D numerical extraction is difficult to support during layout due to its time complexity. For these reasons, the 2 1/2-D approach has been well-studied in recent years [5, 3, 1].

Our first contribution lies in showing how basic drivers in process technology (planarization and minimum metal density requirements) are actually making the parasitic capacitance extraction problem easier, enabling a simple yet accurate 2 1/2-D methodology. Our second contribution is a simple yet accurate 2 1/2-D extraction methodology [16] that has recently been developed and validated in cooperation with major ASIC suppliers; this methodology has been productized and is being shipped with the first release of the Cadence Silicon Ensemble (SE) 5.0 product.

Using a numerical 3-D field solver and leading-edge technology parameters, we first establish the following "foundations".

1. Ground, and neighboring wires in the same layer have significant shielding effects. Thus, both must be considered for accurate modeling.

2. Coupling between wires in layer $i-1$ and wires on layers $i+1$ is negligible when the metal density on layer i exceeds a certain threshold.

3. During capacitance extraction for wires on layer i, layers $i \pm 2$ can be treated as ground planes with negligible error. There is no need to look beyond layers $i \pm 2$.

4. Coupling analysis to wires in the same layer need only consider nearest neighbors independently, with the widths of same-layer neighbor wires having negligible effect on the coupling.

5. The interaction of layer $i-1$ in conjunction with layer $i+1$ on layer i is negligible; therefore, corrections for orthogonal crossovers and crossunders can be performed independently.

These foundations imply that for a given victim wire on layer i, wires on layers $i-2$ and $i+2$ can be treated as ground planes (with farther layers being ignored), while nearest neighbor wires on layer i, as well as all crossover and crossunder wires on layers $i-1$ and $i+1$, must be considered.

The above foundations justify a simplified 2 1/2-D extraction methodology, and can be used to guide the development of analytical formulas for parasitic capacitance. The Cadence Silicon Ensemble 5.0 product contains just such a simplified methodology, which has been developed and validated in cooperation with Motorola and other ASIC suppliers. The methodology entails one-time use of a 3-D field solver to determine the capacitance matrices for multiple predetermined "patterns" (i.e., multi-layer interconnect structures) that vary in widths and spacings of the victim on layer i, and widths and spacings of wires on crossover/crossunder layers $i-1$ and $i+1$. Linearity assumptions allow simple derivation of coefficients that capture per-unit length area, lateral and fringe components of the parasitic capacitance, along with corrections for crossovers and crossunders. In the actual post-routing extraction, a victim net's same-layer neighbors, crossovers, and crossunders are extracted from the geometric layout database, and total capacitance of the victim net is determined by simple pattern-matching and linear interpolation. Experiences of Cadence industrial partners show that the methodology produces satisfactory results.

The remainder of this paper is organized as follows. Section 2 uses 3-D numerical simulations based on representative 0.5 μm, 0.35 μm and 0.18 μm processes to justify these foundations. The Cadence SE 5.0 2.5-D RC extraction methodology, which is based on these foundations, is then described in Section 3; example structures are used to show the accuracy of the methodology. We conclude that the 2 1/2-D extraction method proposed in this paper is sufficient for delay calculation and estimation for performance-driver layout in deep submicron designs.

2 Foundations

2.1 Preliminaries

A multilayer VLSI process has metal interconnects, or wires, on layers $1, 2, \ldots, k$ (i.e., M1, M2, ..., Mk). Currently, there are $k = 6$ layers in leading-edge processes, but $k = 8$ or more will be seen by the turn of the century. We call the multilayer geometric structure of wires a *pattern*. We assume that wires in adjacent layers are orthogonal, which is often true in layout designs. We use geometric parameters of maximum-density local interconnects in $0.50\mu m$, $0.35\mu m$ and emerging $0.18\mu m$ processes(see Table 22 in [17]), and normalize all dimensions with respect to the minimum wire width in a given interconnect structure. The following *normalized* dimensions are used: For $0.50\mu m$ processes, wire width = 1.0, wire thickness = 1.0, and dielectric height between adjacent layers = 1.5(see Figure 1); for $0.35\mu m$ processes, wire width = 1.0, wire thickness = 1.5, and dielectric height between adjacent layers = 1.5; for $0.18\mu m$ processes, wire width = 1.0, wire thickness = 2.5, and dielectric height between adjacent layers = 3.0.[1] Let s be the edge-to-edge spacing between a wire (the *victim*) and its same-layer neighboring wires (*neighbors*). We typically study the "extreme" cases of $s = 1.0$ and $s = \infty$, with the latter meaning that the neighbors are too far away to have significant coupling to the victim.

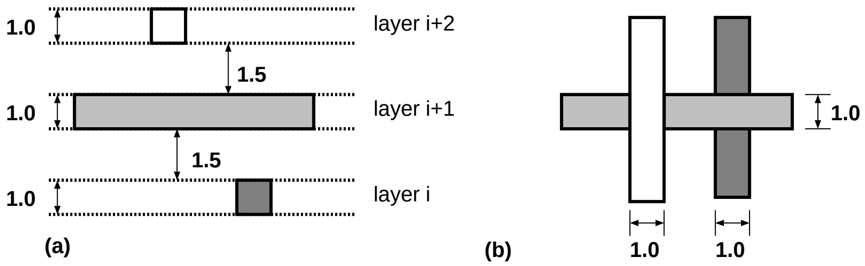

Figure 1: For the maximum-density local interconnect structure in $0.50\mu m$ process, we assume (a) the cross-section view – the thickness is 1.0 for all wires, and the height is 1.5 for all dielectrics (inter-layer spacings); (b) the top view – all wire have width 1.0.

We use an industrial-strength multipole-accelerated 3-D field solver, Fastcap[2] [8], to obtain coupling capacitances between multiple conductors in the form of a capacitance matrix. Since we run Fastcap on normalized patterns in free space, we obtain *normalized capacitances* as output. For example, if the minimum wire width in a pattern is $0.36\mu m$, a normalized capacitance of $100pF$ implies actual capacitance of

$$100(pF) \cdot 0.36(\mu m/m) \cdot \epsilon_r = 0.1404fF$$

where we assume that the relative permittivity of SiO_2 is $\epsilon_r = 3.9$. We will report only *normalized* values for

[1] Let $AR = thickness/width$ denote the aspect ratio for a wire. We see that higher AR values are achieved in more advanced processes, and are deployed for better wiring density. According to Table 22 in [17], the expected value of AR is 1.5 for $0.35\mu m$ processes. For such processes, the expected ratio between the wire thickness and the dielectric thicknesses is $0.6\mu m : 1.0\mu m = 1 : 1.67$. Compared with the $AR = 1.5$ case in our experiment using the normalized wire thickness 1.5 and the normalized dielectric thickness 1.5, the Roadmap's $0.35\mu m$ process has a *relatively* thicker dielectric, perhaps to provide better isolation. Therefore, our foundations concerning the coupling between different layers can be safely extended to the Roadmap's $0.35\mu m$ process. Furthermore, AR according to the Roadmap is generally interpreted with respect to the minimum wire width. In real designs, smaller AR values often apply due to non-minimum wire width on layers above M1 and possibly even including M1; this again implies relatively less coupling between sidewalls and allows our foundations to be safely extended.

[2] Fastcap is a public-domain program available by anonymous ftp from rle-vlsi.mit.edu. It is an element of several commercial products, e.g., from Quantic and Ansoft.

all dimensions and capacitances (in units of pF), as only the ratios between different capacitance values are significant to our study.

2.2 Coupling between wires on layer i and wires on layer $i - 2$

Two experiments study coupling between wires on layers i and $i - 2$, as well as effects of ground planes and same-layer neighboring wires. The pattern for the first experiment has one wire (*victim*) on layer i and one wire on layer $i - 2$, but no wires on layer $i - 1$ (see Figure 2). Let s_{center} be the horizontal distance between the *centers* of the two wires. We shift the wire on layer $i - 2$ and observe the change of the ratio between $C_{i,i}/C_{i,i-2}$, where $C_{i,i}$ is the total capacitance for the victim, and $C_{i,i-2}$ the coupling between the two wires. We also study the two cases where layer $i - 3$ is ground, and where there is no ground at all. Last, we consider two possible spacings ($s = 1.0, \infty$) for the two same-layer neighbors of the victim. All wires have length 20 and the ground is a 40×40 plane. Table 1 shows the following for $0.18\mu m$ process:

- The ground has a strong shielding effect on $C_{i,i-2}$. In the case of no neighbors and full overlap ($s_{center} = 0$), $C_{i,i-2}/C_{i,i} = 28.4\%$ when there is no ground versus 16.3% when there is a bottom ground plane.

- Neighboring wires also have a significant shielding effect on $C_{i,i-2}$. With two neighbors at $s = 1.0$, $s_{center} = 0$ and a bottom ground present, $C_{i,i-2}/C_{i,i} = 1.8\%$ versus 16.3% when there are no neighbors.

- The parallel-plate capacitance from overlap of the victim on layer i and the wire on layer $i - 2$ is not the dominant component in the coupling. From full overlap ($s_{center} = 0$) to non-overlap ($s_{center} = 1$), relative changes in the coupling capacitance are less than 2%.

Similar trends can be observed for $0.50\mu m$ and $0.35\mu m$ processes.

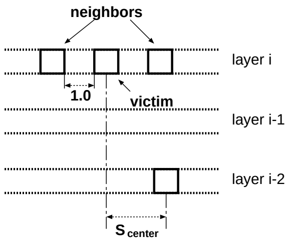

Figure 2: Cross-section of a pattern in the first experiment of Section 2.2.

In practice, there is always at least one ground (e.g., the substrate), and the likelihood of neighboring wires is high (see Footnote 3). Furthermore, it is unlikely that there are no wires on layer $i - 1$. We study the effect of wires on layer $i - 1$ using a pattern with one wire on layer i (the victim), one parallel and fully-overlapped wire on layer $i - 2$ (similar to $s_{center} = 0$ in the first experiment), and a number of wires (*crossunders*) on layer

$0.50\mu m, C_{i,i}/C_{i,i-2}$				
S_{center}	$s = \infty$		$s = 1.0$	
	with ground	without ground	with ground	without ground
0.0	459.6/103.5	424.3/170.9	880/48	874/71
1.0	458.1/101.6	422.5/168.2	897/47	873/68
4.0	499.0/71.0	403.6/139.0	877/26	867/48
10.0	441.4/25.0	374.9/88.0	876/7	865/27
$0.35\mu m, C_{i,i}/C_{i,i-2}$				
S_{center}	$s = \infty$		$s = 1.0$	
	with ground	without ground	with ground	without ground
0.0	483.8/106.4	449.2/174.0	1063/44.22	1063/65.36
1.0	483.0/104.1	446.9/171.4	1063/43.14	1061/64.08
4.0	475.0/78.9	432.0/148.4	1058/26.29	1056/49.11
10.0	466.0/33.2	403.7/98.3	1057/8.98	1053/28.40
$0.18\mu m, C_{i,i}/C_{i,i-2}$				
s_{center}	$s = \infty$		$s = 1.0$	
	with ground	w/o ground	with ground	w/o ground
0.0	486.6/79.49	458.4/130.1	1428/24.77	1424/37.96
1.0	486.5/78.78	451.9/127.4	1428/24.41	1424/37.63
4.0	484.6/71.70	454.8/123.1	1428/21.03	1424/36.91
10.0	479.4/46.96	446.5/100.4	1427/12.30	1424/24.40

Table 1: $C_{i,i}/C_{i,i-2}$, where $C_{i,i}$ is total capacitance of the layer-i victim, and $C_{i,i-2}$ is its coupling to the wire on layer $i-2$.

$i-1$ (see Figure 3). We vary the number of crossunders and observe the change in both $C_{i,i}$ and the ratio $C_{i,i}/C_{i,i-2}$.

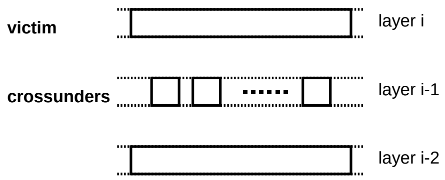

Figure 3: Cross-section for a pattern in the second experiment of Section 2.2.

$0.50\mu m, C_{i,i}/C_{i,i-2}$				
	$s = \infty$		$s = 1.0$	
	with ground	without ground	with ground	without ground
2x	484.8/95.98	457.7/165.7	881.9/50.03	880.0/75.03
4x	537.6/47.57	530.9/76.65	895.2/26.69	894.5/37.61
8x	622.2/6.066	621.9/10.5	924.4/4.59	924.9/6.51
12x	632.2/3.31	632.4/5.17	928.7/2.95	927.0/3.33
$0.35\mu m, C_{i,i}/C_{i,i-2}$				
	$s = \infty$		$s = 1.0$	
	with ground	without ground	with ground	without ground
2x	534.9/66.37	511.3/120.5	1072/30.9	1070/47.9
4x	579.9/43.9	575.0/68.4	1083/22.21	1083/30.94
8x	654.2/8.85	654.2/16.6	1106/4.392	1105/7.09
12x	685.4/1.22	681.1/5.42	1117/0.209	1117/1.17
$0.18\mu m, C_{i,i}/C_{i,i-2}$				
	$s = \infty$		$s = 1.0$	
	with ground	w/o ground	with ground	w/o ground
2x	534.5/48.45	521.5/82.3	1433/16.64	1427/25.25
4x	581.3/21.99	578.5/31.6	1437/9.185	1450/11.54
8x	622.2/3.47	622.5/6.86	1440/3.45	1457/2.67
12x	635.9/2.47	636.7/4.21	1443/2.43	1458/1.95

Table 2: $C_{i,i}/C_{i,i-2}$ values for the second experiment of Section 2.2.

Again, four possible combinations are studied: (i) layer $i-3$ is a bottom plane, or there is no ground; and (ii) the victim has two same-layer neighbors at spacing $s = 1.0$ or $s = \infty$. All wires have length 20 and the ground is a 40×40 plane. Crossunders on layer $i-1$ are evenly distributed over the ground plane. The capacitance values are given in Table 2, where 2x - 12x indicates from 2 to 12 crossunders on layer $i-1$. Note that 12x corresponds to 30% of the area on layer $(i-1)$ being occupied.[3] We observe that, in addition to the strong shielding effect on $C_{i,i-2}$ due to the ground or same-layer neighbors, more crossunders on layer $i-1$ imply less significant $C_{i,i-2}$. For example, in $0.18\mu m$ process, when there are twelve crossunders and a bottom ground, $C_{i,i-2}/C_{i,i} = 0.4\%$ with no neighbors on layer i, and 0.2% with two neighbors on layer i. Given the minimum area occupancy of metal layers in deep-submicron processes, the coupling between a wire on layer i and a wire on layer $i-2$ is not significant. We conclude the following from these two experiments:

Foundation 1 *Ground, and neighboring wires on the same layer, have significant shielding effects. Thus, both must be considered for accurate modeling.*

Foundation 2 *Coupling between wires in layer $i+1$ and wires on layers $i-1$ is negligible when the metal density on layer i exceeds a certain threshold.*

These two foundations are further verified below. Foundation 2 implies that capacitance extraction can be simplified by treating layer $i-2$, and symmetrically layer $i+2$, as ground planes. We now verify this.

2.3 Coupling between wires on layers $i \pm 2$ and i

Three experiments show that layers $i \pm 2$ can be treated as ground planes for wires on layer i. In the first experiment, there is one *victim* wire of length 20 on layer i and one *crossunder* of length 20 on layer $i-1$. The *real* pattern (see Figure 4) in practice has a number of wires on layer $i-2$, with layer $i-3$ acting as a ground plane (or the substrate is a bottom ground plane). We assume that wires on layer $i-2$ are 40 units long. We also solve a *model* pattern by treating layer $i-2$ as a 40×40 ground plane without looking beyond this layer (i.e., there is no ground plane on layer $i-3$). Our experiment varies the number (density) of wires on layer $i-2$ and compares $C_{i,i}$ and $C_{i,i-1}$ for different patterns. $C_{i,i}$ is again the total capacitance for the victim, and $C_{i,i-1}$ is the coupling between the victim and the crossunder. In Table 3, 2x - 16x indicates from 2 to 16 wires on layer $i-2$ for the real pattern; *GND* indicates the model pattern. To take $0.18\mu m$ as an example, compared with the model pattern, $C_{i,i}$ in cases 8x - 16x differs by less than 0.7% when the victim has no neighbors ($s = \infty$), and by less than 0.4% when it has two neighbors at spacing $s = 1.0$; the corresponding values are 6.2% and 7.5% for $C_{i,i-1}$.

Due to the minimum area occupancy requirement, a more likely scenario has a number of crossunders on layer $i-1$ instead of a single crossunder. Our second experiment in this section assumes that there is one *victim* on layer i, two same-layer neighbors of the victim at spacing $s = 1.0$ or $s = \infty$, and twelve crossunders $(u1, \cdots, u12)$ on layer $i-1$ (see Figure 5). All wires on layers i and $i-1$ have length 20. The *real* pattern has

[3] In deep-submicron processes ($\leq 0.35\mu m$) the minimum area occupancy of a metal layer is typically set by the foundry to 30% for uniformity of etch rate or CMP planarization. Foundries may specify certain shapes of dummy metal which are small enough so as to not hold much charge during manufacturing (e.g., 2.5 μm by 2.5 μm). The key observation is that maximum possible occupancy is 50%, even with the line-to-line spacing = 1.0. Thus, conductor structure on adjacent orthogonal wiring layers is fairly predictable.

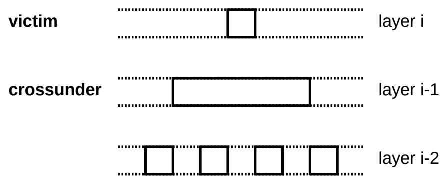

Figure 4: Cross-section of the real pattern in the first experiment of Section 2.3: the victim on layer i, one crossunder on layer $i-1$ and a number of wires on layer $i-2$. Layer $i-3$ is a ground plane, but is not shown in the figure.

	$0.50\mu m, C_{i,i}/C_{i,i-1}$		$0.35\mu m, C_{i,i}/C_{i,i-1}$		$0.18\mu m, C_{i,i}/C_{i,i-1}$	
layer $i-2$	$s=\infty$	$s=1.0$	$s=\infty$	$s=1.0$	$s=\infty$	$s=1.0$
2x	482.2/77.6	883.4/35.4	495.8/102.1	1065/40.6	513.7/112.9	1431/31.93
4x	483.5/75.7	882.0/35.1	507.1/96.98	1066/39.33	519.5/112.0	1432/33.04
8x	491.7/74.4	885.4/34.2	551.7/96.68	1077/46.04	527.4/100.5	1430/27.64
12x	496.6/72.1	886.3/33.3	527.2/87.68	1072/38.42	529.5/99.17	1430/26.64
16x	498.1/71.0	886.3/33.0	529.7/86.15	1073/37.99	530.7/98.00	1433/27.83
GND	481.5/74.8	881.4/35.6	507.7/95.49	1068/38.99	531.0/95.46	1428/30.55

Table 3: $C_{i,i}/C_{i,i-1}$, where $C_{i,i}$ is the total capacitance of the victim, and $C_{i,i-1}$ the coupling between the victim and the crossunder.

twelve wires uniformly distributed in a 40×40 plane on layer $i-2$ and a 40×40 ground on layer $i-3$; the wires on layer $i-2$ have length 40. There are two model patterns: the *model1* pattern treats layer $i-2$ as a 40×40 ground, and the *model2* pattern treats layer $i-2$ as free space. We compare the total capacitance $C_{i,i}$ for the victim wire and the coupling $C_{i,u1}, \cdots, C_{i,u12}$ between the victim wire and crossunders $u1, \cdots, u12$. Table 4 shows that

(i) Both model1 and model2 can produce similar values for total capacitance $C_{i,i}$ and couplings $C_{i,l1}$ and $C_{i,r1}$ between the victim and its same-layer neighbors, when compared with the real pattern.

(ii) Model1 is better than model2 when used to solve the coupling between the victim and crossunders. For $0.18\mu m$ process, compared with the real pattern, the largest deviations for $C_{i,u1}$, $\cdots$, $C_{i,u12}$ are 10.7% when $s=\infty$, and 14.0% when $s=1.0$ for model1; corresponding values for model2 are 45% and 72%. Furthermore, for couplings $C_{i,u3}$, $\cdots, C_{i,u10}$ between the victim and crossunders not at the boundary (see Figure 5), the deviation is at most 4.2% for model1. Since most crossunders in real designs are not at the boundary, the error introduced by model1 is negligible.

(iii) Even when same-layer neighbors have their strongest shielding at minimum spacing $s=1.0$, the

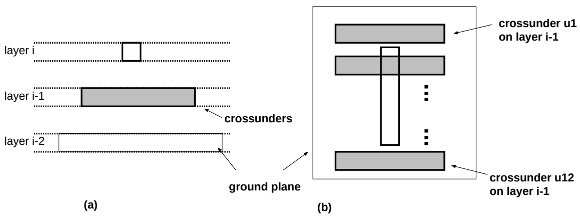

Figure 5: Layer $i-2$ is modeled as a ground plane: (a) the cross-section view; (b) the top view.

coupling mainly due to crossunders accounts for $1-(621.2+626.0)/1447 = 13.8\%$ of the total capacitance $C_{i,i}$ for $0.18\mu m$ process. More significant percentages are observed for representative $0.50\mu m$ and $0.35\mu m$ geometric parameters.. Therefore, coupling between the victim and crossunders must be considered in the capacitance extraction. We conclude that when there is no layer $i+1$ and beyond, layer $i-2$ can be viewed as a ground for computing total capacitances for wires on layer i, or coupling capacitances between wires on layer i and wires on layer $i-1$.

$0.50\mu m$	s	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,u1}$	$C_{i,u2}$	$C_{i,u3}$	$C_{i,u4}$	$C_{i,u5}$	$C_{i,u6}$	$C_{i,u7}$	$C_{i,u8}$	$C_{i,u9}$	$C_{i,u10}$	$C_{i,u11}$	$C_{i,u12}$
real	∞	618.6	-	-	7.987	11.82	33.42	65.14	71.9	73.16	73.13	71.8	63.67	29.24	9.774	5.236
model1		619.2	-	-	8.152	12.08	33.87	66 .1	73.28	74.56	74.52	73.07	64.52	29.79	9.912	5.497
model2		618.6	-	-	9.692	13.53	35.6	69.25	76.26	77.76	77.61	76.08	67.63	32.23	12.63	9.185
real	1.0	928.2	316.1	315.9	3.751	5.736	17.5	32.81	34.25	34.46	34.39	34.33	32.37	15.28	4.839	2.532
model1		927.9	316.6	313.6	3.935	5.959	17.72	33.06	34.58	34.9	34.91	34.69	32.69	15.57	4.994	2.767
model2		927.1	315.1	316.2	4.596	6.662	18.47	34.28	35.82	36.04	36.01	35.83	33.77	16.69	6.209	4.408
$0.35\mu m$	s	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,u1}$	$C_{i,u2}$	$C_{i,u3}$	$C_{i,u4}$	$C_{i,u5}$	$C_{i,u6}$	$C_{i,u7}$	$C_{i,u8}$	$C_{i,u9}$	$C_{i,u10}$	$C_{i,u11}$	$C_{i,u12}$
real	∞	669.8	-	-	9.63	13.78	37.21	70.38	77.71	78.78	78.75	77.53	68.61	32.56	11.64	6.519
model1		669.7	-	-	9.817	13.93	37.72	71.39	79.04	80.28	80.14	78.63	70.37	33.17	11.94	7.431
model2		669.7	-	-	11.7	16.36	39.96	73.94	81.26	82.36	82.17	80.68	71.64	34.91	14.83	10.59
real	1.0	1110	406.4	404.7	4.459	6.483	18.32	32.69	34.01	34.2	33.92	34.19	32.36	15.9	5.51	3.059
model1		1113	408.7	405.1	4.115	6.109	18.4	33.9	35.44	35.57	35.4	35.27	33.37	16.37	5.443	3.168
model2		1110	404.5	407.4	5.264	7.584	19.37	34.47	35.85	35.86	35.6	35.39	33.62	16.83	6.461	4.422
$0.18\mu m$	s	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,u1}$	$C_{i,u2}$	$C_{i,u3}$	$C_{i,u4}$	$C_{i,u5}$	$C_{i,u6}$	$C_{i,u7}$	$C_{i,u8}$	$C_{i,u9}$	$C_{i,u10}$	$C_{i,u11}$	$C_{i,u12}$
real	∞	629.5	-	-	16.4	19.89	36.89	50.95	59.62	61.09	60.59	61.47	51.39	32.92	16.78	12.28
model1		629.7	-	-	16.97	20.21	37.47	53.14	60.98	62.8	62.17	62.01	52.24	33.65	17.24	13.69
model2		630.8	-	-	18.56	21.24	37.45	56.19	63.3	65.61	65.58	62.85	54.74	35.73	20.21	17.94
real	1.0	1447	621.2	626	5.632	7.623	13.11	15.34	16.22	16.65	17.06	18.66	16.29	11.27	5.383	4.095
model1		1447	621	626.3	5.567	7.478	13.38	15.8	17.16	17.49	17.99	19.67	17.04	11.69	5.68	4.668
model2		1447	615.2	616.9	6.11	7.347	13.38	19.33	20.67	20.97	21.11	21.17	20.07	14.22	8.294	7.041

Table 4: Total capacitance $C_{i,i}$ of the victim on layer i and couplings between the victim and crossunders on layer $i-1$.

The third experiment of this section considers the impact of wires on layers $i+1$ and beyond. To have a geometric structure that still can be solved by Fastcap[4], we assume one victim on layer i with two same-layer *neighbors* at spacing $s = 1.0$ or ∞, six crossunders on layer $i-1$ and six crossovers on layer $i+1$. All wires on layer i have length 10, and all crossunders/crossovers have length 20. Crossunders/crossovers are uniformly distributed in 20×20 planes such that the area occupancy for layers $i \pm 1$ is 30%. In the *real* pattern, there are six wires distributed in a 20×20 plane on layer $i+2$ or $i-2$. These wires have length 20; layers $i \pm 2$ also have area occupancy of 30%. In the *model* pattern, layers $i \pm 2$ are 20×20 ground planes.

Table 5 reports total capacitance $C_{i,i}$ for the victim, same-layer couplings $C_{i,l1}$ and $C_{i,r1}$ between the victim and its neighbors, crossunder couplings $C_{i,u1}, \cdots, C_{i,u6}$ between the victim and crossunders $u1, \cdots, u6$, and crossover couplings $C_{i,o1}$, $\cdots$, $C_{i,o6}$ between the victim and crossovers $o1, \cdots, o6$. The difference between the model pattern and the real pattern is less than 0.5% for $C_{i,i}$, $C_{i,l1}$ and $C_{i,r1}$, and about 5% for crossunder or crossover coupling if the crossunder or crossover is not at the boundary in our pattern. We conclude:

Foundation 3 *During capacitance extraction for wires on layer i, layers $i \pm 2$ can be treated as ground planes with negligible error. There is no need to look beyond layers $i \pm 2$.*

[4] Shorter wires mean that the coupling due to the front and end sidewalls, as well as wire corners, is more significant. Our experiments use wires that are as long as possible, subject to Fastcap being run on a workstation with 400MB RAM.

$0.50\mu m$	s	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,u1}$	$C_{i,u2}$	$C_{i,u3}$	$C_{i,u4}$	$C_{i,u5}$	$C_{i,u6}$	$C_{i,o1}$	$C_{i,o2}$	$C_{i,o3}$	$C_{i,o4}$	$C_{i,o5}$	$C_{i,o6}$
real	∞	399.0	-	-	3.74	30.4	58.8	58.7	30.3	3.70	3.69	30.8	58.2	58.8	30.8	3.65
model		398.9	-	-	3.63	31.3	59.4	59.4	31.25	3.50	3.68	31.5	59.9	59.9	31.5	3.69
real	1.0	512.8	142.8	142.2	2.32	18.2	32.7	32.6	18.2	2.24	2.29	18.4	32.1	32.2	18.4	2.24
model		512.4	142.2	142.0	2.25	18.7	32.7	32.7	18.6	2.20	2.27	18.8	33.3	33.3	18.8	2.27

$0.35\mu m$	s	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,u1}$	$C_{i,u2}$	$C_{i,u3}$	$C_{i,u4}$	$C_{i,u5}$	$C_{i,u6}$	$C_{i,o1}$	$C_{i,o2}$	$C_{i,o3}$	$C_{i,o4}$	$C_{i,o5}$	$C_{i,o6}$
real	∞	365.0	-	-	5.16	28.7	52.0	52.0	28.5	5.15	5.27	28.7	52.1	51.7	28.6	5.19
model		365.2	-	-	5.32	29.0	52.3	52.2	28.9	5.25	5.38	29.3	52.5	52.6	29.3	5.32
real	1.0	496.3	151.5	151.2	2.95	16.0	26.6	26.6	15.8	2.91	3.05	15.9	26.7	26.6	15.9	2.96
model		496.7	151.8	151.6	3.02	16.1	26.6	26.6	16.0	2.94	3.07	16.2	26.9	27.0	16.3	3.01

$0.18\mu m$	s	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,u1}$	$C_{i,u2}$	$C_{i,u3}$	$C_{i,u4}$	$C_{i,u5}$	$C_{i,u6}$	$C_{i,o1}$	$C_{i,o2}$	$C_{i,o3}$	$C_{i,o4}$	$C_{i,o5}$	$C_{i,o6}$
real	∞	418.9	-	-	13.51	33.77	52.18	52.26	33.95	13.67	13.93	34.09	52.43	52.35	34.31	14.17
model		418.9	-	-	14.16	34.68	52.54	52.53	34.39	14.26	14.08	34.52	52.67	52.59	34.31	14.15
real	1.0	779.9	310.4	310.4	5.099	11.73	16.09	16.09	11.85	5.03	6.042	13.95	19.46	19.32	13.86	6.135
model		781.6	309.5	308.9	6.663	12.66	17.46	17.34	12.58	6.613	6.679	13.71	18.47	18.31	13.6	6.706

Table 5: Total capacitance $C_{i,i}$ of the victim on layer i, couplings $C_{i,l1}$ and $C_{i,r1}$ between the victim and its same-layer neighbors, and couplings between the victim and crossunders on layer $i-1$ or crossovers on layer $i+1$.

2.4 Coupling between wires on the same layer

To isolate the impact of crossunders and crossovers, we study the following two patterns. The *optimistic* pattern treats layers $i \pm 1$ as ground planes; this emphasizes the shielding effect due to crossunders and crossovers and in general leads to underestimation of couplings between wires on layer i. The *pessimistic* pattern treats layers $i \pm 2$ as ground planes without any wires on layers $i \pm 1$; this removes all shielding effects due to crossunders and crossovers and in general leads to overestimation of couplings between wires on layer i.

We first study the coupling between a victim wire and its non-immediate neighbors. We use a 40×40 ground plane and wires of length 20. Orthogonally with respect to the optimistic and the pessimistic patterns, we again have a *real* pattern and a *model* pattern. The real pattern has five wires on layer i, *l2*, *l1*, *victim*, *r1* and *r2* at spacing $s = 1.0$. The model pattern has only the immediate neighbors (*l1* and *r1*) of the victim. According to Table 6, differences in the total capacitance for the victim between the real pattern and the model pattern are less than 0.2%. The error associated with the model pattern for the coupling between the victim and its immediate neighbors is approximately 3%. Therefore, coupling analysis to wires in the same layer need only consider nearest neighbors.

We also study interactions between the victim's two neighbors as well as the effect of neighbor widths. We consider only the worst case interaction, given by the pessimistic pattern with wires (victim and two neighbors) on layer i and ground planes on layers $i \pm 2$. We use a 40×40 ground plane and wires of length 10. To observe the interaction between the victim's neighbors, we vary the spacings between the victim and its neighbors, and measure the change in total capacitance of the victim. Let C_{l-r} be the total capacitance of the victim when the left and right neighbors are distance l and r away ($l = \infty$ or $r = \infty$ indicates no left or right neighbor). Simulation and derived results are given in Table 7. The *derived* values are based on formula $C_{l-r} = (C_{l-l} + C_{r-r})/2$. Since differences between the simulated and derived values are often less than 1.0%, we see that couplings on opposite sides can be considered independently. To assess the effect of neighbor widths, we assume that the victim has a fixed width of 1.0, and that two neighbors (at spacing 1.0)

$0.50\mu m$	real					model		
	$C_{i,i}$	$C_{i,l2}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,r2}$	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$
optimistic	909.3	23.27	316.2	312.0	26.89	906.4	327.9	327.6
pessimistic	886.6	32.66	332.9	327.2	37.24	881.9	349.9	351.5

$0.35\mu m$	real					model		
	$C_{i,i}$	$C_{i,l2}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,r2}$	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$
optimistic	1120.0	0.8489	377.8	380.3	0.8425	1115	386.9	386.5
pessimistic	891.9	27.33	328.0	324.1	31.7	888.5	341.1	341.5

$0.18\mu m$	real					model		
	$C_{i,i}$	$C_{i,l2}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,r2}$	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$
optimistic	1451	32.04	602.2	602.1	31.67	1449	602.2	619.9
pessimistic	1436	54.9	616.6	616.5	54.86	1436	639.8	639.6

Table 6: Total capacitance $C_{i,i}$ of the victim wire on layer i and couplings $C_{i,l2}, C_{i,l1}, C_{i,r1}$ and $C_{i,r2}$ between the victim wire and its neighbors ($l2, l1, r1$ and $r2$).

$0.50\mu m$															
spacing	1-1	1-2	1-3	1-4	1-∞	2-2	2-3	2-4	2-∞	3-3	3-4	3-∞	4-4	4-∞	∞-∞
simulated	471.5	416.3	399.5	393.0	388.2	359.7	343.0	336.3	329.6	325.9	318.9	313.2	309.1	303.1	300.0
derived	-	415.6	398.7	390.3	385.8	-	342.8	334.4	329.8	-	317.5	313.0	-	304.6	-

$0.35\mu m$															
spacing	1-1	1-2	1-3	1-4	1-∞	2-2	2-3	2-4	2-∞	3-3	3-4	3-∞	4-4	4-∞	∞-∞
	568.4	410.0	360.9	340.7	318.3										
simulated	568.4	490.2	466.8	457.4	447.4	410.0	385.7	376.3	365.2	360.9	351.2	339.8	340.7	329.1	318.3
derived	-	489.2	464.65	454.6	443.4	-	385.5	375.4	364.2	-	350.8	339.6	-	329.5	-

$0.18\mu m$															
spacing	1-1	1-2	1-3	1-4	1-∞	2-2	2-3	2-4	2-∞	3-3	3-4	3-∞	4-4	4-∞	∞-∞
simulated	764.5	639.2	600.0	582.5	559.7	511.5	471.0	452.8	430.3	429.7	411.0	387.7	393.3	368.1	341.7
derived	-	638.0	597.1	578.9	553.1	-	470.6	452.4	426.6	-	411.5	385.7	-	367.5	-

Table 7: Simulated and derived total capacitances of the victim in cases of different neighbor spacing.

have identical widths. We vary the widths of the neighbors and observe the change in total capacitance of the victim (see Table 8). Since the maximum variation is less than 0.2%, widths of neighbors can be ignored. We summarize the experiments of this section by:

Foundation 4 *Coupling analysis to wires in the same layer need only consider nearest neighbors independently, with the widths of same-layer neighbor wires having negligible effect on the coupling.*

2.5 Coupling between wires on layer i and wires on layers $i \pm 1$

To study the interaction between crossunder coupling and the crossover coupling, we first observe the impact of the crossover coupling on the crossunder coupling. We assume that layer i has twelve wires $i1, \cdots, i12$, i.e., area occupancy of 30%, and that layer $i-1$ has one wire (*crossunder*) and same-layer neighbors at spacings

capacitance $C_{i,i}$				
neighbor widths	1	2	3	4
$0.50\mu m$	471.5	471.8	471.7	471.4
$0.35\mu m$	568.4	568.8	568.6	568.5
$0.18\mu m$	764.5	765.2	764.9	764.4

Table 8: Total capacitances $C_{i,i}$ for the victim in case of different neighbor widths.

$s = 1.0$.[5] We solve one pattern which treats layer $i+1$ as a ground plane (*full crossing*), which models the greatest possible effect due to crossovers, and a second pattern which treats layer $i+2$ as a ground plane without any wires on layers $i+1$ (*no crossing*), which models no effect due to crossovers. Again, we use a 40×40 ground plane and wires of length 20.

	crossover	$C_{i1,2}$	$C_{i2,2}$	$C_{i3,2}$	$C_{i4,2}$	$C_{i5,2}$	$C_{i6,2}$	$C_{i7,2}$	$C_{i8,2}$	$C_{i9,2}$	$C_{i10,2}$	$C_{i11,2}$	$C_{i12,2}$
$0.50\mu m$	full	1.628	10.71	24.02	25.29	25.41	25.03	25.22	25.00	25.06	22.27	7.734	0.8726
	no	1.709	10.78	24.08	25.36	25.47	25.08	25.29	25.06	25.16	22.31	7.800	0.9085
$0.35\mu m$	full	2.262	11.62	23.39	24.36	24.42	24.07	24.25	24.07	24.79	21.81	8.234	0.8522
	no	2.659	12.11	23.96	25.04	25.19	24.9	25.12	24.94	25.61	22.47	8.758	1.328
$0.18\mu m$	full	6.31	4.798	8.827	11.2	11.77	11.45	11.14	11.91	11.99	11.55	9.545	7.137
	no	5.946	4.902	8.576	11.5	12.35	12.25	12.09	12.91	12.91	12.27	9.935	7.334

Table 9: Crossunder couplings between wires $i1, \cdots, i12$ on layer i and the crossunder on layer $i-1$ with its same-layer neighbors at spacing 1.0 and ∞, for both full and no crossover.

We compute the crossunder coupling between wires on layer i and the central wire on layer $i-1$ (see Table 9). The difference between the two extreme cases is less than 6% (excluding cases at the boundary). Recall that the total crossunder and crossover coupling accounts for about one third of total capacitance for a victim; hence, the crossunder coupling can be computed independently without considering crossovers while introducing an error of at most 2% for the victim's total capacitance. Due to the symmetry between crossunders and crossovers, we have:

Foundation 5 *The joint interaction of layers $i-1$ and $i+1$ on layer i is negligible; therefore, corrections for orthogonal crossovers and crossunders can be performed independently.*

3 2 1/2-D Methodology

The above foundations justify a simplified yet accurate 2 1/2-D extraction methodology. The Cadence Silicon Ensemble 5.0 product contains just such a methodology [16]. For a *victim* wire on layer i, it looks into a neighborhood structure which contains layers $i \pm 2$ as ground planes, all same-layer immediate neighbors, all crossunders on layer $i-1$, and all crossovers on layer $i+1$. Rather than running 3-D field solver each time, capacitance components are generated based on predetermined capacitance coefficients and then added up to obtain the lumped capacitance for the victim. Lateral, area and fringe capacitance coefficients are predetermined for different widths and spacings for the victim on layer i. Crossover and crossunder correction capacitances are predetermined for different wire widths and spacings in both crossing layers $i \pm 1$ and layer i. In this section, we first present methods to generate capacitance coefficients by using 3-D simulation on predetermined patterns, then discuss the Cadence 2 1/2-D method to compute the lumped capacitance from capacitance coefficients. The methodology is developed and validated in cooperation with Motorola and other ASIC suppliers. Examples are also given to show the accuracy of the methodology.

3.1 Capacitance Component Generation

We assume the following:

[5] We note that a good experiment setting here should have wires of certain density on layer i, which leads to alleviated coupling between crossovers and crossunders and is a more realistic case.

- the substrate is a ground plane for layer i only if $i = 1$ or $i = 2$;
- each of layer $i+2$ and layer $i-2$, if it exists, is a ground plane (resp. the *top* and *bottom* ground planes), and hence no couplings to layers beyond them need be considered; and
- if there is no layer $i+2$, then there is no top ground plane (the substrate or layer $i-2$ is the bottom ground plane).

For 3-D simulation, ground planes should be large enough to cover wires on layers i and $i \pm 1$. In addition, we assume all wires have length l.

3.1.1 Lateral, Area and Fringe Capacitances

In addition to the bottom ground and the possible top ground, we assume a pattern with three wires (victim and neighbors) on layer i (see Figure 6) and no wires on layer $i \pm 1$. It is used to generate lateral, area and fringe capacitances for width w and spacing s, where lateral capacitance is the coupling between sidewalls of the victim and sidewalls of its neighbors, area capacitance is the coupling between grounds and the top/bottom sides of the victim, and fringe capacitance is the coupling between grounds and sidewalls of the victim.

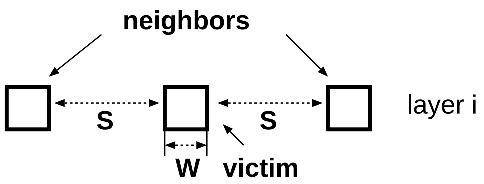

Figure 6: The geometric structure on layer i for lateral, area and fringe capacitance generation.

3-D simulation by FastCap is used to solve the pattern. Let the total capacitance for the victim be C_{self}, and coupling capacitance between it and its neighbors be C_{c1} and C_{c2}[6]. Then, the lateral capacitance coefficient C_l, defined as the lateral capacitance *per-length* and *per-side*, is given by

$$C_l = (C_{c1} + C_{c2})/(2 \cdot l) \tag{1}$$

The remaining part $C_{self} - (C_{c1} + C_{c2})$ is assumed to be the area and fringe capacitances. It needs to be separated into two parts and there are many ways to do it. One way is to run the above simulation with another width w' for the victim, and C'_{self}, C'_{c1} and C'_{c2} are obtained. The following equations are used to separate the area and fringe components:

$$C_{self} - (C_{c1} + C_{c2}) = 2 \cdot l \cdot C_a + 2 \cdot (l + w) \cdot C_f \tag{2}$$

$$C'_{self} - (C'_{c1} + C'_{c2}) = 2 \cdot l \cdot C_a + 2 \cdot (l + w') \cdot C_f \tag{3}$$

where C_a is the area capacitance coefficient, defined as the area capacitance *per-length* and *per-side*, and C_f is the fringe capacitance coefficient, defined as the fringe capacitance *per-length* and *per-side*. Coefficients C_a and C_f can be computed by solving Equations (2) and (3) simultaneously.

[6] In theory, $C_{c1} = C_{c2}$. But numeric roundoff may cause slight difference.

3.1.2 Crossover and Crossunder Correction Capacitances

According to Foundation 5, crossover and crossunder correction capacitances (C_{over} and C_{under}) can be generated independently. We simulate two patterns in order to compute C_{over}. First, we run 3-D simulation by FastCap on the pattern in Figure 7(a). In addition to the bottom ground and the possible top ground, there are three wires on layer i and three wires on layer $i+1$. Wires on layer i have width w and spacing s. Crossovers on layer $i+1$ have width w_c and spacing s_c. In general, crossover correction capacitance is a function of w, s, w_c and s_c. We obtain the total capacitance C_{self} for the central wire (the victim) on layer i.

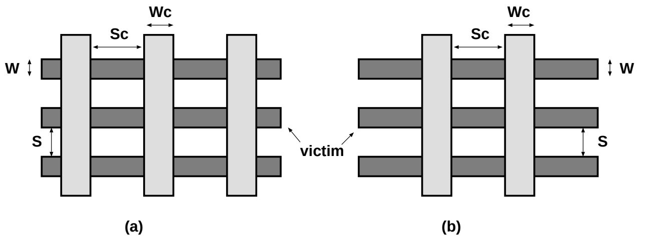

Figure 7: The geometric structure on layers i and $i+1$ for crossover correction capacitance generation.

Then, we run FastCap on the pattern in Figure 7(b). Difference from the pattern in Figure 7(a), it has only two wires on layer $i+1$. We obtain the total capacitance C'_{self} for the victim. Finally, crossover correction capacitance C_{over} is given by

$$C_{over} = (C_{self} - C'_{self})/4 \tag{4}$$

The division is necessary since C_{over} is defined for each corner, and added to the lumped capacitance for the vicitm corner by corner as shown in Table 10. The crossunder correction capacitance C_{under} can be generated similarly.

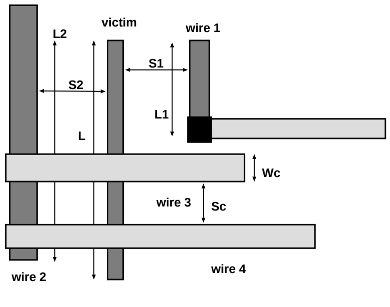

Figure 8: An example for 2 1/2-D capacitance analysis.

3.2 Algorithm for 2 1/2-D Analysis

A typical situation that can occur in gate-array and standard-cell digital IC designs is shown in Figure 8. The victim wire on layer i is being analyzed. *Wire1* and *wire2* are same-layer neighbors and *wire3* and *wire4* are crossovers. We first obtain geometric parameters from the layout database, including width w for the victim, *effective* lengths[7] and spacings, $< l_1, s_1 >$ and $< l_2, s_2 >$, for neighbors wire1 and wire2, and the width and spacing, $< w_c, s_c >$, for every crossover and crossunder (only the width and spacing for the crossover wire3 are shown in this Figure). This information is then used to calculate the capacitance for the victim as given in Table 10. In this table, the *look_up_range* is the minimum spacing between the victim and its neighbor when the coupling between them is negligible. Furthermore, linear interpolation is used to compute values between different widths in the look-up table, and linear interpolation on $1/spacing$ is used to compute values between different spacings in the look-up table. Therefore, at least two widths and at least two spacing for each width should be pre-analyzed and stored in the look-up table. If only two spacings are used for a width, one should be the *look_up_range*. Moreover, linear extrapolation is used for widths and spacings that exceed values given in the look-up table. Closed-form formulas which are more sophisticated than our linear interpolation and extrapolation are were presented in [5, 1]. Those formulas can also be used here. However, in gate-array and standard-cell digital IC designs, choices of widths and spacings are usually limited. Therefore, a look-up table with a reasonable size can be sufficient with limited using of interpolation and extrapolation. It was shown by real designs that our linear interpolation and extrapolation produces satisfactory results.

Begin 2 1/2-D analysis
For any given victim wire segment of width w and length l
  Let the lumped capacitance for the victim be $C_{self} = 0$
  For each side of length l
    Find out all the same-layer neighbors within *look_up_range*
    Let their effective lengths be l_i and spacing s_i
    For each neighbor
      Lookup lateral, area and fringe capacitance coefficients (C_l, C_a and C_f) for s_i and w
      $C_{self} = C_{self} + (C_l + C_a + C_f) \cdot l_i$
    Endfor
    For any crossover of width w_c
      Get the next crossover and determine spacing s_c
      Lookup the crossover correction capacitance C_{over} for w, s_i, w_c, s_c
      $C_{self} = C_{self} + C_{over}$
    Endfor
    For each side of a crossunder of width w_c
      Determine spacing s_c to the neighboring crossunder in the side
      Lookup the crossunder correction capacitance C_{under} for w, s_i, w_c, s_c
      $C_{self} = C_{self} + C_{under}$
    Endfor
  Endfor
  For each side of width w
    Find out all the same-layer neighbors within *look_up_range*
    Let their effective lengths be l_i and spacing s_i
    For each neighbor
      Lookup lateral and fringe capacitance coefficients (C_l and C_f) for s_i and w
      $C_{self} = C_{self} + (C_l + C_f) \cdot l_i$
    Endfor
  Endfor
End

Table 10: Algorithm for 2 1/2-D analysis.

[7] The effective length of a neighbor for a victim is length of the parallel part of both wires.

	2 1/2-D analysis	3-D simulation	error
smaller net	6.53552	6.5713	-0.54%
larger net	3152.42	3261.17	-3.33%

Table 11: Comparison between 2 1/2-D analysis and 3-D simulation

3.3 Examples with 2 1/2-D analysis

Two nets were extracted from real designs and their lumped capacitances were computed based on the 2 1/2-D methodology. We also separated the two nets into a number of small sections and used 3-D simulator FastCap to solve all the relevant geometries for such sections. Capacitances from different sections were then added up. We compared results from two methods in Table 11. The errors are 0.54% for the smaller net and 3.33% for the larger one. Moreover, our method has been validated in cooperation with Motorola and other ASIC suppliers by comparing extracted values with measured values.

A software tool has been developed to automate the coefficient generation. The input to this program consists of thicknesses[8], permissible widths and spacings for wires on every metal layer, and thickness and effective permittivity for the dielectric between adjacent metal layers. The tool automatically generates capacitance coefficients based on 3-D simulation and writes out a LEF file containing all capacitance coefficients.

4 Conclusions

We have addressed post-routing capacitance extraction as it is typically required during performance-driven layout. The context of our methodology would be any standard deep-submicron ASIC design flow, e.g., with a back-end block implementation loop consisting of (1) (incremental) placement, (2) (incremental) global and detailed routing, (3) parasitic extraction, (4) delay calculation and timing/noise analysis (5) driver, buffer and routing topology/wirewidth optimization, and (6) netlist engineering change.

We have validated five “foundations” that allow simplification of the capacitance extraction problem for multilayer interconnects. We have also described a simple yet accurate 2 1/2-D extraction methodology, now implemented in a commercial cell-based layout tool. We showed that this methodology gives results that are very close (within a few percent) to measured silicon and 3-D numerical simulation. Typical extraction and performance verification flows often ignore one or more factors such as process variations, thermal gradients, errors in device and cell characterization, foundry insertion of dummy metal, etc. Since these errors can swamp our several percent error versus 3-D simulation, we conclude that the proposed 2 1/2-D methodology is sufficient for layout optimization. Our ongoing research and development seeks a more holistic integration of synthesis and analysis activities within a framework for constraint-driven design.

References

[1] N. D. Arora, K. V. Raol, R. Schumann, and L. M. Richardson, “Modeling and Extraction of Interconnect Capacitances for Multilayer VLSI Circuits its,” *IEEE Trans. on Computer-Aided Design*, vol. 15, no. 1,

[8] It is possible to have different wire thicknesses in a metal layer.

Jan., 1996, pp. 58-67.

[2] E. Barke, "Line-to-Ground Capacitance Calculation for VLSI: A Comparison," *IEEE Trans. on Computer-Aided Design*, vol. 7, no. 2, 1988, pp. 295-298.

[3] M. Basel, "Accurate and Efficient Extraction of Interconnect Circuits for Full-Chip Timing Analysis," *Proc. WESCON*, pp. 118-123, 1995.

[4] J. Chern, J. Huang, L. Aldredge, P. Li and P. Yang, "Multilevel Metal Capacitance Models for Interconnect Capacitances," *IEEE Electron Device Lett*, vol. EDL-14, pp. 32-43, 1992.

[5] U. Choudhury and A. Sangiovanni-Vincentelli, "Automatic Generation of Analytical Models for Interconnect Capacitances," *IEEE Trans. on Computer-Aided Design*, vol. 14, no. 4, April, 1995, pp. 470-480.

[6] N. Delorme, M. Belleville and J. Chilo, "Inductance and Capacitance Analytic Formulas for VLSI Interconnects," *IEEE Electron Device Lett*, vol. EDL-32, pp. 996-997, 1996.

[7] R. Guerrieri and A. Sangiovanni-Vincentelli, "Three-Dimensional Capacitance Evaluation on a Connection Machine," *IEEE Trans. on Computer-Aided Design*, vol. 7, pp. 1125-1133, 1988.

[8] K. Nabors and J. White, "Fastcap: A Multipole Accelerated 3-D Capacitance Extraction Program," *IEEE Trans. on Computer-Aided Design*, vol. 10, no. 11, Nov. 1991, pp. 1447-1459.

[9] Z. Ning and P. M. Dewilde, "SPIDER - Capacitance Modeling for VLSI Interconnections," *IEEE Trans. on Computer-Aided Design*, vol. 7, no. 12, pp. 1221-1228, Dec. 1988.

[10] A. E. Ruehli and P. A. Brennan, "Efficient Capacitance Calculations for Three-Dimensional Multiconductor Systems," *IEEE Trans. on Microwave Theory Tech.*, vol. MTI-21, pp. 76-82, 1973.

[11] T. Sakurai and K. Tamaru, 'Simple Formulas for Two- and Three- Dimensional Capacitances," *IEEE Trans. on Electron Devices*, vol. ED-30, pp. 183-185, 1983.

[12] T. Sakurai, "Closed-Form Expressions for Interconnect Delay, Coupling, Crosstalk in VLSI's," *IEEE Trans. on Electron Devices*, vol. ED-40, pp. 118-124, 1993.

[13] G. S. Samudra, and H. L. Lee, "A Set of Analytical Formulas for Capacitance of VLSI Interconnects of Trapezium Shape," *IEEE Trans. on Electron Devices*, vol. ED-41, pp. 1467-1469, 1994.

[14] A. Seidl, A. Svoboda, J. Oberndorfer, and W. Rosner, "CAPCAL - A 3D Capacitance Solver for Support of CAD Systems," *IEEE Trans. on Computer-Aided Design*, vol. 7, no. 11, 1988, pp. 549-556.

[15] R. H. Uebbing and M. Fukuma, "Process-Based Three-Dimensional Capacitance Simulation–TRICEPS," *IEEE Trans. on Computer-Aided Design*, vol. 5, 1986, pp. 215-210.

[16] S. Yen, N. Shirali, "Capacitance Extraction", Cadence Design Systems *application Note*, 1995.

[17] Semiconductor Industry Association, *National Technology Roadmap for Semiconductors*, 1994.

[18] F. C. Wu, S.C. Wong, P. S. Liu, D. L. Yu and F. Lin "Empirical Models for Wiring Capacitances in VLSI," *Proc. IEEE Int'l Symp. on Circuits and Systems*, 1996.