An Efficient Inductance Modeling for On-chip Interconnects

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Abstract. In this paper, we present an efficient yet accurate inductance extraction methodology. We first show that without loss of accuracy, the extraction problem of n traces can be reduced to a number of one-trace and two-trace subproblems. We then solve one-trace and two-trace subproblems via a table-based approach. The table-based inductance model has been integrated with a statistically-based RC model generation [1] to generate RLC models for on-chip interconnects. Application examples show that our method is efficient enough to be used during iterative procedures of interconnect simulation and layout optimization.

I. Introduction

It has been shown for years that interconnect delay and crosstalk have become bottle necks in determining circuit performance. In order to simulate and optimize on-chip interconnects, the parasitic parameters (resistance, capacitance and inductance) need to be extracted from the interconnect geometry. This extraction must be accurate as a correlation with "final" verification engines is needed for design convergence. The extraction must also be efficient, because it may be performed dozens of times on the full-chip level and thousands of times on critical nets. Clearly, numerical extraction is hard to support during iterative procedures of simulation and optimization.

Accurate and efficient extractions for resistance and capacitance have been achieved recently. For example, a 2.5D capacitance extraction methodology was shipped with Cadence Silicon Ensemble 5.0 product[2], and a fast generation of statistically-based worst-case RC models was implemented and used at Hewlett-Packard [1]. Both used the table-based approach, which is suitable for iterative simulation and optimization purposes. Due to increasingly wider and longer wire traces, faster clock frequencies and shorter rising times, inductance effects of on-chip interconnects no longer can be ignored. However, no inductance extraction methodology, which is accurate and efficient for iterative simulation and optimization purposes, has been presented.

In this paper, we describe an efficient and accurate methodology to extract inductance under the PEEC model. In section II, we validate two foundations which allow us to reduce the problem size of inductance extraction without loss of accuracy. In section III, we propose a table-based inductance extraction methodology based on the two foundations. In section IV, we present two applications of the inductance extraction methodology: (i) to derive the effective (loop) inductance for a coplanar-waveguide; (ii) to be integrated with the statistically-based RC model generation in [1] to generate RLC models for on-chip interconnects. We also use the RLC model to optimize bus structures. Section V concludes this paper.

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II. Foundations for Inductance Extraction

A. Preliminaries

There are multiple metal layers in a VLSI technology. We assume that wire traces in adjacent layers are orthogonal, and extract the inductance for a *block*, which contains n traces (T1, T2,..., Tn) of same lengths in the same layer (see Figure 1). In addition, we also assume that the two most outside traces, T1 and Tn, are dedicated ground traces. When the block size is three, it is a coplanar-waveguide, which is one of the three basic forms for transmission line, and is often used for clock tree in high-speed designs. When the block size is large, it models the bus structure with outside ground traces that can be used for shielding only or for shielding and power supply at the same time. Because traces are orthogonal in adjacent layers, traces in layer N+1 and layer N-1 will not affect the inductance of traces in the current layer N [7]. In section V, we will discuss the impacts of layer N+2 and layer N-2.

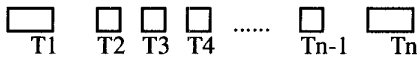

Figure 1:The cross-section view for a block of n traces, where T1 and Tn are dedicated ground traces. The width for each trace is W1, W2,..., and Wn, and spacings are S1, S2,..., Sn.

Note that the capacitive effect is a "short-range" effect in the sense that for a block, only the mutual capacitance between adjacent traces are important, and the rest of the mutual capacitance can be ignored. Therefore, for any trace, it is sufficient to solve the trace and its two adjacent traces via numerical extraction [2]. In other words, we are able to reduce the n-trace capacitance problem to a number of 3-trace subproblems. The inductive effect, however, is a "long-range" effect. For example, in Figure 2, we compute the inductance for a block with size n=5 by assuming that the wire thickness is 2.0um, wire width W1=4um, W2=W3=W4=0.8um, W5= 2um, and all spacings are 0.8um. We specify that T1 and T5

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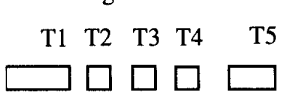
are ground traces, and run a 3D inductance tool RI3 in Raphael [3] to compute loop inductance. The result is a 3x3 matrix because the inductance is defined with respect to ground traces. In the matrix, diagonal elements are self inductance, and off-diagonal elements are mutual inductance. The mutual inductance between T2 and T4 can not be ignored even though there is T3 between them.

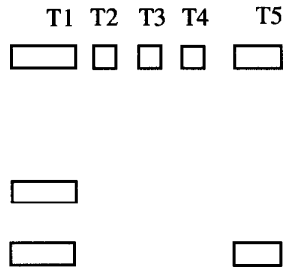


$$\begin{array}{c} \\ T2 \\ T3 \\ T4 \end{array} \begin{bmatrix} 1.73 & 1.15 & 0.53 \\ 1.15 & 1.94 & 1.24 \\ 0.53 & 1.24 & 1.92 \end{bmatrix}$$

Figure 2:Loop inductance (nH) for a block of size n=5 by specifying that T1 and T5 are ground traces. The trace length is 4000um.

In general, there is a significant mutual inductance between any traces within a block (e.g., for a block of size n=32). Due to this "long-range" effect, even though we assume that all signal traces have an identical width, and the spacings are identical, the brute-force way to build inductance tables will have large table sizes.The table for self inductance has six dimensions: two widths for ground traces, one width for signal traces, the trace location, and uniform spacing and length. Note that the trace length is needed because the inductance is *not* a linear function of trace length. At the same time, the table for mutual inductance needs locations for two traces, which leads to seven-dimension tables. We may not afford to consider different widths and spacings for different traces.

Furthermore, the loop inductance in Figure 2 assumes that all current returns via the two ground traces, which may not be true for the high frequency(e.g., when only one trace is switching, its current may return from adjacent quiet traces). The right way to extract inductance for a block is to run RI3 without specifying ground traces. Then, for the block in Figure 2, we obtain a 5x5 matrix (see Figure 3(a)). Again, the diagonal elements are self inductance, and off-diagonal elements are mutual inductance. An important observation is that now the self inductance of a trace depends only on the



$$\begin{array}{c} \\ T1 \\ T2 \\ T3 \\ T4 \\ T5 \end{array} \begin{bmatrix} 6.17 & 5.43 & 5.12 & 4.89 & 4.66 \\ 5.43 & 6.79 & 6.10 & 5.48 & 5.04 \\ 5.12 & 6.10 & 6.79 & 6.10 & 5.33 \\ 4.89 & 5.48 & 6.10 & 6.79 & 5.77 \\ 4.66 & 5.04 & 5.33 & 5.77 & 6.50 \end{bmatrix} \quad (a)$$

$$\begin{array}{c} T1 \end{array} \begin{bmatrix} 6.17 \end{bmatrix} \quad (b)$$

$$\begin{array}{c} T1 \\ T5 \end{array} \begin{bmatrix} 6.17 & 4.66 \\ 4.66 & 6.50 \end{bmatrix} \quad (c)$$

Figure 3: Partial inductance (nH) for (a) a block of size n=5 without specifying ground traces, (b) trace T1 only, and (c) two traces T1 and T5.

trace itself, and the mutual inductance of two traces depends only on the two traces themselves. For example, in Figure 3(b), we compute the self inductance L_{11} for T1 with other traces removed, and obtain the same L_{11} as in Figure 3(a). In Figure 3(c), we compute the mutual inductance L_{15} for T1 and T5 with T2, T3 and T4 removed, and obtain the same L_{15} as in Figure 3(a).

When we do not specify which traces are ground traces, we compute partial inductance (denoted as L_P) under the PEEC model[1]. In general, we have the following foundations:

Foundation 1 Self Lp of a trace is *solely* decided by the trace (its length, width and thickness).

Foundation 2 Mutual Lp of two traces is *solely* decided by the two traces (their lengths, widths and thicknesses, and the spacing between them).

B. Validation of foundations

In order to validate the two foundations, the following illustrates the inductance extraction procedure under the PEEC model. The PEEC model was introduced in [4,5], and has been widely used in numerical inductance extraction tools (for example, [3,6]). Because the inductance is defined only for closed loops, the partial inductance of a trace can be viewed as the inductance of the trace as it forms a loop with infinity. If the current density is uniform in traces T_k and T_m, the mutual inductance under the PEEC model, Lp_{km} is [4]:

$$Lp_{km} = \frac{\mu}{4\pi}\frac{1}{a_k a_m}\int_{b_k}^{c_k}\int_{a_k}^{c_m}\int_{b_m}^{}\int_{a_m}^{} \frac{dl_k \bullet dl_m}{r_{km}} da_k da_m \qquad (1)$$

where a_k and a_m are cross-sectional areas, b_k and $b_m$are starting points, c_k and c_m are ending points, all for traces T_k and T_m, respectively. In addition, r_{km} is the distance between dl_k and dl_m, which represent differential elements of length of traces T_k and T_m. When k=m, (1) gives the self Lp of a trace.

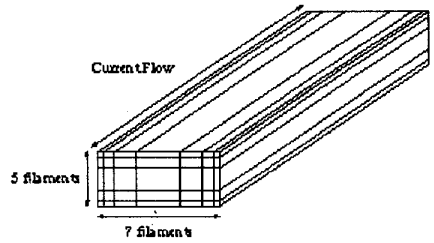


Figure 4:A trace is divided into 5x7 filaments.

In the case where the current is not uniform in a trace, a trace can be divided into rectangular filaments (see Figure 4). The current is assumed to flow along the length of each filament with a constant density within each filament. Therefore, (1) may be used for each filament. It is easy to see that Foundations 1 and 2 hold for each filament with respect to (1). I.e., the self Lp of a filament is solely decided by the filament, and the mutual Lp between two filaments is solely decided by the

1. In section IV, we will show how to generate the effective loop inductance from the partial inductance, using the coplanar waveguide as an example.

two filaments. The conclusions hold for cases of a single trace and multiple traces.

If we assume that trace T_k has P filaments, and trace T_m Q filaments, then Lp_{km} is given by

$$Lp_{km} = \sum_{i=1}^{P} \sum_{j=1}^{Q} Lp_{ij} \quad (2)$$

where Lp_{ij} is the mutual Lp between filament i of Tk and filament j of Tm. Again, when k=m, (2) computes the self Lp for a trace. It is easy to see that foundations 1 and 2 still hold after using (2) to compute Lp for traces.

III. Table-based Inductance Extraction

The two foundations enable us to reduce the n trace inductance problem into 1-trace subproblems to solve the self L_p, and into 2-trace subproblems to solve the mutual Lp. There is *no* loss of accuracy during the reduction.

As given in [8], the self inductance may be solved by

$$L(nH) = 2l \times \left[\ln\left(\frac{2l}{w+t}\right) + 0.5 - k\right], \quad (3)$$

where $k = f(w,t)$ and $0 < k < 0.0025$, and l, w, and t are length, width and thickness of the trace in unit of *cm*. The mutual inductance for two traces of same width and length is

$$L(nH) = \frac{\mu_o l}{2\pi}\left[\ln\left(\frac{2l}{s}\right) - 1 + \frac{s}{l}\right] \quad (4)$$

where s is spacing between two traces, again in unit of *cm*.

These equations give us two insights: First, the inductance for on-chip interconnects is *not* linearly scalable. Both self and mutual inductance are super-linear functions of the trace length. Secondly, because of the logarithmic operation of l/w and l/s, both mutual and self inductance is less sensitive to variations of trace width and spacing as the capacitance and resistance are. The two insights are also verified by experiments with numerical inductance tools. The second insight enables us not to consider the impact of process variation for inductance extraction, even though the impact must be considered for resistance and capacitance extractions [1].

There are limitations of applying the two equations however. First, they do not consider the skin depth and internal inductance[1];Second, widths are not considered for mutual inductance. Therefore, we propose to build tables via numerical inductance extraction for self and mutual inductance.

There are two parts in the table-based inductance extraction. One is to pre-compute inductance tables. We assume that each layer has a nominal thickness, and build tables for different layers. The self inductance table has two dimensions: width and length. The mutual inductance table has three dimensions: widths for two traces and the spacing between them. The 3D inductance extraction tool RI3 is invoked to solve a block of two traces for different combinations of lengths, widths, and spacings. The resulting self and mutual inductance is stored in tables. Note that only 2-trace subproblems need to be solved, because results to 1-trace subproblems are parts of results to 2-trace subproblems. In addition, the inductance depends on the skin depth, which is a function of frequency. We run RI3 under the significant frequency. The significant frequency is defined as $0.17/t_r$, where t_r is the minimum rising/falling time [7].

The other part of the table-based inductance extraction is table lookup.For each trace in a block, we obtain a self inductance from tables for a given layer, length and width. For any combination of two traces Ti and Tj, we obtain a mutual inductance from tables for a given layer, widths, and spacing between Ti and Tj. A bicubic spline algorithm [9] will be used to compute inductance that is not given in the table.

IV. Applications of Inductance Model

A. L_{eff} for coplanar-waveguide

The coplanar-waveguide structure (a block of size n=3, see Figure 5) is often used for on-chip clock trees in high-speed designs. Not to consider the inductive effect will lead to a significant underestimate of delay and noise. Therefore, the effective loop inductance (L_{eff}) of the signal trace needs to be computed in order to use the transmission line theory. In the following, we derive L_{eff} as a function of Lp for the three traces T1, T2 and T3, where T2 is the signal trace, and T1 and T3 coplanar ground traces.

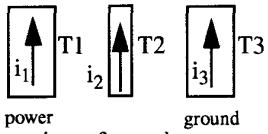


Figure 5: The top view of a coplanar-waveguide

L_{eff} is defined for the current loop that has two segments: the first segment is current i_2 through T2; the second segment has two parallel branches, i.e., i_1 through T1 and i_3 through T3. According to the definition of L_{eff}, we have

$$\Delta V = L_{eff} \cdot \frac{di_2}{dt} = Lp_{22} \cdot \frac{di_2}{dt} + Lp_{21} \cdot \frac{di_1}{dt} + Lp_{23} \cdot \frac{di_3}{dt} \quad (5)$$
$$-Lp_{11} \cdot \frac{di_1}{dt} - Lp_{12} \cdot \frac{di_2}{dt} - Lp_{13} \cdot \frac{di_3}{dt},$$

and the two ground traces have the same voltage drop

$$Lp_{11} \cdot \frac{di_1}{dt} + Lp_{12} \cdot \frac{di_2}{dt} + Lp_{13} \cdot \frac{di_3}{dt} \quad (6)$$
$$= Lp_{13} \cdot \frac{di_1}{dt} + Lp_{23} \cdot \frac{di_2}{dt} + Lp_{33} \cdot \frac{di_3}{dt},$$

finally, the current are conservative according to KCL

1. The RC2 and RC3 in Raphael [3] do not consider the internal inductance, and therefore are not capable of extracting on-chip inductance.

$$i_1 + i_2 + i_3 = 0 \quad (7)$$

L_{eff} can be derived by simultaneously solving (5)-(7). When T1 and T3 are symmetric with respect to T2, L_{eff} is

$$L_{eff} = Lp_{22} - 2Lp_{23} + \frac{Lp_{11}}{2} + \frac{Lp_{13}}{2} \quad (8)$$

Experiments show that (8) using our partial inductance tables gives results very close to L_{eff} obtained by 3D extractions using RI3. In general, under the assumption that all current returns within the block, we may solve the L_{eff} for trace Tj in the block of size n using the following n equations: one equation based on the definition of L_{eff} for Tj like (5), N-2 equations (like (6)) based on KVL that all traces (other than Tj) have equal voltage drop, and one equation like (7) based on KCL that the total current is conservative.

B. Bus optimization

We also have integrated the table-based inductance model with the statistically-based RC model [1] to obtain the RLC model for on-chip interconnects. As discussed in section III, we do not need to consider the impact of process variations for inductance, but we do consider the impact for resistance and capacitance [1]. In addition, because of the assumption that traces in adjacent layers are orthogonal, there is no need to consider the mutual inductance between traces in layer N and those in layer N+1 or N-1. At the same time, trace densities in layers N+1 and N-1 are considered during capacitance extraction for traces in layer N. The resulting RLC model is represented as the SPICE netlist. The current return path will be determined automatically by SPICE.

In the following, we apply the RLC model to optimize a bus structure with 18 signal traces, and two fat power-traces outside the signal traces. For all traces, the wire length is 2000um, thickness 2.0um, and spacing 0.8um. The width is 0.8um for all signal traces, and 16um for fat power-traces. We also assume the following signal pattern: all signal traces are simultaneously switching up with rising time of 80ps, except that one of the two central signal traces is the quiet victim. For all traces, the driver is 130x of the minimum inverter in a representative 0.18um CMOS technology, and the receiver 40x of the minimum inverter. We measure the noise at the far-end of the victim trace (the input node of receiver) via SPICE simulation. In order to control noise, we will insert shielding traces, which are dedicated AC-ground traces with similar widths as the signal traces. Our objective is to make the far-end noise less than 0.25V.

When there is no shielding traces, the noise of victim trace is 0.71V. Then, we insert a shielding trace for every six signal traces, and increase the width Ws for shielding traces from 0.8um to 2.4um. The noise is 0.22V with Ws=2.4um. Finally, we insert a shielding trace for every three traces. The noise is 0.17V when Ws=0.8. Detailed results using SPICE and our RLC model are presented in Table 1.There is a clear trade-off between area and noise: we may reduce the noise by a factor of 4.2x while the total routing area is increased by 13%, and the total wire area is increased by 8.8%.

Ns	Ws	Noise(V)	routing area(um)	wire area(um)
18	--	0.71	61.6	46.4
6	0.8	0.38	64.8	48.0
6	1.6	0.27	66.4	49.6
6	2.4	0.22	68.0	51.2
3	0.8	0.17	69.6	50.4

TABLE I Comparison between different shielding insertion solutions. Column one (Ns) is the number of signal traces between two ground(shielding) traces, and column 2 (Ws) is the width for the shielding traces. Column 3 is the total routing area of the bus structure, and column 4 is the total wire area.

V. Discussions and Conclusions

In this paper, we have presented a table-based inductance extraction methodology. We also have applied it to compute L_{eff} for coplanar-waveguide, and to generate RLC models for on-chip interconnects. The RLC model has been used to optimize bus structures via SPICE simulations.

However, our inductance model considers traces only in one layer. It is believed that for traces in layer N, the current return path via layer N+2 or N-2 has a very high impedance, therefore the lion's share of the current returns via loops in the same layer. In addition, layers N+2 and N-2 are statistically quiet. Therefore, it is acceptable to consider only layer N. Further study on the impact of layer N+2 and N-2 is planned.

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