Modeling and Layout Optimization for On-chip Inductive Coupling*

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Abstract

In this paper, we study the modeling and layout optimization for on-chip interconnect structures to minimize the inductive coupling. We first investigate the characteristics of mutual (as well as self) inductance for coplanar, micro-stripline, and stripline structures, and examine the effectiveness of design freedoms such as wire sizing, spacing, and shielding. We then propose formula-based k_{eff} models as the figures of merit for inductive coupling in the three interconnect structures, and apply the proposed models to automatically synthesize on-chip interconnect structures. Experiments show that compared to the coupling coefficients computed by a numerical field solver, the k_{eff} models have about 15% difference for coplanar structures, and have negligible difference for micro-stripline and stripline structures. In addition, interconnect structures meeting given noise specifications can be synthesized instantly using proposed k_{eff} models.

*This work makes use of machines donated by Intel, whose generous donation is greatly appreciated. Related works and update on this work can be found at http://eda.ece.wisc.edu.

1 Introduction

As we move into gigahertz circuit designs in nanometer technologies, on-chip inductance becomes more and more important due to the longer wires, shorter rise times, and lower resistive wires (caused by relatively thicker and wider wires on top metal layers and the use of copper to replace aluminum). Therefore, modeling and layout optimization for on-chip inductance have been drawing increasingly more attentions. The inductance models can be classified into the following categories: (i) numerical based inductance extraction such as [1][6][2] that are accurate, but are too expensive to be used for the full-chip level, and (ii) formula or table based inductance extraction such as [7][4] that are reasonably accurate and efficient enough to be used for full-chip level timing analysis and simulation. However, all aforementioned methods do not provide enough insights to guide the layout design. Even though we may apply iterative layout, extraction, simulation based on these methods to achieve an optimal layout design, we can not afford this iterative procedure for most designs.

The characteristics of on-chip self inductance have been studied recently in [9], and a few layout techniques have been examined. However, without considering mutual inductance, the resulting layout designs might be far away from the optimal. In this paper, we study the modeling and layout optimization to minimize the inductive coupling. We first investigate the characteristics of on-chip mutual inductance (as well as self) for coplanar, micro-stripline and stripline structures. With respect to the on-chip inductive coupling, we also examine impacts of layout design freedoms, such as wire sizing, spacing, and shielding. We then propose efficient k_{eff} models for the on-chip inductive coupling, which can be used as figures of merit to guide layout optimization. We finally apply the proposed models to synthesize min-cost on-chip interconnect structures to meet the noise specifications. This paper is part of our efforts to develop an integrated set of models and algorithms for interconnect planning and optimization under accurate RLC models for giga-scale system-on-chip designs. Furthermore, as part of the efforts, the proposed k_{eff} model for coplanar structures has been used to study the simultaneous shielding insertion and net ordering problem to minimize both capacitive and inductive coupling [5].

The remainder of this paper is organized as follows: we study the coplanar interconnect structure in Section 2, and the micro-stripline and stripline structures in Section 3. Formula-based k_{eff} models are developed for the two interconnect structures in the two sections. We then apply the k_{eff} models to synthesize 64-bit wide bus structures in Section 4, and verify the synthesized interconnect structures via the numerical inductance extraction tool FastHenry[6]. We conclude the paper in Section 5.

2 Coplanar Structures

2.1 Characteristics of Inductance

In this section, we consider parallel wires of the same length in the same layer. In addition to the *signal wire* (in short, *s-wires*), there are other two types of coplanar wires. One type is *power/ground grids* (in short, *P/G grids*), and the other type is *shielding wires* (in short, g-*wires*). P/G grids are often much wider than s-wires, on the other hand, g-wires often have similar widths as s-wires, and are directly connected to P/G grids. As shown in Figure 1, two edge wires labeled by P and G are part of the power and ground grids, wires labeled by s are signal wires, and wires labeled by g are shielding wires.

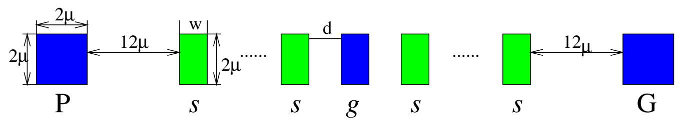

Figure 1: The cross-section view of a coplanar interconnect structure. P and G stand for wires of P/G grids, s stands for signal wires, and g stands for shielding wires.

In experiments in the section, we assume that all s-wires and g-wires have the same width w, either $0.8\mu m$ or $1.6\mu m$, and the edge-to-edge space d between s-wires and g-wires is uniform, either $0.8\mu m$ or $1.6\mu m$. As shown in Figure 1, we assume the distance between P/G grids and the edge s-wire is $12\mu m$, and the width of the P/G grids is $2\mu m$. The thickness of all wires is $2\mu m$, which is a typical thickness for global interconnects like those in strawman technologies [10]. Unless specified, the length for those wires is $2000\mu m$.

The coplanar structure we study contains 18 s-wires, which from left to right are numbered from 1 to 18. We call the group of s-wires sandwiched by a pair of adjacent g-wires or P/G grids as a *block*, and the number of s-wires in a block as the *block size*. When there is no g-wire, the 18 s-wires within the P/G grids can be represented by $P18sG$. If we insert one g-wire uniformly within the s-wires, the coplanar structure can be represented by $P9sg9sG$. Similarly, if we uniformly insert two and five g-wires among those s-wires, respectively, we can represent the coplanar structure by $P6sg6sg6sG$ (or in short, $P(6sg)^2 6sG$) and $P(3sg)^5 3sG$, respectively. To consider the impact of P/G grids and g-wires (as well as P/G planes later on), we computed the *loop inductance* by the numerical inductance extraction tool FastHenry in this paper. In addition, we assume that unless otherwise specified, the clock frequency of the target design is $3GHz$, and set the significant frequency [8] as $30GHz$ when we run FastHenry. In the following, we first study coplanar structures without shielding wires, then coplanar structures with shielding wires.

2.2 Coplanar Structures without Shielding Wires

We study the inductance for the $P18sG$ structure without any g-wire. Figure 2 shows the self inductance of the first s-wire (wire 1) and the mutual inductance between it and other s-wires. Clearly, the mutual inductance is significant when compared to the self inductance. The mutual inductance between wire 1 and wire 2 is 77% of the self inductance of wire 1. This means the noise and delay induced by mutual inductance are substantially important. Moreover, even though it is well accepted that the value for coupling capacitance between non-adjacent wires is insignificant, it is not true for coupling inductance. Although the mutual inductance decreases for non-adjacent s-wires, the mutual inductance between wire 1 and wire 3 is still 65% of the self inductance for wire 1, and is still 80% of the mutual inductance between wire 1 and wire 2. Therefore, we can not ignore the mutual inductance between non-adjacent wires, either.

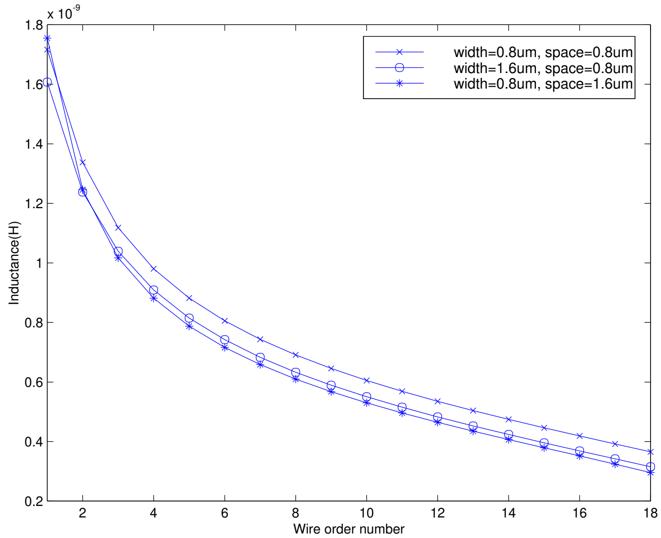

Figure 2: Self and mutual inductance for the wire 1 in the $P18sG$ coplanar structure.

In addition, the loop inductance is not sensitive to wire sizing and spacing. As shown in Figure 2, when we double the wire width from $0.8\mu m$ to $1.6\mu m$, the total width of the $P18sG$ structure is increased by 149%. However, the self inductance of wire 1 is decreased only by 10%, and the mutual inductance between wire 1 and other s-wires is decreased by from 7% to 14%. When we double the space from $0.8\mu m$ to $1.6\mu m$, the total width is increased by 151%. However, the self inductance of wire 1 is even increased by 2% (due to being moved further away from the P/G grids), and the mutual inductance between wire 1 and any other s-wire is decreased by from 7% to 19%.

2.3 Coplanar Structures with Shielding Wires

We study the inductance for 18 s-wires when g-wires are inserted among them. As shown in Figure 3, when g-wires are inserted, all inductance (both self and mutual) decrease. If we insert one g-wire ($P9sg9sG$ in the figure), compared to the inductance for $P18sG$, self inductance is reduced by 15%, total mutual inductance (the sum of all mutual inductance with respect to wire 1) is reduced by 49%, and the total width increases only by 5%. When we insert more g-wires, as shown by $P(6sg)^2 6sG$ and $P(3sg)^5 3sG$ cases in Figure 3, the self inductance of wire 1 is respectively reduced by 22% and 37%, and total mutual inductance is respectively reduced by 69% and 89%. The increase of the total width for the interconnect structure is only 11% and 28%, respectively.

For those s-wires that are separated by the g-wires, Figure 3 shows that the mutual inductance between them is very small, if it is not negligible. The maximum mutual inductance outside the block is only 8% of the maximum mutual inductance within a block. Therefore we are able to assume the inductive effects are mainly limited inside each block

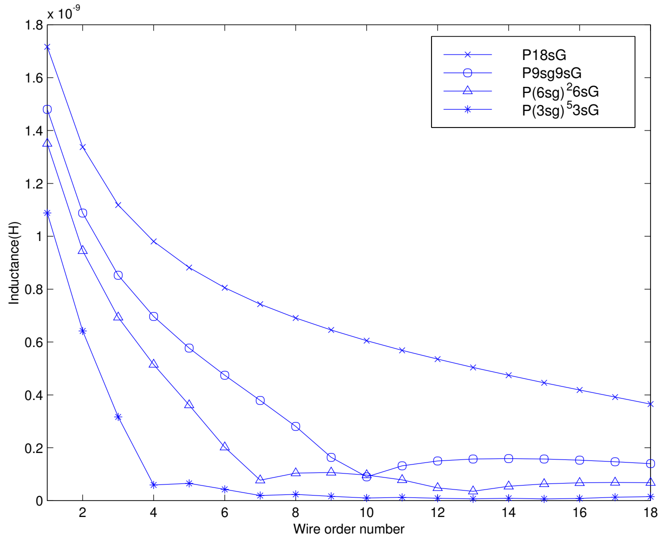

Figure 3: Self and mutual inductance for wire 1 in the $P18sG$, $P9sg9sG$, $P(6sg)^2 6sG$ and $P(3sg)^5 3sG$ coplanar structures.

without losing much accuracy.

Given the above studies, we conclude that compared to wire sizing and spacing, shielding is much more effective to reduce inductance, especially mutual inductance. To guide the interconnect structure synthesis using shielding, we will develop an effective coupling model in next subsection.

2.4 Effective Coupling Model

For any two given s-wires i and j, the coupling coefficient k_{ij} between them is defined as:

$$k_{ij} = \frac{L_{ij}}{\sqrt{L_{ii} \times L_{jj}}} \tag{1}$$

where L_{ii} and L_{jj} is self inductance of wire i and j, and L_{ij} is mutual inductance between them. It is well known that k_{ij} provides the first-order approximation for the coupling between two s-wires.

We propose the following model to approximate k_{ij}. When wire i and j are in different blocks, k_{ij} is zero[1]. When wire i and j are in a same block, we first computer intermediate functions f and g (defined below), then obtain the coupling coefficient k_{ij} as the mean of $f(i)$ and $g(j)$.

We use Figure 4 to illustrate how to compute k_{ij}. Let g_l and g_r be the g-wires or P/G grids bounding a block, and N_{gl}, N_i, N_j and N_{gr} be the ordering of those four wires from left to right. We assume $f(g_l) = g(g_r) = 0$, and $f(j) = g(i) = 1$. If $N_i \leq N_j$, we define $f(i) = \frac{N_i - N_{gl}}{N_j - N_{gl}}$, and $g(j) = \frac{N_{gr} - N_j}{N_{gr} - N_i}$. Then, we compute the coupling coefficient $k_{ij} = \frac{f(i)+g(j)}{2}$. We call this model for the coupling coefficient as effective coupling model, denoted as k_{eff} model.

[1]Here, k_{ij} can be also approximated by a small constant.

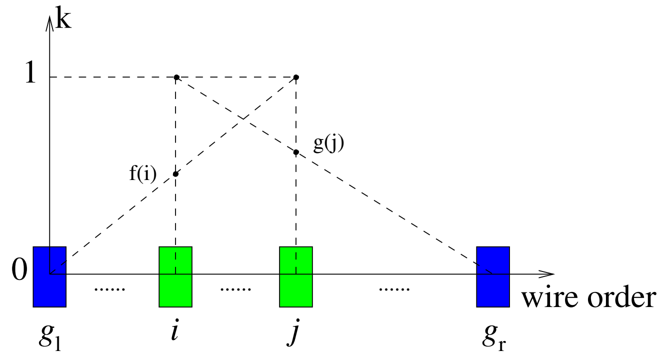

Figure 4: Cross-section view of a block.

The k_{eff} model is independent of the width and length of s- and g-wire. In order to validate this simplification for width and length, we compute k_{ij} of $P(6sg)^2 6sG$ structure via FastHenry in Table 1. We use three combinations of wire width and length. Compared with the first row in the table, when we change the wire length from $2000\mu m$ to $1000\mu m$ (see row 2 in the table), the maximum difference for k_{ij} is only 3%. When we change the wire width from $0.8\mu m$ to $1.6\mu m$ (see row 3 in the table), the maximum difference for k_{ij} is only 2.6%. Therefore, the coupling coefficient k is not sensitive to wire width and length.

Width, space and length(μm)	k_{12}	k_{13}	k_{14}	k_{15}	k_{16}
$w = 0.8, d = 0.8, l = 2000$	0.71(0%)	0.53(0%)	0.41(0%)	0.31(0%)	0.21(0%)
$w = 0.8, d = 0.8, l = 1000$	0.72(1.0%)	0.54(1.8%)	0.42(2.3%)	0.32(2.7%)	0.22(3.0%)
$w = 1.6, d = 0.8, l = 2000$	0.71(0.4%)	0.54(1.9%)	0.42(2.3%)	0.32(2.3%)	0.21(2.6%)

Table 1: Coupling coefficients between the wire 1 to other s-wires inside a block for the $P(6sg)^2 6sG$ structure.

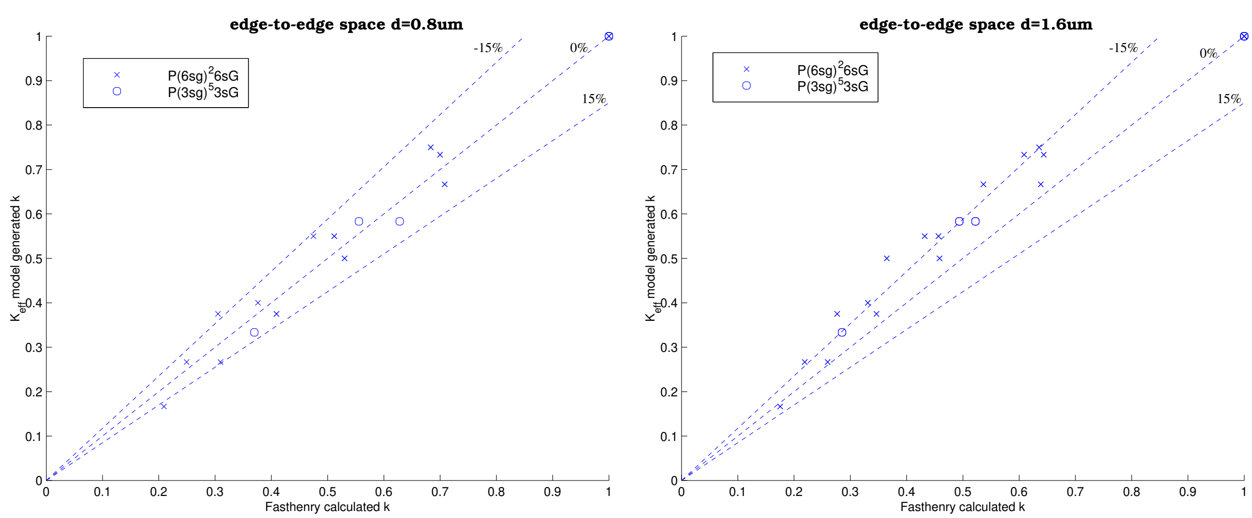

Figure 5: Comparison between coupling coefficients obtained by k_{eff} model and FastHenry.

In order to verify our model with respect to the space between wires and to further exam the accuracy of it, we compare k_{ij} computed by FastHenry and our k_{eff} model in Figure 5. In the figure, x-axis is coupling coefficient given by FastHenry and y-axis is coupling coefficient given by the k_{eff} model. Two structures are used: $P(6sg)^2 6sG$ and $P(3sg)^5 3sG$. Three dashed lines stand for difference of 0%, 15% and -15%, respectively. When $d = 0.8\mu m$, most of the points lie within the $\pm 15\%$ error range. At the same time, most of those k_{ij} calculated by the k_{eff} model are larger than those calculated by FastHenry. Therefore the k_{eff} model tends to be conservative and is safe to be used in designs. Furthermore, when the block size decreases from 6 to 3, the error of the k_{eff} model is reduced. It implies that our model has higher accuracy when block size is smaller. When $d = 1.6\mu m$, the k_{eff} model is more conservative compared to the model in $d = 0.8\mu m$. Hence, it is safe to assume that the k_{eff} model is independent of spacing. The k_{eff} model will be used in Section 4 to synthesize coplanar interconnect structures.

3 Stripline and Micro-stripline Structures

3.1 Characteristics of Inductance

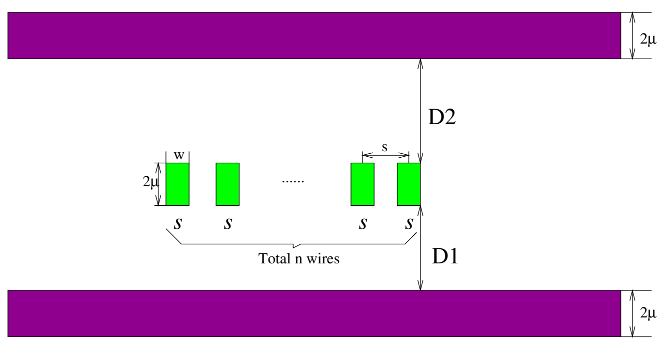

Figure 6: Cross-section view of stripline structure.

In this section, we study the micro-stripline and stripline structures, where power/ground planes (in short, *P/G planes*) are used as current return path for s-wires. When there is only one P/G plane, it is a *micro-stripline* structure. When there are two P/G planes, it is a *stripline* structure. As shown in Figure 6, if there are n s-wires in a stripline structure, it may be represented by (D_1, ns, D_2), where D_1 is the surface-to-surface distance between the lower P/G plane and the signal layer, and D_2 is the surface-to-surface distance between the upper P/G ground plane and the signal layer. Similarly, a micro-stripline with n s-wires can be represented by (D, ns), where D is the surface-to-surface distance between P/G plane and signal layer in the structure. We use $0.10\mu m$ technology of the strawman technologies [10] in this section. The thickness for both signal and P/G layers is $2.0\mu m$, and the ILT (i.e., Inter-Layer Thickness) between adjacent metal layers is $1.4\mu m$. Therefore, if the P/G plane in a micro-stripline structure is two-layer away from the signal layer and there are 18 s-wires, the interconnect structure can be represented by $(4.8\mu m, 18s)$. We consider *pitch-space* (i.e., the center-to-center space) between s-wires, which is different from the edge-to-edge space d used in Section 2. In the following, we first study the effects of P/G planes and the distance between the signal layer and P/G planes, and then investigate the impacts of the width of P/G planes and the wire sizing and spacing of the signal wires.

3.1.1 Effects of Ground Plane

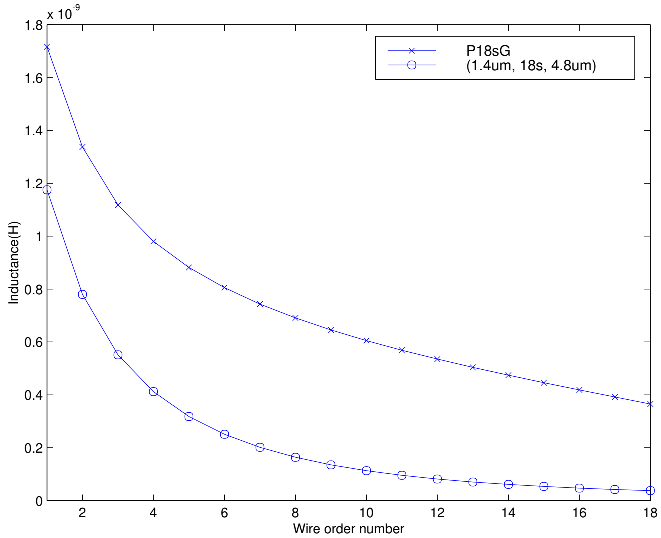

Figure 7: Self and mutual inductance for leftmost s-wire in coplanar structure $P18sG$ and in stripline structure $(1.4\mu m, 18s, 4.8\mu m)$.

We first compare the two following structures, $P18sG$ coplanar structure, and the stripline structure $(1.4\mu m, 18s, 4.8\mu m)$. For both structures, the wire width is $0.8\mu m$ and the pitch-space is $1.6\mu m$. For stripline structure, the P/G plane width is $2000\mu m$, which is sufficient for current returning at $30GHz$ (see experiments in Section 3.1.2 later on). As shown in Figure 7, compared to the inductance for the coplanar structure, self and total mutual inductance for the stripline structure is reduced by 32% and 70%, respectively.

To investigate the difference between micro-stripline and stripline structures, we compare the following three structures: micro-stripline structure $(1.4\mu m, 18s)$, stripline structure $(1.4\mu m, 18s, 4.8\mu m)$ and stripline structure $(1.4\mu m, 18s, 1.4\mu m)$. The width of all P/G planes is $2000\mu m$. For the stripline structure (D_1, ns, D_2) and micro-stripline structure (D_1, ns), if $D_1 < D_2$, we define that (D_1, ns) is a *reduced micro-stripline structure* of (D_1, ns, D_2). For example, micro-stripline $(1.4\mu m, 18s)$ is a reduce micro-stripline structure of stripline structure $(1.4\mu m, 18s, 4.8\mu m)$ and $(1.4\mu m, 18s, 1.4\mu m)$. Figure 8 shows the self and mutual inductance of the leftmost s-wire in the three interconnect structures. We observe the following:

First, both self and mutual inductance will be reduced when there are more P/G planes presented. Compared to the micro-stripline structure $(1.4\mu m, 18s)$, self and total mutual inductance of the leftmost s-wire in the stripline structure $(1.4\mu m, 18s, 1.4\mu m)$ are reduced by 19% and 54%, respectively.

Second, the shielding effect of ground plane is mainly determined by the nearest ground plane, because most of the current in s-wires returns from the closest P/G plane. That is demonstrated by the fact that for the self and mutual inductance of

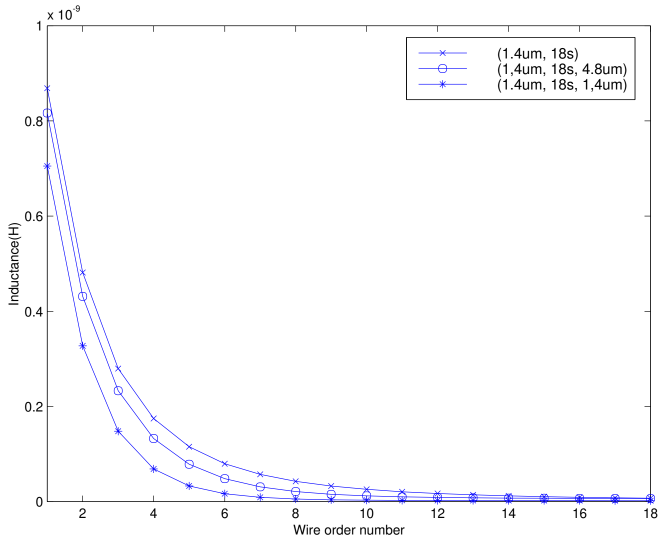

Figure 8: Self and mutual inductance for leftmost wire in micro-stripline structure and stripline structures.

the leftmost wire there is only 6% and 23% differences between the stripline structure $(1.4\mu m, 18s, 4.8\mu m)$ and its reduced micro-stripline structure $(1.4\mu m, 18s)$. Also, both self and mutual inductance of the reduced micro-stripline structure are larger than those of its corresponding stripline structures.

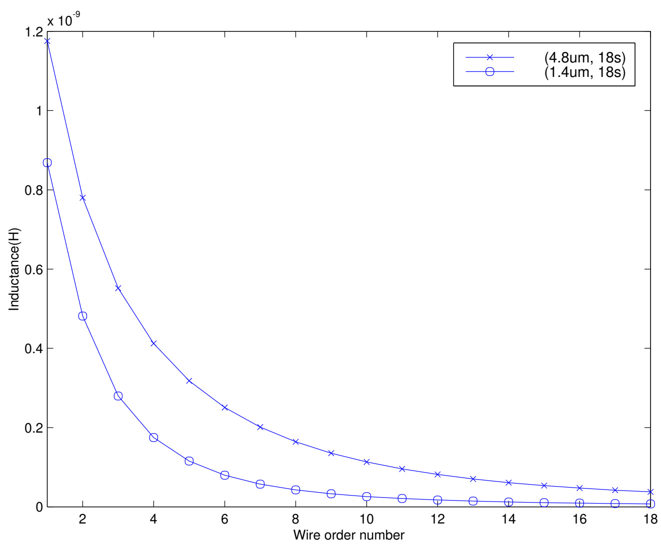

Figure 9: Self and mutual inductance for leftmost wire in micro-stripline structures $(1.4\mu m, 18s)$ and $(4.8\mu m, 18s)$.

Furthermore, we study the impacts of the distance between the P/G plane and the signal layer. We use two micro-stripline structures $(1.4\mu m, 18s)$ and $(4.8\mu m, 18s)$, where the P/G plane is one-layer and two-layer away from the signal layer, respectively. As shown in Figure 9, when the P/G plane is one-layer away, the self and total mutual inductance of the leftmost wire are 26% and 59% smaller, compared to the case where the P/G plane is two-layer away. Therefore, the distance between the P/G plane and the signal layer has great impact on inductance.

3.1.2 Effects of P/G Plane Width

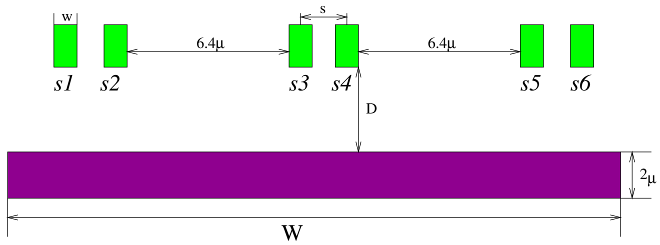

Figure 10: Cross-section view of a micro-stripline structure for $W = 5, 10, 15, 20, 25, 30, 35, 40, 45, 200\mu m$

To study the impacts of the P/G plane width, we consider the micro-stripline structure shown in Figure 10, where from left to right, wires are $s1$ to $s6$, respectively. We assume that all wires are $0.8\mu m$ wide, and the pitch-space between $s1$ and $s2$, between $s3$ and $s4$, and between $s5$ and $s6$ is $1.6\mu m$. The edge-to-edge space between $s2$ and $s3$, as well as that between $s4$ and $s5$, is $6.4\mu m$. The total width of the signal layer is $20\mu m$. Keeping the micro-stripline structure symmetric, we shrink the width of plane W, from $200\mu m$ to $5\mu m$ at step of $5\mu m$, and observe the changes of L_{12} and L_{34}, where L_{12} is the mutual inductance between wire $s1$ and $s2$, and L_{34} the mutual inductance between wire $s3$ and $s4$.

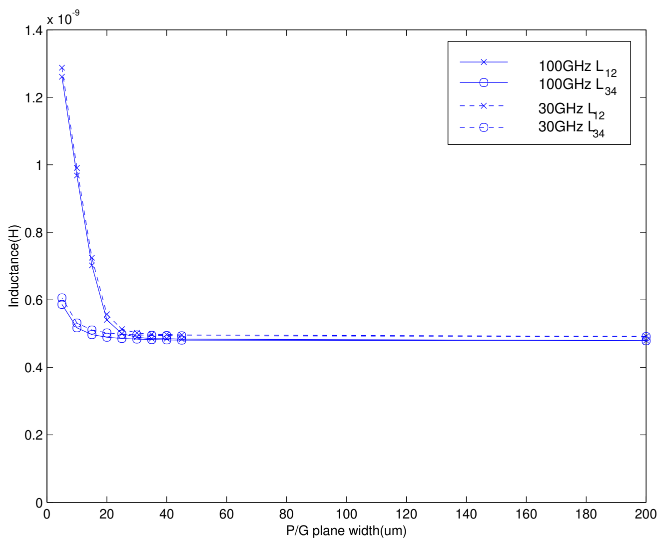

Figure 11: Mutual inductance L_{12} and L_{34} of different P/G plane widths and frequencies.

As shown in Figure 11, the inductance curve is flat when the P/G plane width is large enough. However, when the P/G plane width is shrunk close to the total width of the bus structure ($20\mu m$ in this experiment), L_{12} and L_{34} are increased quickly. This overall trend is independent of the frequency.

Let T be the total width of the signal layer, and D be the surface-to-surface distance between the P/G plane and the signal layer. We propose that the P/G plane width $W = T + 2 \times D$ is sufficient and provides a nice tradeoff between silicon area and the shielding quality. As shown in Table 2, the mutual inductance of $W = T + 2D$ are at most 6.5% larger than the mutual inductance of $W = 200\mu m$. On the other hand, if we use the P/G plane width $W = T$, the mutual inductance is up to 16.7% larger.

D between layers	Inductance(nH)	$W = 200\mu m$	$W = T + 2D$	$W = T$
$D = 1.4\mu m$	L_{12}	47.88	51.00(6.5%)	53.94(12.7%)
	L_{34}	47.66	48.41(1.6%)	48.62(2.0%)
$D = 4.8\mu m$	L_{12}	77.97	82.87(6.3%)	91.14(16.9%)
	L_{34}	77.70	80.39(3.5%)	82.94(6.7%)

Table 2: L_{12} and L_{34} for different P/G plane width.

3.1.3 Effects of Wire sizing and Spacing

To study the impacts of wire sizing and spacing, we change the wire width of the micro-stripline structure $(1.4\mu m, 18s)$ with P/G plane when the plane width $W = 2000\mu m$. We use pitch-space $s = 3.2\mu m$, and change the wire width from $0.8\mu m$ to $1.6\mu m$ and to $2.4\mu m$, respectively. As shown in Figure 12, the self inductance is reduced by 15% and 28%, respectively. Total mutual inductance, however, only has 0.4% and 7% difference when wire widths are doubled and tripled. It is observed in [3] that mutual loop inductance of two wires is *solely* decided by the two wires (their lengths, widths and thicknesses, and the spacing between them). Our experiments here further show that the wire width has little impacts on the mutual inductance of two wires in micro-stripline and stripline structures, and mutual inductance mainly depends on the pitch-space between two wires. Therefore, spacing, but not wire sizing, is an effective layout freedom to change mutual inductance.

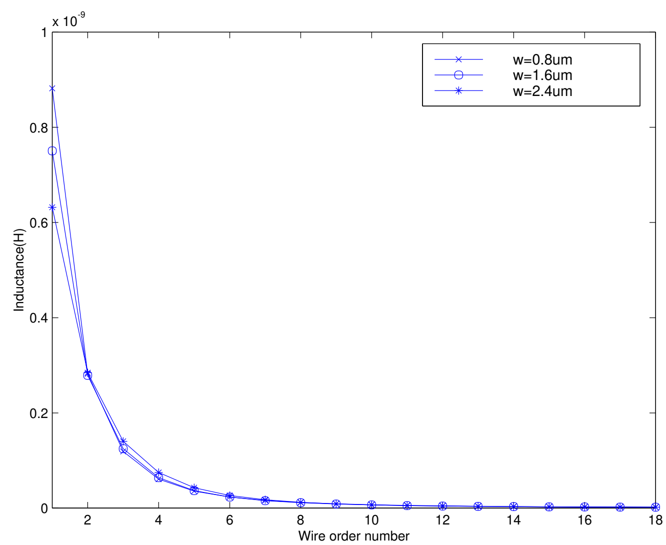

Figure 12: Self and mutual inductance for leftmost wire in $(1.4\mu m, 18s)$ structures, with different wire width.

3.2 Effective Coupling Model

Based on those studies on micro-stripline and stripline structures, we proposed formula (2) to model the coupling coefficient k_{ij} between two wires i and j:

$$k_{ij} = e^{-as^b} \tag{2}$$

where s is the pitch spacing between wire i and wire j, and a and b are constants depending on the wire width[2] and P/G plane distance D. A two-dimension table for a and b (see an example in Table 3) can be built for micro-stripline structure, and a three-dimension table for a and b (see an example in Table 4) can be built for stripline structure. We call (2) as k_{eff} model for micro-stripline and stripline structures.

Distance of P/G plane \ Wire width	$w = 0.8\mu m$	$w = 1.6\mu m$	$w = 2.4\mu m$
$D = 1.4\mu m$	(0.48, 0.74)	(0.39, 0.80)	(0.28, 0.88)
$D = 4.8\mu m$	(0.35, 0.71)	(0.28, 0.76)	(0.20, 0.83)

Table 3: Two dimensional table of (a, b) for micro-stripline structures.

Distance of P/G planes \ Wire width		$w = 0.8\mu m$	$w = 1.6\mu m$	$w = 2.4\mu m$
$D_1 = 1.4\mu m$	$D_2 = 1.4\mu m$	(1.27, 0.23)	(0.45, 0.95)	(0.34, 0.99)
$D_1 = 1.4\mu m$	$D_2 = 4.8\mu m$	(0.72, 0.51)	(0.48, 0.72)	(0.35, 0.77)
$D_1 = 4.8\mu m$	$D_2 = 4.8\mu m$	(0.63, 0.40)	(0.50, 0.50)	(0.37, 0.56)

Table 4: Three dimensional table of (a, b) for stripline structures.

In fact, the k_{eff} model for the reduced micro-stripline structures is a conservative model for the correspondent stripline structures. In Table 5, we compare the k_{ij} of micro-stripline structure $(1.4\mu m, 18s)$, stripline structure $(1.4\mu m, 18s, 1.4\mu m)$ and stripline structure $(1.4\mu m, 18s, 4.8\mu m)$, columns 2-6 are the coupling k_{1j} between the leftmost s-wire and other s-wires in those structures for all $k_{1j} \geq 0.02$. It is clear that the coupling k_{ij} of reduced micro-stripline structure are always larger than those of the stripline structures.

Interconnect Structures	k_{12}	k_{13}	k_{14}	k_{15}	k_{16}
$(1.4\mu m, 18s)$	0.56	0.33	0.20	0.13	0.09
$(1.4\mu m, 18s, 4.8\mu m)$	0.53	0.29	0.16	0.10	0.06
$(1.4\mu m, 18s, 1.4\mu m)$	0.47	0.21	0.10	0.05	0.02

Table 5: Coupling k_{ij} for micro-stripline and stripline structures, when $k_{ij} \geq 0.02$.

Our k_{eff} model is independent of the length of s-wires. To validate this simplification, we compute k_{ij} for different wire lengths via FastHenry in Table 6 for micro-stripline structure $(1.4\mu m, 18s)$. The pitch-space between each wire is $3.2\mu m$, and the wire width is $0.8\mu m$. When we change the wire length from $2000\mu m$ to $1000\mu m$, the maximum difference for k_{ij} is less than 0.4%.

[2] Although the wire width has little impacts on mutual inductance, it affects self inductance and in turn coupling coefficients k_{ij}.

Width and length (μm)	k_{12}	k_{13}	k_{14}	k_{15}	k_{16}
$w = 0.8, l = 2000$	0.32(0%)	0.14(0%)	0.07(0%)	0.04(0%)	0.03(0%)
$w = 0.8, l = 1000$	0.32(0.05%)	0.14(0.22%)	0.07(0.23%)	0.04(0.29%)	0.03(0.37%)

Table 6: Coupling k_{ij} for a micro-stripline structure of different lengths, when $k_{ij} \geq 0.02$.

To exam the accuracy of the k_{eff} model, we compare k_{ij} computed by FastHenry and our k_{eff} model in Figure 13. In Figure 13(a) and Figure 13(b), x-axis is coupling coefficient given by FastHenry and y-axis is coupling coefficient given by the k_{eff} model. Three micro-stripline structures and two stripline structures are used. They all have 18 s-wires, and different combinations of wire width and distance between layers are used. As one can see from the figures, the error of the k_{eff} model is negligible for micro-stripline structure. The k_{eff} model has relatively large error for stripline structure when k_{ij} is less than 0.1. Note that the error is not important for such small coupling k_{ij}. Therefore, the k_{eff} model for micro-stripline and stripline structures has much higher accuracy compared to that for coplanar structures.

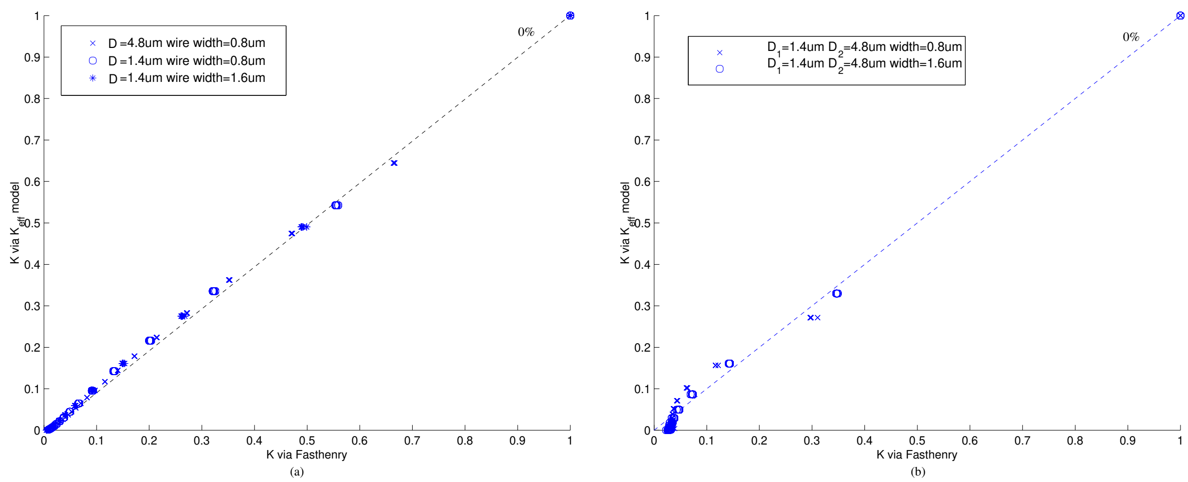

Figure 13: Comparison between coupling coefficients computed by FastHenry and k_{eff} model: (a) micro-stripline structure, and (b) stripline structure.

4 Synthesis of On-chip Interconnect Structures

The k_{eff} models for coplanar and micro-stripline/stripline structures can be used to synthesize on-chip interconnect structures to minimize inductive coupling. In the following, we will use k_{eff} models to design 64-bit bus structures to achieve given noise specifications. We compute the total coupling for each wire i as:

$$K_i = \sum_{j=1(j \neq i)}^{n} k_{ij} \tag{3}$$

where k_{ij} is coupling coefficient between wire i and wire j, n is the total wire number. We consider both coplanar and micro-stripline structures, and assume that the layer stackup is given. We also assume that the wire width is always $0.8\mu m$, and the edge-to-edge spaces in the coplanar structure between all the s- and g-wires are uniform and equal to $0.8\mu m$. Based on our studies of on-chip inductance in Section 2 and 3, we consider shield insertion for coplanar structures, and spacing for micro-stripline structures. We will compare the cost of resulting interconnect structures, and use FastHenry to verify the results.

In the following example, the noise specifications are $K_i \leq 4$ and $K_i \leq 2$, respectively. For the micro-stripline structure, we increase the pitch-space between wire from $0.8\mu m$ at step of $0.1\mu m$, until the maximum $K_i \leq 4$ and $K_i \leq 2$. For the coplanar structure, we start with two edge P/G grids, and insert more g-wires among the s-wires until the maximum $K_i \leq 4$ and $K_i \leq 2$. Essentially , the maximum K_i of k_{eff} model for coplanar structure depends on the maximum block size. For given n wires and a maximum block size m, the structure can always be divided into $\lceil \frac{n}{m} \rceil$blocks. Then we let as many as possible central blocks have block size $(m-1)$, and let m be the size of rest blocks[3].

Table 7 summarizes the synthesized interconnect structures. To reduce the noise specification from $K_i \leq 4$ to $K_i \leq 2$, the total width of the micro-stripline structure is increased by 73%, and the total width of the coplanar structure is increased by 8%. We also compare the maximum K_i obtained by both k_{eff} models and FastHenry. The maximum K_i obtained by our models are 8%, 8%, 12% and -5% different from those obtained by FastHenry, respectively. As verified by FastHenry, the synthesized interconnect structures meet the target K_i. The total time used to synthesize those interconnect structures based on k_{eff} models are less than 1 second. It takes several thousands seconds to verify an interconnect structure by FastHenry.

Interconnect structures	Target K_i	Synthesized structures	Maximum K_i		Total wire width(μm)	Running time	
			k_{eff} models	FastHenry		Synthesis	FastHenry
micro-stripline	4	$s = 1.5\mu m$	3.85(8%)	3.56	95.3(0%)	$\ll$ 1 Second	4575 Seconds
	2	$s = 2.6\mu m$	1.95(8%)	1.80	164.6(73%)	$\ll$ 1 Second	6243 Seconds
coplanar	4	$P(7sg)^2(6sg)^6(7sg)^1 7sG$	3.54(12%)	3.17	116.0(0%)	$\ll$ 1 Second	1623 Seconds
	2	$P(4sg)^{15} 4sG$	1.71(-5%)	1.80	125.6(8%)	$\ll$ 1 Second	1726 Seconds

Table 7: Synthesis and verification of interconnect structures satisfying noise specifications.

We further conducted the following experiments to associate K_i with the noise value. We assume that the wire length is $2000\mu m$, the driver for each wire is 130x of the minimum inverter in a representative $0.18\mu m$ CMOS technology, and the receiver 40x of the minimum inverter. The worst-case signal pattern is applied as the following: all signal wires are simultaneously switching up with rising time of $80ps$, except that one of the two central wires is the victim. We measure the noise at the far-end of the victim wire (the input node of receiver) via SPICE simulation. For the coplanar interconnect structure: $P18sG$, $P(6sg)^2 6sG$ and $P(3sg)^5 3sG$, Table 8 shows the relationship between K_i and on-chip noise obtained by SPICE. It is clear that with more g-wires inserted into the interconnect structures, the noise decreases as K_i does. For $K_i < 2$, the noise is less than 20% of VDD for this interconnect structure.

[3]The central wires have more inductive coupling than the edge wires, so making the central block smaller can alleviate this effect.

Interconnect structure	K_i of victim	Noise (V)	Noise/VDD
$P18sG$	7.68	0.71	55%
$P(6sg)^2 6sG$	3.03	0.38	29%
$P(3sg)^5 3sG$	1.27	0.17	13%

Table 8: Maximum K_i and on-chip interconnect noises.

5 Conclusions and Discussions

In this paper, we have studied the characteristics of on-chip inductance for coplanar, micro-stripline, and stripline structures, and have examined impacts of layout design freedoms such as wire sizing, spacing, and shielding. We have proposed formula-based k_{eff} models as the figures of merit for inductive coupling in the three interconnect structures. Experiments show that the k_{eff} model for the coplanar structure has less than 15% difference compared to the coupling coefficients computed by the numerical field solver FastHenry, and the k_{eff} model for the micro-stripline and stripline structure has negligible difference. We have also applied the proposed models to automatically synthesize on-chip interconnect structures. The automatic synthesis can be finished instantly, and resulting interconnect structures meet the noise specification as verified by FastHenry.

In the future, we plan to build the *explicit* relation between the noise and inductive and capacitive coupling coefficients, and apply the new noise model to layout optimization in deep sub-micron designs.

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