GLOBAL INTERCONNECT SIZING AND SPACING WITH CONSIDERATION OF COUPLING CAPACITANCE

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ABSTRACT

This paper presents an efficient approach to perform *global interconnect sizing and spacing* (GISS) for multiple nets to minimize interconnect delays with consideration of coupling capacitance, in addition to area and fringing capacitances. We introduce the formulation of *symmetric* and *asymmetric* wire sizing and spacing. We prove two important results on the *symmetric* and *asymmetric effective-fringing properties* which lead to a very effective bound computation algorithm to compute the upper and lower bounds of the optimal wire sizing and spacing solution for *all* nets under consideration. Our experiments show that in most cases the upper and lower bounds meet quickly after a few iterations and we actually obtain the optimal solution. To our knowledge, this is the first in-depth study of global wire sizing and spacing for *multiple nets* with consideration of coupling capacitance. Experimental results show that our GISS solutions lead to substantial delay reduction than existing single net wire-sizing solutions without consideration of coupling capacitance.

1. INTRODUCTION

Since the formulation of the optimal wire-sizing problem [1], there have been extensive studies in recent years on optimal wire-sizing algorithm. Most early works used Elmore delay model [2] for interconnects and study the discrete wire sizing [1, 3, 4] and continuous wire shaping or sizing [5, 6]. The wire-sizing problem is also studied under high-order delay model in [7, 8]. A comprehensive survey of these optimization techniques can be found in [9]. These works showed that significant delay reduction can be achieved by optimal wire-sizing in submicron designs. However, none of them explicitly considered the coupling capacitance.

As VLSI technology continues to push toward deep submicron, the coupling capacitance between adjacent wires has become the dominating component in the total interconnect capacitance, due to the decreasing spacing between adjacent wires and the increasing wire aspect ratio for deep submicron processes. Therefore, it is unlikely that an optimal wire-sizing solution which considers only the area and fringing capacitances would remain optimal when the coupling capacitance is considered.

High coupling capacitance in deep submicron design results in both noise (capacitive crosstalk) and additional delay. In this paper, we study the *global interconnect sizing and spacing* (GISS) problem for delay minimization with consideration of the coupling capacitance, in addition to the area and fringing capacitances. In Section 2, we introduce the problem formulation for *symmetric* and *asymmetric* wire sizing and spacing for both single and multiple nets. In Section 3, we present a dynamic programming based algorithm for single net optimization. Then in Section 4, we reveal two *effective-fringing properties* for both symmetric and asymmetric wire-sizing, and propose a very efficient bound computation algorithm to compute the upper and lower bounds of the optimal wire sizing and spacing solution for *all* nets, not just *one* net, under consideration. Experimental results in Section 5 show that the algorithm often leads to identical lower and upper bounds, and therefore achieves optimal solutions. It gives substantial improvement over the single net wire-sizing algorithm without coupling capacitance consideration. Discussion and Future work will be given in Section 6.

2. PROBLEM FORMULATION

2.1. Symmetric and Asymmetric Wire Sizing

Given a layout of n nets, denoted $\mathcal{N}_i$ for $i = 1...n$. Net $\mathcal{N}_i$ consists of $n_i + 1$ terminals $\{s_0^i, \cdots, s_{n_i}^i\}$ connected by a routing tree, denoted T_i. s_0^i is the source of $\mathcal{N}_i$, and the driver D_i at the source has an effective output resistance of R_i. The rest of the terminals are sinks. The terminals (source and sinks) of T_i are at fixed locations, and T_i consists of m_i wire segments denoted by $\{E_1^i, \cdots, E_{m_i}^i\}$. The *center-line* of a wire segment divides the original wire segment evenly. In Figure 1(a), for example, two horizontal wire segments E_1 and E_2 are shown with their center-lines. We assume that the center-line for each wire segment is fixed during wire sizing and spacing.

Each wire segment has a set of discrete choices of wire widths $\{W_1 = W_{min}, W_2, \cdots, W_r\}$. We use w_E to denote the width of the wire segment E. All previous works implicitly assumed *symmetric wire-sizing*, which widens or narrows each wire segment in a symmetric way above and below the center-line of the original wire segment. An example of symmetric wire-sizing of the two wire segments E_1 and E_2 with a neighboring net is shown in Figure 1(b).

However, symmetric wire-sizing may be too restrictive for interconnect sizing and spacing, especially when coupling capacitance is considered. In this paper, we propose an *asymmetric wire-sizing* scheme where we may widen or narrow above and below the center-line of the original wire segment asymmetrically. Using the same example as in Figure 1(b), we would like E_1 to be farther away from its neighboring wire. As a result, we grow only the bottom half of the wire segment, keeping the top half intact, as shown in Figure 1(c). Let $w_E^{\downarrow}$ ($w_E^{\uparrow}$) represent the width of the wire

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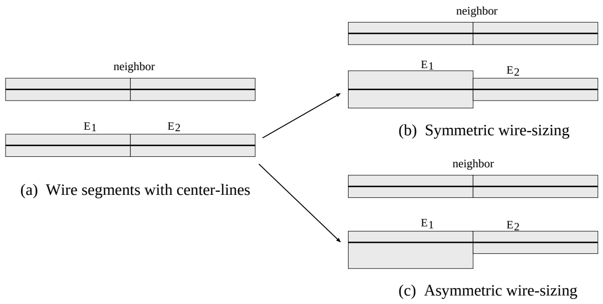

Figure 1. (a) Wire segments with center-lines. (b) Symmetric wire-sizing. (c) Asymmetric wire-sizing.

below (above) a horizontal line segment. The new wire width is defined as $w_E = w_E^{\downarrow} + w_E^{\uparrow}$. An asymmetric wire-sizing solution is valid if $w_E^{\downarrow} \geq W_{min}/2$ and $w_E^{\uparrow} \geq W_{min}/2$. Note that for symmetric wire-sizing, $w_E^{\downarrow} = w_E^{\uparrow} = w_E/2$. To avoid introducing additional notation, we also use $w_E^{\downarrow}$ and $w_E^{\uparrow}$ to denote the asymmetric wire widths for the left and right parts of a vertical wire segment, respectively.

2.2. Interconnect Sizing and Spacing for Single Net

Given a layout of n routing trees T_i's, the interconnect sizing and spacing problem for a single net is to find a symmetric wire assignment $\mathcal{W} = \{w_{E_1^j}, \cdots, w_{E_{m_j}^j}\}$ or an asymmetric wire assignment $\mathcal{W} = \{w_{E_1^j} = (w^{\downarrow}_{E_1^j}, w^{\uparrow}_{E_1^j}), \cdots, w_{E_{m_j}^j} = (w^{\downarrow}_{E_{m_j}^j}, w^{\uparrow}_{E_{m_j}^j})\}$ for a routing tree of interest, say T_j, in order to optimize the following weighted delay objective (as used in [1]) with consideration of *the area, fringing* and *coupling* capacitances:

$$t_{T_j}(\mathcal{W}) = \sum_{k=1}^{m_j} \lambda_k^j \cdot t_{T_j}(s_k^j, \mathcal{W}), \tag{1}$$

where λ_k^j is the criticality of sink s_k^j in net $\mathcal{N}_j$, and $t_{T_j}(s_k^j, \mathcal{W})$ is the sink delay with wire-sizing solution $\mathcal{W}$.

We model the routing tree of each net by an RC tree and use the distributed Elmore delay model [2] to measure the interconnect delays. The formulations used in this section are similar to those in [1]. For clarity of presentation, we assume that a uniform grid structure is superimposed on the routing plane, and each wire segment in the routing plane is divided into a sequence of wires of unit length. Nonetheless, the results presented in this paper can be extended easily to the case where the wire segments are of non-uniform lengths in the same way as in [1].

Assume that the sheet resistance is r, the unit wire area capacitance coefficient c_a, the unit wire fringing capacitance coefficient c_f, and the unit wire lateral capacitance c_{xl}, then the wire resistance r_E and wire capacitance c_E for any grid edge E can be written as follows:

$$r_E = \frac{r}{w_E} \quad \text{and} \quad c_E = c_a \cdot w_E + c_f + c_{xl}(w_E, s_E^{\downarrow}, s_E^{\uparrow})$$

Note that $c_{xl}(w_E, s_E^{\downarrow}, s_E^{\uparrow})$ depends on the spacings $s_E^{\downarrow}$ and $s_E^{\uparrow}$ between E and its lower and upper (or left and right) neighboring wire segments, respectively, whereas c_a and c_f are assumed constants depending only the technology [1].

Note that we focus on the objective of minimizing the weighted sum of sink delays as in [1]. A previous work [10] showed that by assigning appropriate criticality/weight of each sink based on Lagrangian relaxation, the weighted-sum formulation can be used iteratively to meet the required arrival times.

2.3. Global Interconnect Sizing and Spacing for Multiple Nets

In the global interconnect sizing and spacing problem for multiple nets, again, we assume that an initial layout of n routing trees T_i's is given. With consideration of the area, fringing and coupling capacitances, the GISS problem for multiple nets is to find a symmetric wire assignment $\mathcal{W} = \{w_{E_1^1}, \cdots, w_{E_{m_1}^1}, \cdots, w_{E_1^n}, \cdots, w_{E_{m_n}^n}\}$ or an asymmetric wire assignment $\mathcal{W} = \{w_{E_1^1} = (w^{\downarrow}_{E_1^1}, w^{\uparrow}_{E_1^1}), \cdots, w_{E_{m_1}^1} = (w^{\downarrow}_{E_{m_1}^1}, w^{\uparrow}_{E_{m_1}^1}), \cdots w_{E_1^n} = (w^{\downarrow}_{E_1^n}, w^{\uparrow}_{E_1^n}), \cdots, w_{E_{m_n}^n} = (w^{\downarrow}_{E_{m_n}^n}, w^{\uparrow}_{E_{m_n}^n})\}$ for all T_i's such that, the summation of the weighted performance measure of all nets, i.e.,

$$t(\mathcal{W}) = \sum_{j=1}^{n} \delta_j t_{T_j}(\mathcal{W}) \tag{2}$$

is minimized, where δ_j indicates the criticality of net j.

2.4. 2D Capacitance Model

A table-based 2.5D capacitance model suitable for layout optimization was presented in [11] recently, where the lumped capacitance for a wire contains the following components: area and fringing capacitances, lateral coupling capacitance, and cross-over and cross-under capacitances. Based on this model, we consider only area, fringing and lateral coupling capacitances in this paper, since they are the major part of the lumped capacitance. That is, we use a 2D capacitance model simplified from the original 2.5D model. We first use 3D field solver to build tables for area, fringing and lateral coupling capacitances under different width and spacing combinations. During layout optimization, we generate area, fringing and lateral coupling capacitances from pre-built tables. Details and justification of this method can be found in [11].

3. OPTIMAL SIZING AND SPACING FOR SINGLE NET

The optimal wire sizing and spacing problem for a single net with fixed surrounding wire segments can be solved by adapting the bottom-up dynamic programming(DP)-based buffer insertion and wire-sizing algorithm proposed by [3]. Note that in [3], the objective function is to minimize the maximum delay or to meet arrival time requirements, while

[1] In fact, in deep sub-micron designs, c_a and c_f are no longer constants. Their values depend on the width and spacings. A more general notation should be $c_a(w_E, s_E^{\downarrow}, s_E^{\uparrow})$ and $c_f(w_E, s_E^{\downarrow}, s_E^{\uparrow})$. Our GISS algorithm for single-net optimization (Section 3) is able to handle this general capacitance model. The optimality of our bound computation algorithm for multiple nets (Section 4), however, assumes that both c_a and c_f are constants. Its extension for more general 2D capacitance model is discussed in Section 4.3.

our objective is to minimize the weighted sum of all sink delays, which is similar to that in [12]. The major differences of the bottom-up dynamic programming part between this paper and [12] are: (1) we include lateral coupling capacitance between neighboring wires for delay calculation; (2) for the more general asymmetric wire sizing and spacing formulation, we keep two-piece ($w_E^{\downarrow}$ and $w_E^{\uparrow}$) information for each grid edge while performing bottom-up accumulation and top-down pruning. Other details about the DP-based algorithm can be found in [3] and [12].

The single net wire-sizing and spacing can be used for the post-layout optimization for a single critical net (e.g., the clock net). However, this optimization will largely depend on the previous layout of other neighboring nets. And also since many critical nets may share the limited routing resource, just optimizing one net may indeed sacrifice the performance of other critical nets. In the next section, we will look into the global layout optimization for multiple nets.

4. GLOBAL INTERCONNECT SIZING AND SPACING FOR MULTIPLE NETS

The difficulty of the GISS problem for multiple nets arises from the fact that the lateral coupling capacitance coefficient for each wire segment changes with the width and spacings. Moreover, there is no closed form representation for lateral coupling capacitance. The key to solving the multiple-net wire sizing and spacing problem is the *effective-fringing property* of wire-sizing solutions under different spacing conditions. The beauty of this property is that we are able to reduce the GISS problem with variable lateral coupling capacitance to an optimal wire-sizing problem with consideration of only constant area capacitance coefficient and different effective-fringing capacitance coefficients for different wire segments. Such a reduction allows us to compute *global* upper and lower bounds of the optimal wire sizing and spacing solution for *all* nets. In the following, we first state the symmetric and asymmetric effective-fringing properties and discuss their implications. Then, we will describe the bound computation algorithm, followed by a refinement algorithm to obtain the final global interconnect sizing and spacing solution when the lower and upper bounds computed as above do not meet. Extensions to more general 2D capacitance models will then be discussed.

4.1. Effective-Fringing Property: Theorems and Implications

First, we consider the case of symmetric GISS. We define the dominance relation between symmetric wire-sizing solutions of a routing tree in the same way as in [1]:

Definition 1 Symmetric Dominance Relation: *Given two wire width assignments $\mathcal{W}$ and $\mathcal{W}'$, let w_E be the width assignment of edge E in $\mathcal{W}$ and w'_E be the wire width of E in $\mathcal{W}'$. Then, $\mathcal{W}$* dominates *$\mathcal{W}'$ ($\mathcal{W} \geq \mathcal{W}'$) if for any segment E, $w_E \geq w'_E$.*

In the following, we consider an optimization problem called *optimal wire-sizing under variable effective-fringing coefficients (OWS-EF)*. While we still assume a constant area capacitance coefficient c_a, we now define for each wire segment E the *effective-fringing capacitance coefficient* $c_{ef}(E) = c_f + c_{xl}(w_E, s_E^{\downarrow}, s_E^{\uparrow})$ which incorporates the lateral coupling capacitance. It shall be clear later on that this set of effective-fringing capacitance coefficients for all edges allows us to capture the lateral coupling capacitance effectively. The performance measure that we aim at optimizing for OWS-EF problem is the same as in Eqn. (1) except that c_f is replaced by $c_{ef}(E)$ and c_{xl} disappears. Let $\mathcal{C}_{ef}$ denote the set of effective-fringing capacitance coefficients $c_{ef}(E)$'s for all edges in T. We define $\mathcal{C}_{ef} \geq \mathcal{C}'_{ef}$ if $c_{ef}(E) \geq c'_{ef}(E)$ for every E in T. Then the symmetric effective-fringing property can be stated as follows:

Theorem 1 Symmetric Effective-Fringing Property: *For the same routing tree T and a constant c_a, let $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ be an optimal wire-sizing solution to the OWS-EF problem under a set of variable effective-fringing capacitance coefficients $\mathcal{C}_{ef} = \{c_{ef}(E) \mid E \in T\}$, and $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef})$ be an optimal sizing solution under a different set of $\mathcal{C}'_{ef} = \{c'_{ef}(E) \mid E \in T\}$. Then $\mathcal{C}_{ef} \geq \mathcal{C}'_{ef}$ implies that $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ dominates $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef})$.*

The proof of this theorem can be found at [13]. The theorem can be used very effectively to determine the upper and lower bounds of the original optimal GISS problem. Suppose $\mathcal{W}^*$ denotes the global optimal wire-sizing solution optimizing t_T. Let $\mathcal{S}^{\downarrow *}$ and $\mathcal{S}^{\uparrow *}$ denote the spacing obtained based on $\mathcal{W}^*$, and $c_{xl}(w_E^*, s_E^{\downarrow *}, s_E^{\uparrow *})$ be the lateral coupling capacitance coefficient for each edge E based on $\mathcal{W}^*$, $\mathcal{S}^{\downarrow *}$, and $\mathcal{S}^{\uparrow *}$. Let $\mathcal{W}^{\downarrow U}$ and $\mathcal{W}^{\uparrow U}$ be upper bounds of $\mathcal{W}^{\downarrow *}$ and $\mathcal{W}^{\uparrow *}$, and $\mathcal{S}^{\downarrow L}$ and $\mathcal{S}^{\uparrow L}$ be lower bounds of $\mathcal{S}^{\downarrow *}$ and $\mathcal{S}^{\uparrow *}$, respectively. Then $c_{xl}(w_E^U, s_E^{\downarrow L}, s_E^{\uparrow L}) \geq c_{xl}(w_E^*, s_E^{\downarrow *}, s_E^{\uparrow *})$, as the lateral coupling capacitance coefficient decreases when the width of E decreases and the spacings between E and its neighbors increases.

Now consider two instances of the OWS-EF problem. In the first instance, the effective-fringing capacitance coefficient of edge E is $c_{ef}(E) = c_f + c_{xl}(w_E^U, s_E^{\downarrow L}, s_E^{\uparrow L})$. In the second instance, the effective-fringing capacitance coefficient of edge E is $c'_{ef}(E) = c_f + c_{xl}(w_E^*, s_E^{\downarrow *}, s_E^{\uparrow *})$. Clearly, $\mathcal{C}_{ef} \geq \mathcal{C}'_{ef}$. From the symmetric effective-fringing property, the optimal solution $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ dominates the optimal solution $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef})$. Note that $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef}) = \mathcal{W}^*$. Therefore, $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ is also an upper bound of the optimal solution $\mathcal{W}^*$. This procedure can be applied to compute wire width upper bounds (equivalently, lower bounds of spacings) for *all* nets.

Similarly, suppose we are given a lower bound of the optimal wire-sizing solution, denoted $\mathcal{W}^L$. From $\mathcal{W}^L$, we can calculate a spacing upper bound $\mathcal{S}^U$. Now, applying the optimization process for the OWS-EF problem as in the above discussion, $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ will be dominated by $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef}) = \mathcal{W}^*$, since $\mathcal{C}_{ef} \leq \mathcal{C}'_{ef}$. In other words, we have computed a lower bound of the optimal solution.

For asymmetric GISS, we can define

Definition 2 Asymmetric Dominance Relation: *Given two wire width assignments $\mathcal{W} = (\mathcal{W}^{\downarrow}, \mathcal{W}^{\uparrow})$ and $\mathcal{W}' = (\mathcal{W}^{\downarrow\prime}, \mathcal{W}^{\uparrow\prime})$, let $w_E = (w_E^{\downarrow}, w_E^{\uparrow})$ be the width assignment of edge E in $\mathcal{W}$ and $w'_E = (w_E^{\downarrow\prime}, w_E^{\uparrow\prime})$ be the wire width of E in $\mathcal{W}'$. Then, $\mathcal{W}$* dominates *$\mathcal{W}'$ if for any segment E, $w_E^{\downarrow} \geq w_E^{\downarrow\prime}$ and $w_E^{\uparrow} \geq w_E^{\uparrow\prime}$ for any edge E, respectively.*

Then, the asymmetric effective-fringing property can be stated as follows:

Theorem 2 Asymmetric Effective-Fringing Property: *For the same routing tree and a constant c_a, let*

$\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}_{ef}, \mathcal{W}^{\downarrow})$ be an optimal asymmetric wire-sizing solution to the OWS-EF problem with a fixed $\mathcal{W}^{\downarrow}$ and a set of effective-fringing capacitance coefficients $\mathcal{C}_{ef}$, and $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}'_{ef}, \mathcal{W}^{\downarrow\prime})$ be an optimal sizing solution under another fixed $\mathcal{W}^{\downarrow\prime}$ and a different set of $\mathcal{C}'_{ef}$. Then, $\mathcal{W}^{\downarrow} \geq \mathcal{W}^{\downarrow\prime}$ and $\mathcal{C}_{ef} \geq \mathcal{C}'_{ef}$ imply $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}_{ef}, \mathcal{W}^{\downarrow})$ dominates $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}'_{ef}, \mathcal{W}^{\downarrow\prime})$.

Again, the proof of this theorem can be found at [13]. We can also apply the asymmetric effective-fringing property to compute global upper and lower bounds of the optimal wire sizing and spacing solution by solving asymmetric OWS-EF problem. From an upper bound $(\mathcal{W}^{\downarrow U}, \mathcal{W}^{\uparrow U})$, we can again compute lower bound spacings $\mathcal{S}^{\downarrow L}$ and $\mathcal{S}^{\uparrow L}$, and set of lateral coupling capacitance coefficients $c_{xl}((w_E^{\downarrow U}, w_E^{\uparrow U}), s_E^{\downarrow L}, s_E^{\uparrow L})$'s. Similarly, we can compute another set of lateral coupling capacitance coefficients, $c_{xl}((w_E^{\downarrow *}, w_E^{\uparrow *}), s_E^{\downarrow *}, s_E^{\uparrow *})$'s from an optimal wire-sizing solution $\mathcal{W}^* = (\mathcal{W}^{\downarrow *}, \mathcal{W}^{\uparrow *})$.

We denote $c_{ef}(E) = c_f + c_{xl}((w_E^{\downarrow U}, w_E^{\uparrow U}), s_E^{\downarrow L}, s_E^{\uparrow L})$ and $c'_{ef}(E) = c_f + c_{xl}((w_E^{\downarrow *}, w_E^{\uparrow *}), s_E^{\downarrow *}, s_E^{\uparrow *})$ as before. By the asymmetric effective-fringing property, $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}_{ef}, \mathcal{W}^{\downarrow U})$ dominates $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}'_{ef}, \mathcal{W}^{\downarrow *}) = \mathcal{W}^{\uparrow *}$, and therefore, it is still an upper bound of $\mathcal{W}^{\uparrow *}$, the optimal wire-sizing for the top or right portion of each edge. Similar argument applies for the lower bounds and for the bottom (or left) portion of each edge.

4.2. Algorithm for Upper and Lower Bound Computation

The effective-fringing properties (both symmetric and asymmetric) lead to a very effective algorithm to compute the upper and lower bounds of the optimal wire sizing and spacing solution for all nets under consideration. The following presentation considers asymmetric wire sizing and spacing in general. Symmetric wire sizing and spacing can be achieved by simply enforcing $w_E^{\downarrow} = w_E^{\uparrow}$ for all edges.

Upper Bound Computation

$i \leftarrow 0$
$(\mathcal{W}_U^{\downarrow}(i), \mathcal{W}_U^{\uparrow}(i)) \leftarrow$ `Initialize Wire Width Upper Bound`
do
  $\mathcal{C}_{xl}^U(i) \leftarrow$ `Compute Lateral Coefficient`$(\mathcal{W}_U^{\downarrow}(i), \mathcal{W}_U^{\uparrow}(i))$
  $\mathcal{C}_{ef}^U(i) \leftarrow$ `Compute Effective-Fringing Coefficient`$(\mathcal{C}_{xl}^U(i))$
  $\mathcal{W}_U^{\downarrow}(i+1) \leftarrow$ `DPW`$(\mathcal{W}_U^{\uparrow}(i), \mathcal{C}_{ef}^U(i))$ `/* for all nets */`
  $\mathcal{C}_{xl}^{U\prime}(i) \leftarrow$ `Compute Lateral Coefficient`$(\mathcal{W}_U^{\downarrow}(i+1), \mathcal{W}_U^{\uparrow}(i))$
  $\mathcal{C}_{ef}^{U\prime}(i) \leftarrow$ `Compute Effective-Fringing Coefficient`$(\mathcal{C}_{xl}^{U\prime}(i))$
  $\mathcal{W}_U^{\uparrow}(i+1) \leftarrow$ `DPW`$(\mathcal{W}_U^{\downarrow}(i+1), \mathcal{C}_{ef}^{U\prime}(i))$ `/* for all nets */`
  $i \leftarrow i+1$
while $(\mathcal{W}_U^{\downarrow}(i), \mathcal{W}_U^{\uparrow}(i)) \neq (\mathcal{W}_U^{\downarrow}(i-1), \mathcal{W}_U^{\uparrow}(i-1))$

Figure 2. Algorithm to compute an upper bound of the global optimal wire-sizing.

The algorithm to compute an upper bound of the optimal solution is illustrated in Figure 2. The algorithm starts at the iteration $i = 0$. First we initialize upper bounds of all wire widths specified by the layout constraints. A sample initialization is shown in Figure 3. Let E_l and E_u be two parallel horizontal edges, with E_l below E_u. Let W_{min} be

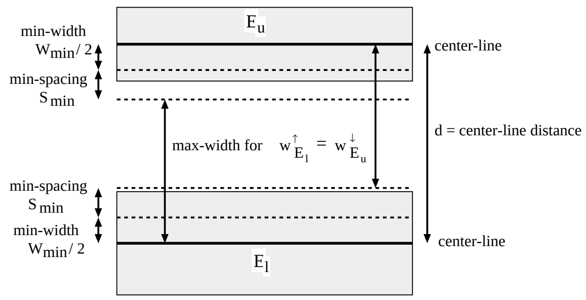

Figure 3. Initialization of upper-bound wire widths.

the minimum wire width, and S_{min} be the minimum spacing between two parallel wires from the layout constraints. If the distance between the center-lines of E_l and E_u is d, then the maximum width (i.e., the initial upper bound) for $w_{E_l}^{\uparrow}$ (the side closer to E_u) and $w_{E_u}^{\downarrow}$ (the side closer to E_l) is $d - W_{min}/2 - S_{min}$.

From the upper bound $(\mathcal{W}_U^{\downarrow}, \mathcal{W}_U^{\uparrow})$, we compute the upper bound effective-fringing capacitance coefficients. Again, consider E_l and E_u which are of distance d. Let $w_{E_l}^{\uparrow U}$ be the width of E_l in $\mathcal{W}_U^{\uparrow}$, and $w_{E_u}^{\downarrow U}$ the width of E_u in $\mathcal{W}_U^{\downarrow}$. If $d - w_{E_l}^{\uparrow U} - w_{E_u}^{\downarrow U} < S_{min}$, then, the upper bound wire widths overlap and we assign the lower bound spacing between E_l and E_u to be S_{min}, i.e., $s_{E_l}^{\uparrow L} = s_{E_u}^{\downarrow L} = S_{min}$. Otherwise, the lower bound spacings $s_{E_l}^{\uparrow L}$ and $s_{E_u}^{\downarrow L}$ are $d - w_{E_l}^{\uparrow U} - w_{E_u}^{\downarrow U}$. Similarly, for E_l and its lower neighbor we compute $s_{E_l}^{\downarrow L}$. From $s_{E_l}^{\uparrow L}$ and $s_{E_l}^{\downarrow L}$, we can compute $c_{xl}((w_{E_l}^{\downarrow U}, w_{E_l}^{\uparrow U}), s_{E_l}^{\downarrow L}, s_{E_l}^{\uparrow L})$. Let $\mathcal{C}_{xl}^U$ denote such set of lateral coupling capacitance coefficients obtained from $(\mathcal{W}_U^{\downarrow}, \mathcal{W}_U^{\uparrow})$. We then compute the effective-fringing coefficient $c_{ef}(E_l) = c_f + c_{xl}((w_{E_l}^{\downarrow U}, w_{E_l}^{\uparrow U}), s_{E_l}^{\downarrow L}, s_{E_l}^{\uparrow L})$. Similarly we can calculate the upper bound $c_{ef}(E_u)$. We refer to the set of upper bound $c_{ef}(E)$ for all edges based on $\mathcal{C}_{xl}^U$ as $\mathcal{C}_{ef}^U$.

We then perform the following iterative process to update the wire width upper bounds. To compute $\mathcal{W}_U^{\downarrow}(i+1)$, we apply the bottom-up dynamic programming-based wire-sizing (DPW) algorithm outlined in Section 3 to each net with fixed $\mathcal{W}_U^{\uparrow}(i)$ and $\mathcal{C}_{ef}^U(i)$, without explicitly dealing with lateral coupling capacitance. Then, we can similarly compute $\mathcal{W}_U^{\uparrow}(i+1)$ for each net using $\mathcal{W}_U^{\uparrow}(i)$, and updated $\mathcal{W}_U^{\downarrow}(i+1)$ and $\mathcal{C}_{ef}^{U\prime}(i)$. The process is iterated until $(\mathcal{W}_U^{\downarrow}(i), \mathcal{W}_U^{\uparrow}(i))$ is identical to $(\mathcal{W}_U^{\downarrow}(i+1), \mathcal{W}_U^{\uparrow}(i+1))$.

For the lower bound computation, we start with the minimum allowable width for each wire $(\mathcal{W}_L^{\downarrow}(0), \mathcal{W}_L^{\uparrow}(0))$, and compute $\mathcal{C}_{xl}^L(0)$, a set of lateral capacitance coefficients obtained under lower bound wire widths. Subsequently $\mathcal{C}_{ef}^L(0)$ is computed from $\mathcal{C}_{xl}^L(0)$. Then, we apply the iterative process as in the upper bound computation.

Our experiments show that in most cases, the lower and upper bounds computed as above will meet after a few iterations and we actually obtain the optimal solution from the bound computations. When the upper and lower bounds do not meet, we will use the following refinement algorithm to obtain the final wire sizing and spacing solution for each net: We first take the lower bound of each side for each wire segment as our initial layout. Then we will iteratively perform single net wire sizing and spacing optimization method presented in Section 3 to obtain the final GISS solution following the order of each net's priority. We call the overall bound computations and final refinement algorithm GISS/FAF, where FAF denotes the fixed area and fringing capacitance coefficients.

4.3. Extension to Variable Area and Fringing Capacitance Coefficients

The optimality of bound computation in the above GISS/FAF algorithm is based on the effective-fringing properties which assume the area capacitance coefficient c_a and the fringing capacitance coefficient c_f are constants independent of wire widths and spacings. However, in deep submicron designs, c_a and c_f are dependent on wire widths and spacings (e.g., there are about 30% variations on c_a and c_f values in our 2D capacitance tables). Nevertheless, the GISS algorithm can still be used in this case simply by computing the area and fringing capacitances from the general 2D model directly during the bottom up dynamic programming optimization. However, the effective-fringing properties cannot be used to guarantee that the optimal solution is always within the upper and lower bounds computed by the GISS algorithm. We call the algorithm using variable c_a and c_f's as GISS/VAF. Experimental results in Section 5.2 show that GISS/VAF often achieves better results when compared with GISS/FAF.

5. EXPERIMENTAL RESULTS

We have implemented GISS using C++ under the Sun SPARC station environment. In this section, we present the experimental results. The parameters used in our experiments are based on the $0.18\mu m$ technology specified in the SIA roadmap [14]. The sheet resistance is 0.0638 $\Omega/\square$. The minimum wire sizing W_{min} is $0.22\mu m$ and minimum spacing S_{min} between neighboring wires is $0.33\mu m$. Then, *pitch* spacing, defined as the sum of minimum spacing and minimum wire size, is equal to $0.55\mu m$. The allowable wire widths for each side along the center line are from 0.11 to 1.1 μm, with the incremental step to be 0.11 μm. The area, fringing and lateral coupling capacitances are obtained by a look-up table obtained through the 2D capacitance extraction model [11]. The driver effective resistance is 119 Ω. The input capacitance for each sink is set to be 12.0fF.

5.1. Optimal Sizing and Spacing for a Single Net

We perform experiments for the optimal single-net sizing and spacing algorithm on 5 nets provided by Intel. The routing trees are the same as used in [4]. These trees originally have multiple sources and we randomly assign one as the unique single source. We assign equal criticality for each sink so the weighted delay becomes the average delay. Given the initial layout of these five nets, we randomly assign some surrounding wire segments with spacing from the net being 1 to $5 \times pitch$.

In Table 1, we summarize the average and maximum HSPICE delays from different algorithms: minimum wire sizing (MIN); symmetric optimal wire-sizing (OWS-S) algorithm without considering the coupling capacitance (but coupling capacitance through the 2D model is included in its final HSPICE simulation); symmetric GISS algorithm (GISS-S) and asymmetric GISS algorithm (GISS-A). In the parentheses under OWS-S, GISS-S and GISS-A, we list the percentage of improvement over MIN. From the table, we can see that GISS-A consistently outperforms all other algorithms. In terms of its average delay, which is our objective function, the reduction is up to 52.4% compared with the MIN solution (Net4), and 29.4% with OWS-S (Net5) and 29.4% with GISS-S (Net5).

Although the average delay is our objective, experimental results show that this formulation reduces the maximum delays as well. From the table, we can see that GISS-A outperform MIN, OWS-S and GISS-S by up to 45.2% (Net2), 21.2% and 22.0% (Net5) compared with MIN, OWS-S and GISS-S respectively.

5.2. Optimal Sizing and Spacing for Multiple Nets

To demonstrate the effectiveness of GISS algorithm, we perform experiments for global optimal wire sizing and spacing for multiple nets on a 16-bit parallel bus structure of 10 mm long with the center distance between adjacent bus line set to be $\{2, 3, 4, 5, 6\} \times pitch$ respectively.

In Table 2, we give the average delays (maximum delays are the same due to the symmetry of the bus structure) from HSPICE simulations and normalized wire widths (ratio of average wire size to W_{min}). We still list in the parentheses the percentage of delay reduction over MIN. In the table, column GISS/FAF uses the GISS algorithm with fixed c_a and c_f (obtained through the 2D table-look-up with $3 \cdot W_{min}$ width and $5 \cdot S_{min}$ spacing) to guide the layout optimization, whereas GISS/VAF directly uses the 2D model with variable area and fringing capacitance coefficients during the layout optimization. All these algorithms use the 2D model for final HSPICE simulations.

We observe that the upper and lower bounds often meet quickly after just a few iterations for both GISS/FAF and GISS/VAF. For GISS/FAF, from the effective fringing property, we indeed obtain the optimal solution under the given constant c_a and c_f.

From the table, we can see that the average delays of GISS/FAF outperform those of MIN by up to 56.6%, and outperform those of OWS by up to 43.4% respectively. Although GISS/VAF cannot guarantee optimality, our experiments do show that it outperforms GISS/FAF by up to 26.9%. This is due to that: (i) c_a and c_f are no longer constants for deep submicron design, (ii) we use the 2D model with variable c_a and c_f's for both HSPICE simulations, which GISS/VAF also uses during GISS optimization. It actually suggests that our GISS algorithm may indeed have the capability to handle more general capacitance models.

The normalized width from GISS is larger than that from OWS since the effective fringing capacitance coefficients for GISS are larger than those for OWS, which confirms our effective-fringing properties.

6. DISCUSSIONS AND FUTURE WORK

Our study has shown convincingly that it is very important to consider coupling capacitance into VLSI interconnect optimization for deep submicron designs. We have proposed two general formulations, symmetric and asymmetric, for the global interconnect sizing and spacing problem and revealed the effective-fringing properties for both symmetric and asymmetric scenarios. We develop an effective algorithm to compute the lower and upper bounds for the global optimal sizing and spacing solution. Our experiments show that in most cases, the upper and lower bounds meet in a few iterations so we will get the optimal GISS solution for fixed area and fringing capacitance coefficients.

We prove the effective-fringing properties and derive the GISS algorithm under the assumption of fixed c_a and c_f.

	length	Average Delay (ns)				Maximum Delay (ns)			
	(mm)	MIN	OWS-S	GISS-S	GISS-A	MIN	OWS-S	GISS-S	GISS-A
Net1	3.6	0.08	0.08 (-0.00%)	0.08 (-0.00%)	0.08 (-0.00%)	0.13	0.13 (-0.00%)	0.13 (-0.00%)	0.13 (-0.00%)
Net2	6.6	0.29	0.17 (-41.4%)	0.16 (-44.8%)	0.14 (-51.7%)	0.31	0.19 (-38.7%)	0.19 (-38.7%)	0.17 (-45.2%)
Net3	10.07	0.62	0.49 (-21.0%)	0.49 (-21.0%)	0.47 (-24.2%)	0.81	0.66 (-18.5%)	0.66 (-18.5%)	0.64 (-21.0%)
Net4	10.57	0.42	0.22 (-47.6%)	0.21 (-50.0%)	0.20 (-52.4%)	0.56	0.37 (-33.9%)	0.33 (-41.1%)	0.31 (-44.6%)
Net5	31.98	2.17	1.80 (-17.1%)	1.80 (-17.1%)	1.27 (-41.5%)	3.52	3.11 (-11.6%)	3.14 (-10.8%)	2.45 (-30.4%)

Table 1. Comparison of the average and maximum delays using different algorithms.

	Average Delay (ns)				Normalized wire width			
center spacing	MIN	OWS	GISS/FAF	GISS/VAF	MIN	OWS	GISS/FAF	GISS/VAF
$2 \times pitch$	1.75	1.45 (-17.1%)	0.82 (-53.1%)	0.82 (-53.1%)	1.00	1.75	2.60	2.99
$3 \times pitch$	1.51	0.83 (-45.0%)	0.63 (-58.3%)	0.56 (-62.9%)	1.00	2.40	2.64	3.56
$4 \times pitch$	1.29	0.66 (-48.8%)	0.56 (-56.6%)	0.45 (-65.1%)	1.00	2.50	2.64	3.70
$5 \times pitch$	1.21	0.60 (-50.4%)	0.53 (-56.2%)	0.42 (-65.3%)	1.00	2.50	2.64	3.75
$6 \times pitch$	1.16	0.56 (-51.7%)	0.52 (-55.2%)	0.38 (-67.2%)	1.00	2.50	2.59	4.06

Table 2. Comparison of average delays and normalized wire widths for a 16-bit parallel bus structure under 5 different pitch spacings using different algorithms.

Our experiments indeed show that it is also very effective under variable c_a and c_f's. It suggests that the GISS algorithm actually have the capability to handle more general capacitance models. Further validation is planned as a future work.

An alternative for computing lower and upper bounds is to use the local refinement method based on dominance property similar to those used in [1, 12, 15]. In particular, the GISS problem under variable c_a and c_f's may be formulated as a general CH-posynomial program [15]. Therefore, a local refinement based algorithm similar to that used in [15] may be used to compute the lower and upper bounds of the global optimal solution under variable c_a and c_f's. According to our experience, the local refinement based algorithm can be much faster than the dynamic-programming based algorithm used in this paper. We plan to implement it in the future. Also, we plan to develop efficient noise models and extend our GISS algorithm for noise control and minimization.

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