Formulae and Applications of Interconnect Estimation Considering Shield Insertion and Net Ordering *

James D. Z. Ma and Lei He
Electrical and Computer Engineering Department
University of Wisconsin, Madison, WI 53706
dma@cae.wisc.edu and lhe@ece.wisc.edu

Abstract

It has been shown recently that simultaneous shield insertion and net ordering (called SINO/R as only random shields are used) provides an area-efficient solution to reduce the RLC noise. In this paper, we first develop simple formulae with errors less than 10% to estimate the number of shields in the min-area SINO/R solution. In order to accommodate pre-routed P/G wires that also serve as shields, we then formulate two new SINO problems: SINO/SPR and SINO/UPG, and propose effective and efficient two-phase algorithms to solve them. Compared to the existing dense wiring fabric scheme, the resulting SINO/SPR and SINO/UPG schemes maintain the regularity of the P/G structure, have negligible penalty on noise and delay variation, and reduce the total routing area by up to 42% and 36%, respectively. Various estimation results developed in this paper can be readily used to guide global routing and high-level design decisions.

1. INTRODUCTION

Signal integrity is a critical design issue for high-performance deep-submicron circuits and systems. Most existing studies focus on reducing the capacitive coupling, and effective techniques include net ordering [1, 2], buffer insertion [3, 4], and shielding such as the dense wiring fabric (DWF) [5]. As we move towards gigahertz circuits and systems, the inductive coupling gains increasing prominence. Different from the capacitive coupling that exists between adjacent wires, the inductive coupling may affect both adjacent and non-adjacent wires [6]. It has been shown that shielding and buffer insertion are still effective to reduce inductive coupling [6, 7, 8], but net ordering alone becomes less effective [9]. Therefore, a simultaneous shield insertion and net ordering (SINO/R) problem has been studied to minimize the routing area under a given RLC noise bound [9, 10].

However, it is not clear how to incorporate the above SINO/R schemes into the VLSI physical design flow. Concerns include: (i) How to estimate the number of shields and pre-allocate the routing area for shields at an early enough stage during physical design? and (ii) How to accommodate P/G wires that also serve as shields? P/G wires are often pre-routed and are preferred by the designer to have a regular structure.

To solve the above concerns, we first study in this paper the interconnect congestion estimation for min-area SINO/R solutions. We then formulate two new SINO problems: SINO problem with simultaneous signal and power routing (SINO/SPR) and SINO problem with uniform P/G structure (SINO/UPG). Based on the estimation result, we propose efficient two-phase algorithms to solve them, considering pre-routed P/G wires and maintaining the regularity of P/G structure. Compared to the recently proposed dense wiring fabric (DWF) scheme [5], the resulting SINO-based wiring schemes can reduce the total routing area by up to 42%, with negligible penalty on noise and delay variation.

The rest of this paper is organized as follows: Section 2 introduces preliminaries and reviews the related work. Section 3 presents shield estimation for SINO/R solutions. Section 4 formulates and solves two new SINO problems: SINO/SPR and SINO/UPG. Section 5 concludes this paper with discussions on future work. A full version of this paper is available as a technical report [11], including proof of theorems and more experimental results.

2. PRELIMINARIES AND RELATED WORK

Similar to [10, 9], we denote a signal net as *s-wire* and define that two nets s_1 and s_2 are *sensitive* to each other if a switching signal on s_1 causes s_2 to malfunction (due to extraordinary crosstalk or delay variation) and vice-versa. Further, we assume that two non-sensitive nets do *not* switch simultaneously. The *sensitivity rate* of s_i is defined as the ratio of the number of aggressors for s_i to the total number of signal nets. For a set of coupled RLC signal nets, the sensitivity rate can be either uniform (i.e., every signal net has the same sensitivity rate) or non-uniform. The sensitivity for all s-wires in a given problem can be represented compactly with a sensitivity matrix of size $n \times n$, where n is the number of s-wires. An entry of 1 or 0 in location (i, j) indicates that s_i and s_j are sensitive or not sensitive, respectively, to one another. A random shield is directly connected (without through devices) to the P/G wire structure.[1] By inserting a shield between two sensitive s-wires, we are able to eliminate the capacitive coupling and reduce the inductive coupling. We use the terms "wire" and "net" interchangeably in this paper.

The SINO/R problem is first studied under the K_{eff} model [9], and then under the explicit noise model [10]. Both use random shields to obtain min-area SINO solutions. Similar to [10, 9], we assume in this paper that all signal nets have uniform wire width, length, thickness, and spacing. We use the explicit noise model from [10] unless otherwise stated. The model computes the worst-case noise voltage considering both capacitive coupling and long-range inductive coupling. Therefore the noise bound can be represented as an explicit voltage. Extensive experiments have shown that the explicit noise model is conservative compared to SPICE

*This research is partially supported by NSF CAREER Award CCR-0093273 and a grant from Intel. Address comments to lhe@ece.wisc.edu.

[1] The most convenient way to connect random shields is to add vias between shields and P/G wires in orthogonal routing layers. In this paper, we assume that there is a connection between the P/G structure and every $100\mu m$-long random shield.

simulation over the distributed PEEC (partial element equivalent circuit) model [12] under the worst-case signal pattern.

Throughout this paper, we consider the following set of interconnect design specifications (see Table 1) derived from ITRS [13]. In order to alleviate the impacts of initial placement and the distribution of sensitive wires on experimental results, the sensitive nets are picked randomly with respect to a given s-wire and its sensitivity rate. Unless otherwise stated, we always generate ten different random sensitivity matrices and ten initial placements for each design combination, and consider the average number of shields. We use the following accurate circuit model to verify SINO solutions: we divide each wire into $100\mu m$-long segments. Each segment is modeled by an RLC π-model, with a coupling capacitance to its adjacent segment that does not belong to the same wire. There is a coupling inductance between any two segments, no matter whether they belong to the same wire or different wires. We use SPICE to simulate the resulting circuit model and obtain the *peak noise* for a single SINO solution as the maximum noise among all wires considering the worst-case signal pattern. We report both maximum and average peak noise if there are multiple SINO solutions.

technology	$0.10\mu m$	driver resistance	150Ω
Vdd	1.05V	load capacitance	60fF
noise bound	0.15V	wire width	$1.0\mu m$
frequency	3GHz	wire spacing	$0.8\mu m$
input rising time	$33ps$	wire thickness	$1.1\mu m$
wire length	$2000\mu m$, $1400\mu m$, $1000\mu m$		

Table 1: Interconnect design specifications derived from ITRS.

3. SHIELD ESTIMATION

It has been established in [14] that the number of shields (N_s) is a quadratic function of uniform sensitivity rate (S) and a linear function of the number of signal nets (N). In order to explicitly accommodate L as a variable into the shield estimation, we perform SINO/R experiments and show N_s versus L in Figure 1 for given N and S. Different from the intuition, N_s does not monotonically increase with respect to L. We may divide the figure into two regions: Region I with L smaller than $2000\mu m$, and Region II with L larger than $2000\mu m$. N_s monotonically increases with respect to L in Region I, but not in Region II. This can be explained by the observation made in [15, 16] that the inductive effect becomes relatively weak for long wires. However, from $500\mu m$ to $2000\mu m$ (Region I), which are typical interconnect lengths considering the buffer insertion for performance optimization [17], N_s can be best characterized by a quadratic function.

Using curve fitting via nonlinear regression analysis method [18], we obtain the following formula with respect to three variables $\{N, S, L\}$:

$$\begin{aligned} N_s &= 8.49\times10^{-6}\cdot L^2\cdot S^2 - 3.82\times10^{-7}\cdot L^2\cdot N\cdot S \\ &\quad -7.93\times10^{-6}\cdot L^2\cdot S + 3.90\times10^{-6}\cdot L^2 \\ &\quad -0.010\cdot L\cdot S^2 + 0.26\cdot N\cdot S + 0.045\cdot L\cdot S \\ &\quad -17.06\cdot S - 0.10\cdot N - 0.014\cdot L + 6.88 \end{aligned} \quad (1)$$

for the uniform sensitivity. When the sensitivity rate is not uniform but is S_i for s-wire s_i, the shield estimation can be obtained by replacing S with $\frac{1}{N}\cdot\sum_{i=1}^{N} S_i$ and S^2 with $\frac{1}{N}\cdot\sum_{i=1}^{N} S_i^2$ in formula (1). Therefore, we have the following formula:

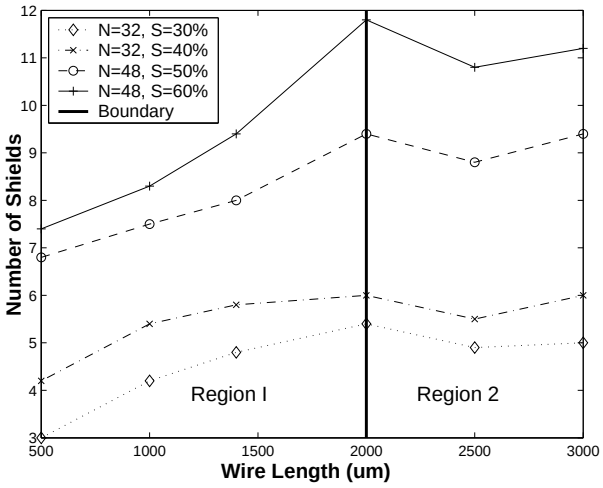

Figure 1: N_s versus L for different combinations of N and S in the $0.10\mu m$ technology.

$$\begin{aligned} N_s &= 8.49\times10^{-6}\cdot\frac{L^2}{N}\cdot\sum_{i=1}^{N} S_i^2 - 3.82\times10^{-7}\cdot L^2\cdot\sum_{i=1}^{N} S_i \\ &\quad - 7.93\times10^{-6}\cdot\frac{L^2}{N}\cdot\sum_{i=1}^{N} S_i + 3.90\times10^{-6}\cdot L^2 \\ &\quad - 0.010\cdot\frac{L}{N}\cdot\sum_{i=1}^{N} S_i^2 + 0.26\cdot\sum_{i=1}^{N} S_i + 0.045\cdot\frac{L}{N}\cdot\sum_{i=1}^{N} S_i \\ &\quad - \frac{17.06}{N}\cdot\sum_{i=1}^{N} S_i - 0.10\cdot N - 0.014\cdot L + 6.88 \end{aligned} \quad (2)$$

In Figure 2, we compare the numbers of shields computed by formulae (1) and (2) with those obtained by *individual* SINO/R solutions. Even though the formulae are developed on the average number of shields, one can easily see that N_s given by the formulae has errors less than 10% compared to *each and every* SINO/R solution under the same experimental setting. We believe that the function template used in formulae (1) and (2) can be re-used by other generations of technologies, except that coefficients should be re-evaluated using a limited set of SINO experiments as we do in this paper. Details of formula development and verification, as well as the estimation for the ITRS $0.07\mu m$ technology can be found in [11].

4. APPLICATIONS OF SHIELD ESTIMATION

In this section, we first formulate two new SINO problems: SINO/SPR and SINO/UPG, and then propose two-phase algorithms to solve them based on shield estimation (1) and (2).

4.1 SINO/SPR Problem

4.1.1 Motivation and Problem Formulation

P/G wires are also shields to reduce the inductive and capacitive noise but not considered in SINO/R problems. In order to consider pre-routed P/G structures, we formulate the following new *p*-SINO problem:

FORMULATION 1. *(optimal p-SINO problem): Given a set of signal nets and a pre-routed P/G structure, the optimal p-SINO*

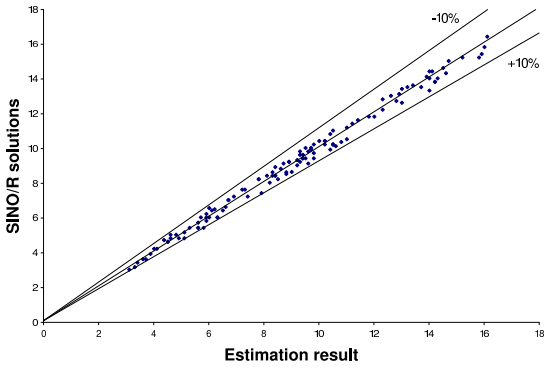

Figure 2: Comparison of numbers of shields between formulae and min-area SINO/R solutions. All errors are less than 10%.

problem finds a min-area SINO solution such that any s-wire has total noise less than a given bound.

We assume that the P/G structure is regular, i.e., the *P/G pitch*, defined as the number of routing tracks between a pair of adjacent P/G wires, is a constant. Hence, P/G wires have fixed track assignments but signal nets or random shields can be assigned to arbitrary routing tracks. In [11], we have proven the following theorem:

THEOREM 1. *The optimal p-SINO problem is NP-hard.*

Therefore, we develop a simulated annealing algorithm similar to the SINO/R algorithm in [10]. Please refer to [11] for details of the algorithm development.

P/G pitch size	5	6	7
sensitivity rate	maximum peak noise / average peak noise		
30%	0.1183/0.0947	0.1214/0.1009	0.1216/0.1026
50%	0.1291/0.1107	0.1212/0.1023	0.1249/0.1060
70%	0.1352/0.1168	0.1273/0.1084	0.1310/0.1121
sensitivity rate	P/G wires / random shields		
30%	6/2.0	5/2.0	**4/2.2**
50%	**6/2.2**	5/3.8	4/4.8
70%	**6/3.8**	5/6.8	4/8.0

Table 2: Summary of *p*-SINO solutions for 32 signal nets with uniform sensitivity rate. In each cell of rows 3–5, the first value is the maximum peak noise and the second value is the average peak noise. In each cell of rows 7–9, the first value is the number of pre-routed P/G wires and the second value is the average number of random shields.

We have tested our algorithm implementation using a number of design combinations with fixed wire length $2000\mu m$. The maximum and average peak noise values for each of the resulting *p*-SINO solutions are presented in Table 2. All maximum peak noise values are smaller than 0.15V, the specified noise bound in Table 1. We also report the number of P/G wires and average number of random shields in Table 2. The min-area solution is highlighted for each sensitivity rate. One can easily see that different P/G structures (i.e., different P/G pitches) lead to SINO solutions with different area costs. For example, in the case of 70% sensitivity rate, the best P/G structure has a P/G pitch of 5 and leads to a min-area solution with a total of 9.8 shields on average. On the other hand, increasing the P/G pitch to 7 leads to a total of 12 shields on average, an increase of 25% compared to the min-area solution. This observation motivates us to study the following SINO/SPR problem to find the best P/G structure that can achieve the min-area solution.

FORMULATION 2. *(optimal SINO/SPR problem): For a given number of signal nets and a given noise bound, the optimal SINO/SPR problem decides a regular P/G structure such that the resulting p-SINO solution with respect to the P/G structure has minimum area and fewer random shields than P/G wires.*

Because random shields have to be connected with P/G wires, they bear implicit routing overhead and weaken the desired regularity of shielding structure. In order to explore the tradeoff between layout regularity and routing area, we explicitly require that random shields be fewer than P/G wires in our problem formulation, i.e., on average, there is at most one random shield inserted between every pair of adjacent P/G wires.

4.1.2 SINO/SPR Algorithm

A brute-force solution to the SINO/SPR problem is to enumerate all possible P/G structures using the *p*-SINO algorithm, and then find the solution with the minimum area. Because the *p*-SINO problem is NP-hard, we propose the following efficient two-phase algorithm: in the first phase, we define a regular P/G structure based on SINO/R shield estimation (1) and (2); and in the second phase, we carry out *p*-SINO procedures to find the min-area SINO/SPR solution by searching the *very* limited neighborhood of the predefined P/G structure. This two-phase algorithm is expected to achieve the solution of the same quality with the brute-force algorithm but in a much shorter runtime.

Specifically, we speculate in the first phase that the optimal P/G structure that leads to the min-area solution should have a P/G pitch space (*PS*) given by

$$PS = \lceil \alpha \cdot \frac{N}{N_s} \rceil \quad (3)$$

where N_s is the estimated number of random shields used in min-area SINO/R solutions and is given by formula (1) or (2). Furthermore, we speculate that the coefficient α is a constant and is insensitive to different experiment settings. This speculation will be verified through experiments later on.

To achieve the min-area SINO/SPR solution in the second phase, we first apply the *p*-SINO algorithm with respect to the pre-routed P/G structure defined in formula (3). We call the resulting SINO/SPR solution the best among the *0-order neighborhood* (in short, *best of 0-neighbor*). We may then apply the *p*-SINO algorithm to extra P/G structures defined by P/G pitches $(PS+1)$ and $(PS-1)$, respectively. We denote the best solution among the three P/G pitches $(PS+1)$, *PS*, and $(PS-1)$ as *the best of the first-order neighborhood* (in short, *best of 1st-neighbor*). Similarly, we may have the best of 2nd-neighbor, 3rd-neighbor, and etc.. Empirical evidence will show that searching only the first-order neighborhood is capable of achieving the min-area solution.

4.2 SINO/UPG Problem

An alternative approach to maintain the regularity of the P/G structure is to distribute the P/G wires uniformly without inserting any random shield. We can still apply net ordering for noise minimization. This introduces the following SINO/UPG problem formulation:

FORMULATION 3. *(optimal SINO/UPG problem): For a given number of signal nets and a given noise bound, the optimal SINO/*

UPG problem decides a regular P/G structure and assigns signal nets to routing tracks such that the resulting solution has minimum area and any s-wire has noise less than the given bound.

Similar to the SINO/SPR problem, a brute-force algorithm can be applied to search exhaustively over all possible P/G structures for the min-area SINO/UPG solution. Based on the same methodology used to solve the SINO/SPR problem, however, we have also developed a much more efficient two-phase algorithm. In the first phase, we speculate the following P/G pitch:

$$PS = \lceil \beta \cdot \frac{N}{N_s} \rceil \quad (4)$$

We anticipate that β is also a constant. But because no random shields are allowed, more P/G wires are needed to meet the given noise bound and β should be smaller than α. In the second phase, we carry out modified *p*-SINO procedures that employs net ordering only to obtain the min-area SINO/UPG solution.

We will show that the formula (4) provides a tight upper bound for the optimal P/G structure. SINO/UPG solutions are always found if we start with this pre-defined P/G structure and decrease the speculated P/G pitch by at most three tracks.

4.3 Experimental Results and Discussions

We have implemented and applied our two-phase SINO/SPR and SINO/UPG algorithms to a large number of design combinations with 48 signal nets, including cases with uniform sensitivity rates from 30% to 60% and two non-uniform sensitivity cases 1 and 2 (see Table 3). No single SINO solution of various formulations costs more than ten seconds in a PIII machine.

4.3.1 SINO/SPR Results

We present the distribution of the min-area SINO/SPR solutions among different neighborhoods in Figure 3. Almost all of the min-area solutions are obtained within the first-order neighborhood. Only 2 out of 180 design combinations have min-area solutions with P/G pitch $(PS-2)$ or $(PS+2)$, i.e., the min-area solution is in the second-order neighborhood. We present the peak noise in column 4 of Table 3. The maximum peak noise is always smaller than the given noise bound. We also present the number of P/G wires for the min-area solution and the correspondent average number of random shields in column 10 of Table 3. The random shields in all experimental results are fewer than the P/G wires, as required in our problem formulation. Further, as anticipated, the required P/G wires and random shields increase when the sensitivity rate and wire length increase. The longer wire implies fewer buffers inserted. Therefore, there is a smooth tradeoff between the buffer area and routing area for P/G wires and shields. Moreover, as we speculated, the coefficient α can be set as a constant (=1.82) through experiments.

Because the min-area solution for almost all design combinations is achieved by only searching the first-order neighborhood of the pre-defined P/G structure, we summarize the two-phase SINO/SPR algorithm in Figure 4.

4.3.2 SINO/UPG Results

Similarly, we set the coefficient β in formula (4) as 1.12 through experiments and apply the two-phase algorithm to solve the SINO/UPG problem in a similar fashion with Figure 4. The distribution of the SINO/UPG solutions among different P/G pitches are presented in Figure 5. The min-area SINO/UPG solution is always found by subtracting at most three tracks from the speculated P/G pitch, i.e., at most four P/G pitches need to be tried. In column 5 of Table 3, all of the maximum peak noise values are smaller than the given bound. In column 11, we present the number of P/G wires that are needed for the min-area SINO/UPG solution. Again as anticipated, the required P/G wires increase when the sensitivity rate and wire length increase. Therefore, there is a smooth tradeoff between the area for buffers and P/G wires.

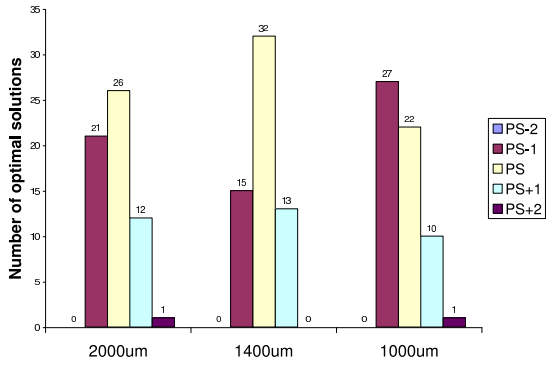

Figure 3: Distribution of min-area SINO/SPR solutions.

Given a number of signal nets, sensitivity, wires length, and noise bound voltage Phase One: Use formulae (1)–(3) to define a regular P/G structure Phase Two: Carry out *p*-SINO procedures to find the min-area solution within the first-order neighborhood of the pre-defined P/G structure.

Figure 4: Two-Phase SINO/SPR algorithm.

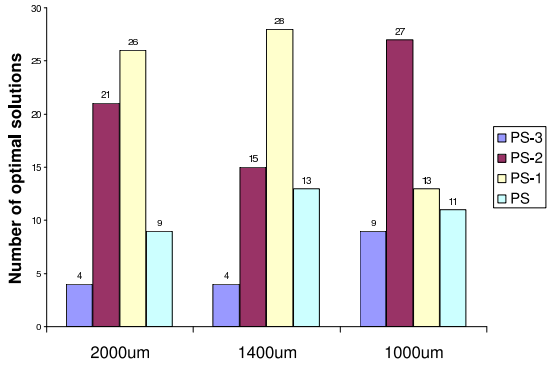

Figure 5: Distribution of min-area SINO/UPG solutions

4.3.3 Comparison between SINO Solutions

The three types of SINO solutions cover a spectrum of design tradeoffs between the regularity of shielding structure and total routing area. We have SINO/R < SINO/SPR < SINO/UPG in terms of the shielding regularity, and SINO/R < SINO/SPR < SINO/UPG in terms of the total area. I.e., SINO/R has the minimum area but the most irregular shielding structure, and SINO/UPG has the maximum area but the regular P/G structure without any random shields. It is easy to see from Table 3 that SINO/SPR offers the most interesting/desired scheme. It maintains a regular P/G structure, leads to a total area only slightly larger than SINO/R, but

1	2	3	4	5	6	7	8	9	10	11
wire length	sensivity rate	SPICE-computed peak noise (in V)			shield pitch	P/G pitch		P/G wires / random shields		
		SINO/R	SPR	UPG	SINO/R	SPR	UPG	SINO/R	SPR	UPG
$0.10\mu m$ technology, noise bound = 0.15V (14% Vdd)										
2000 μm	30%	0.1003/0.0740	0.1168/0.0981	0.1148/0.0926	7 : 6.6 : 6	9	4	0/7.2	5/3.0	13/0
	40%	0.1075/0.0769	0.1192/0.0997	0.1352/0.1176	7 : 6.2 : 6	9	4	0/8.0	5/4.0	13/0
	50%	0.1142/0.0784	0.1204/0.1010	0.1185/0.1063	6 : 5.2 : 5	7	3	0/9.4	6/3.6	17/0
	60%	0.0967/0.0805	0.1197/0.1104	0.0924/0.0785	5 : 4.2 : 4	6	2	0/11.4	8/3.8	25/0
	case 1	0.1042/0.0755	0.1193/0.1005	0.1157/0.0980	6 : 5.4 : 5	6	3	0/9.4	5/4.6	17/0
	case 2	0.1081/0.0782	0.1210/0.0993	0.1032/0.0737	6 : 5.4 : 5	8	4	0/8.6	5/4.2	13/0
1400 μm	30%	0.1022/0.0758	0.1179/0.0977	0.1210/0.1044	8 : 7.6 : 7	12	6	0/6.2	4/2.4	9/0
	40%	0.1057/0.0772	0.1195/0.1009	0.1386/0.1193	8 : 7.4 : 6	12	6	0/6.6	4/3.0	9/0
	50%	0.1101/0.0792	0.1210/0.1058	0.1187/0.0915	6 : 5.8 : 5	9	4	0/8.2	5/3.6	13/0
	60%	0.1073/0.0799	0.1215/0.1123	0.1038/0.0769	6 : 5.6 : 5	8	3	0/9.2	6/3.6	17/0
	case 1	0.1019/0.0794	0.1189/0.1056	0.1164/0.1028	7 : 6.8 : 6	11	4	0/7.8	4/3.8	13/0
	case 2	0.1066/0.0769	0.1197/0.1009	0.1301/0.1176	7 : 6.6 : 6	12	6	0/7.0	4/3.2	9/0
1000 μm	30%	0.1074/0.0772	0.1202/0.0994	0.1347/0.1142	10 : 9.6 : 9	13	8	0/5.2	3/2.4	7/0
	40%	0.1103/0.0785	0.1218/0.1044	0.1385/0.1170	8 : 7.2 : 6	12	8	0/6.6	4/2.8	7/0
	50%	0.1089/0.0802	0.1226/0.1077	0.1237/0.1106	7 : 6.4 : 6	12	6	0/7.2	4/3.6	9/0
	60%	0.1115/0.0813	0.1270/0.1141	0.1261/0.1128	7 : 6.2 : 6	9	4	0/8.0	5/3.8	13/0
	case 1	0.1082/0.0797	0.1230/0.1075	0.1215/0.1024	8 : 6.8 : 6	11	6	0/7.0	4/3.4	9/0
	case 2	0.1096/0.0779	0.1224/0.1053	0.1044/0.0728	8 : 7.2 : 7	12	6	0/6.6	4/3.6	9/0

Composition of the non-uniform sensitivity									
sensitivity	10%	20%	30%	40%	50%	60%	70%	80%	90%
case 1	2	0	2	0	7	7	19	9	2
case 2	0	0	6	17	9	15	1	0	0

Table 3: (i) top table - Comparison of SINO/R, SINO/SPR, and SINO/UPG solutions. In each cell of columns 3–5, the first value is the maximum peak noise and the second value is the average peak noise. In each cell of column 6, the first value is the maximum random shield pitch, the second value is the average random shield pitch, and the third value is the minimum random shield pitch. In each cell of columns 9–11, the first value is the number of P/G wires and the second value is the average number of random shields. (ii) bottom table - Composition of the two non-uniform sensitivity cases.

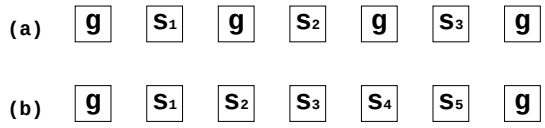

Figure 6: (a) DWF scheme with alternated shields (P/G wires) and signal wires; (b) SINO solutions with five signal wires between a pair of shields. The shield pitch of five is about the average shield pitch in Table 5. We consider fifteen signal wires during the simulation by duplicating the above structure three times and measure delay variations for the central structure.

reduces the total area by up to 18% compared to SINO/UPG (see the result in Table 3 for $2000\mu m$ length and 60% sensitivity).

4.3.4 Comparison between SINO and DWF Schemes

The essence of SINO formulations is that whenever a signal wire is switching, its neighboring wires are either quiet signal wires or shields. The SINO/UPG with the extremely dense P/G structure alternates signal wires and shields, and is equivalent to the dense wiring fabric (DWF) proposed in [5] (see Figure 6.(a)). The total area of SINO solutions depends on the sensitivity rate. We argue that changing the single-phase clock to two-phase non-overlapping clock leads to a 50% sensitivity rate for all signal nets (see [11]). Given this sensitivity rate and $1400\mu m$ wire length, SINO/SPR and SINO/UPG solutions use a total of 8.6 and 13 shields (see Table 3), respectively. But DWF needs 49 P/G wires for the 48 signal nets. Compared to DWF, SINO/SPR and SINO/UPG reduce the total area by 42% and 36%, respectively, and still maintain regular P/G structures.

The DWF is originally designed to reduce both noise and delay variations under the RC model. As we have convincingly shown that SINO is able to meet the given noise bound, we now compare their delay variations under the RLC model. We use interconnect structures in Figure 6, and assume that these nets are $1400\mu m$-long. We use SPICE simulation over the best-case and worst-case signal patterns to obtain delay variations, under the constraint that there are no adjacent signal nets switching at the same time for the SINO structure. The resulting delay variation is $5.2ps$ for the DWF structure[2] (see Figure 6.(a)), and $7.7ps$ for the SINO structure (see Figure 6.(b)). The difference between the delay variations is negligible $2.5ps$. Given the total area reduction of up to 42% and such a small penalty on delay variation, we believe that various SINO schemes, especially the SINO/SPR and SINO/UPG schemes with regular P/G structures, are viable alternatives to the DWF scheme.

5. CONCLUSION AND FUTURE WORK

Simultaneous shield insertion and net ordering (SINO/R) introduced in [9, 10] is an area-efficient technique to reduce the RLC noise. In this paper, we have developed simple yet accurate formulae (with errors less than 10%) to estimate the numbers of shields for min-area SINO/R solutions.

To accommodate pre-routed P/G wires, we have formulated new SINO/SPR and SINO/UPG problems and proposed two-phase algorithms to solve them, based on the shield estimation for min-area SINO/R solutions. Experiments show that the two algorithms are

[2]Because we use RLC model in this paper, the delay variation is larger than that under RC model in [5].

effective and efficient. Compared to the dense wiring fabric scheme [5], the resulting SINO/SPR and SINO/UPG wiring schemes have negligible penalty on noise and delay variation, and reduce the total routing area by up to 42% and 36%, respectively.

The interconnect estimation results in this paper (together with the total routing area estimation in [11]) can be used to guide global routing and high-level or early-stage design decisions. The simplest interconnect structure, parallel bus structure, is assumed in this work. We intend to further incorporate various SINO formulations and estimation to a global router for signal and power net co-design.

6. REFERENCES

[1] T. Gao and C. L. Liu, "Minimum crosstalk switchbox routing," in *ICCAD*, 1994.

[2] T. Xue and E. S. Kuh, "Post global routing crosstalk synthesis," *IEEE Trans. on CAD*, Dec. 1997.

[3] A. Vittal, L. Chen, M. Marek-Sadowska, K. Wang, and S. Yang, "Crosstalk reduction for VLSI," *IEEE Trans. on CAD*, 1997.

[4] C. J. Alpert, A. Devgan, and S. T. Quay, "Buffer insertion for noise and delay optimization," in *DAC*, 1998.

[5] S. Khatri, A. M. Mehrotra, R. K. Brayton, and A. Sangiovanno-Vincentelli, "A novel VLSI layout fabric for deep sub-micron applications," in *DAC*, 1999.

[6] L. He, N. Chang, S. Lin, and O. S. Nakagawa, "An efficient inductance modeling for on-chip interconnects," in *CICC*, 1999.

[7] M. W. Beattie and L. Pileggi, "IC analyses including extracted inductance model," in *DAC*, 1999.

[8] Y. Cao, C. M. Hu, X. Huang, A. B. Kahng, S. Muddu, D. Stroobandt, and D. Sylvester, "Effects of global interconnect optimizations on performance estimation of deep submicron design," in *ICCAD*, 2000.

[9] L. He and K. M. Lepak, "Simultaneous shielding insertion and net ordering for capacitive and inductive coupling minimization," in *ISPD*, 2000.

[10] K. M. Lepak, I. Luwandi, and L. He, "Simultaneous shield insertion and net ordering for coupled RLC nets under explicit noise constraint," in *DAC*, 2001.

[11] J. D. Ma and L. He, "Simultaneous signal and power routing based on interconnect estimation," in *Univerisity of Wisconsin, Technical Report, ECE-01-002*, 2001.

[12] A. Ruehli, "Equivalent circuit models for three-dimensional multiconductor systems," *IEEE Trans. on MTT*, 1974.

[13] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors*, 1999.

[14] J. D. Ma and L. He, "Simulatenous signal and power routing under K_{eff} model," in *SLIP*, 2001.

[15] A. Deutsch and et al., "When are transmission-line effects important for on-chip wires," *IEEE Trans. on MTT*, 1997.

[16] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figures of merit to characterize the importance of on-chip inductance," in *DAC*, 1998.

[17] J. Cong, L. He, K. Khoo, C. Koh, and Z. Pan, "Interconnect design for deep submicron ICs," in *ICCAD*, 1997.

[18] C. Daniel, F. Wood, and J. Gorman, *Fitting equations to data: computer analysis of multifactor data*. New York: Wiley, 1980.