Research Interests

I. Summary of Previous Works

With a strong background in circuit simulation, interconnect extraction and modeling, and VLSI layout design and optimization, my research goals are to study issues critical to the design of state-of-the-art VLSI circuits and systems, to propose practical solutions based on physical and algorithmic foundations, and to transfer prototype tools to the industry. My doctoral thesis focuses on the following two problems: the interconnect-centric layout optimization, and interconnect extraction and modeling. Both problems are of growing importance as we move into the era of nanometer technology and gigahertz frequency, because the system performance has increasingly become dominated by the interconnect delay.

I.1 Contributions to layout optimization

My earliest work at UCLA [C4, J5] was the first in-depth study to consider **the wiresizing optimization for multi-source nets**, such as bus structures in microprocessors or other VLSI systems, while previous approaches only considered nets with single sources. We obtained several elegant theoretical results, and developed a highly efficient algorithm based on the variable wire segmentation, called the bundled wiresizing algorithm. Not only did the algorithm lead to substantial delay reduction for multi-source nets, it also improved the speed of the previous single-source wiresizing algorithm by as much as a factor of 100, without losing any accuracy. The work has been extended to consider simultaneous driver and wire sizing for multi-source nets [C6], and has generated follow-up works from UC San Diego [1] and UT Austin [2,3]. The wire sizing algorithm has also been used in a later work from UCLA [4].

My main contribution in the layout optimization area was to formulate and solve **the simultaneous transistor and interconnect sizing (STIS) problem** [C6,C10,J7]. Among the earliest works to optimize both devices and wires, our series of works stood out in the following ways: (i) Our formulations were capable of handing a netlist and complex gates, whereas other works considered a single net with only drivers or buffers. (ii) We were able to apply accurate device models (e.g., table-based models) with consideration of effects like waveform shapes, whereas most works could only handle device models using very simple formulas. More importantly, our works made a theoretically innovative contribution. We developed three classes of optimization problems, **the simple, monotonically constrained, and bounded CH-programs**, and showed that many layout optimization problems including the STIS problem were CH-programs. We proposed to compute *tight* lower and upper bounds of the exact solutions to the three CH-programs, using three types of local refinement (LR) operations respectively. In practice, our STIS algorithm based on different types of LR operations achieved optimal solutions under different device models. Although our STIS formulation is more general than most works, the algorithm is one of the most efficient methods in the literature. Our works have stimulated interests on LR-based optimization from UT Austin [5,6].

In addition, drawing upon my strength in interconnect extraction and modeling, I formulated **the global interconnect sizing and spacing (GISS) problem** based on the concept of asymmetric wire sizing, in a joint paper with my UCLA colleagues [C9]. Taking account of the coupling capacitance, the problem optimized the wire sizing and spacing solutions *simultaneously* for multiple nets. In contrast, previous wire sizing formulations considered a single net without coupling capacitance. Because the formulation well captured the characteristics of the interconnect capacitance in deep submicron designs, it obtained significant delay reductions compared to the single-net wire sizing formulations. Furthermore, the GISS problem was shown to be a CH-program [C10,J7]. It instantly resulted in a LR-based algorithm that is 100x faster than an alternative approach using a dynamic-programming technique. Moreover, the formulation and solution of the GISS problem have been naturally integrated into the framework of the STIS problem, which makes the

STIS work [C10,J7] the only existing device and wire sizing study that is able to apply accurate models for both device delay and interconnect capacitance.

The industry has expressed a great deal of interests in these works that addressed the critical issues in the high-performance interconnect designs. One of my UCLA colleagues integrated the bundled wiresizing algorithm [C4,J5] into the GARDS system, which is a layout tool from Silicon Valley Research, Inc. Moreover, I have implemented the bundled wiresizing algorithm, as well as STIS and GISS algorithms [C6,C10,J7] in the **TRIO (Tree, Repeater and Interconnect Optimization) package**, which comprises of a variety of interconnect optimization algorithms mainly developed in UCLA [C8]. I also have played a leading role in program integration and design flow control for the package, and have provided models for device delay and interconnect capacitance, as well as algorithms for the simultaneous buffer and wire sizing module. The package has been included in a global routing system of Intel, and has been transferred to Hewlett-Packard Research Laboratories.

I.2 Contributions to interconnect extraction and modeling

I have collaborated with the industry to work on interconnect extraction and modeling, with emphasis on efficient generation of accurate models for interconnect resistance, capacitance and inductance. In a joint work [C7] between Cadence Design Systems, Inc. and UCLA, five "foundations" were proposed and validated based on basic constraints (planarization and minimum metal density requirement) in process technologies. These foundations enable a **2½-D capacitance extraction methodology**, which reduces the multi-layer capacitance extraction problem at the full-chip level to two subproblems, one considering three wire traces on a metal layer and the other considering six wire traces on two adjacent layers. The 2½-D methodology has been shipped with the Silicon Ensemble 5.0 product from Cadence for timing verification, and has been used in the TRIO package and quite a few recent works from UCLA (e.g., [7,8]) for interconnect synthesis and planning.

In the latest cooperation with Hewlett-Packard Research Laboratories (HPL), I proposed **an efficient inductance extraction methodology** in order to generate the RLC model for on-chip interconnects. My HPL colleagues and I have also applied the RLC model, with consideration of process variations, to simulating and optimizing interconnects for the most advanced microprocessor designs. A paper on the inductance extraction methodology has been submitted to a major IEEE conference [9].

II. Future Plans

In the near future, I would like to work on **computer-aided design for high-speed circuits**, especially on inductance-aware interconnect planning and synthesis. The on-chip inductive effect has become a factor of increasing prominence that limits the circuit performance for high-end microprocessors and other VLSI systems. However, very few existing works have considered the on-chip inductance for interconnect synthesis, and they have tended to use over-simplified inductance models. I am interested in developing a spectrum of highly efficient algorithms under the accurate RLC model. Moreover, I will make prototype tools available to the industry and the academia. Concerning interconnect planning, there are few preliminary recent studies (e.g., [8]) using *nominal* RC models. My research plans include further studies in this direction as well. I will use the RLC models (e.g., [9]), and consider process variations and process migration. I would also like to study the **physical design for SOI** (system on chip), with emphasis on synthesis of power, clock and global nets, and process migration of IP blocks. In addition to my rich research experience in physical design, my knowledge of and insights in circuit simulation and interconnect extraction and modeling will greatly facilitate these critical studies.

Teaching Interests

I would like to teach a variety of **graduate courses** on design automation, including VLSI Design, Logic Synthesis of Digital Systems, Physical Design Automation of VLSI Systems, and Circuit Simulation and Analysis. In order to better prepare students to design high-performance systems for the nanometer technology and gigahertz frequency, I would also like to offer an **advanced graduate course**, Interconnect Modeling and Optimization. This new course has just started to be offered in UCLA. It is based on a comprehensive survey of existing results on interconnect synthesis and layout compiled by my UCLA colleagues and me [J6]. I also prepared and gave a four-hour lecture on interconnect extraction for this course, and assigned and evaluated homework on this topic.

Given my double background in electrical engineering and computer science, I am also capable of teaching a wide range of **undergraduate classes**, such as Logic Design of Digital Systems, Computer Architecture, Computer Network Fundamentals, Basic Methods of Data Organization, and programming languages.

References:

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