Interconnect Planning, Synthesis, and Layout for Performance, Signal Reliability, and Cost Optimization

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Proposal Period: 1998 to 2001
Amount Requested for Proposal Period: $359,982
Date of Renewal Submission: November 14, 1998
Expiration Date of Proposal: 2001

Proposal Approvals

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1 Overview of Proposed Research

As VLSI technology reaches deep submicron device dimensions and gigahertz clock frequencies, interconnect delay has become the dominating factor in determining system performance. Also, due to the increase in wire aspect ratio (height over width) in deep submicron designs, coupling effect of interconnect lines has a strong impact on signal reliability. Furthermore, since interconnects in future ICs may require 6-8 wiring layers, and a significant portion of system power will be consumed on charging and discharging interconnect structures, interconnect synthesis and optimization will also have important implication on design complexity, manufacturing cost and power dissipation.

In this project, we propose to investigate an interconnect-centric design flow and methodology, which emphasizes interconnect planning and synthesis throughout the design process in order to optimize the overall system performance, reliability, and cost. We plan to study the following set of problems, which are critical to the success of such an interconnect-centric design methodology:

Interconnect Planning: Careful interconnect planning needs to be carried out at each level of the design process for accurate estimation and effective optimization of system performance, reliability, and cost. We plan to investigate the following interconnect planning problems: (i) interconnect architecture planning prior to the design process, which determines the optimal number of routing layers, the nominal width and spacing in each layer, the thickness of each interconnect and isolation layer, the metal resistivity and dielectric constant of each layer (assuming different material/process may be used for different layers for performance, yield, cost considerations), vertical interconnection schemes (e.g. via dimensions and structures), etc., for overall system-level performance and power optimization, subject to the manufacturing constraints; (ii) interconnect planning with RTL-level floorplanning, which defines the global and local interconnects, provides an estimate of overall interconnect distribution and interconnect performance, and guides the RTL-level and logic-level synthesis tools to perform retiming, pipelining, and various logic optimization to meet the performance target; (iii) interconnect planning with physical-level floorplanning, which interacts closely with the interconnect synthesis tools (to be discussed later) and plan for the best interconnect topology, wire ordering and widths, wire spacing, layer assignments, etc., together with the physical floorplan of logics, under the constraints of the performance, signal reliability, yield, area, and the overall cost of the design. We believe that interconnect planning is a very important, if not the most important, step in high-level design, synthesis, and layout coupling.

Interconnect Synthesis: Interconnect synthesis will be a key part of the interconnect planning system, which determines the optimal or near-optimal interconnect topology, wire width and spacing, buffer locations and sizes, etc, to meet the performance and signal reliability requirements of one or several nets. Since RC delay minimization for a single isolated net is fairly well understood, our focus will be on proper modeling of *crosstalk and substrate noise* and take them into consideration in synthesizing and optimizing *multiple physically-related and temporally-related nets*. We shall also study the inductive effect on interconnect synthesis in gigahertz IC designs.

Interconnect Layout: A flexible and highly efficient multi-layer gridless routing system is critical for providing accurate interconnect planning and estimation, and implementing the chosen interconnect structures with complex topology, ordering, width, and spacing specifications determined from interconnect planning and synthesis. We will leverage our ongoing research effort in developing an efficient multi-layer general-area gridless router for mixed-signal MCM designs supported under the DARPA Electronic Packaging and Interconnects (EP&I) program. No additional funding will be requested from SRC to support this part of the effort.

The proposed research addresses many key issues in the following critical areas identified in the SRC

Task Force Report on Physical Design: (B) high-level design, synthesis & layout coupling, (C) signal timing, (D) signal integrity, (E) placement and routing. The proposed research forms a single-task project.

2 Individual Task Descriptions

2.1 Catalog page

Task ID: 605.001

Start: 01-Jan-1998

Technology Areas: Design Sciences > Electronic Design Automation

Anticipated Primary Result: A new interconnect-centric design flow with innovative approaches, efficient algorithms, and prototype software tools for early interconnect planning, optimal interconnect synthesis, and efficient interconnect layout.

Background: As VLSI technology moves to deep submicron device dimensions and gigahertz clock frequencies, VLSI interconnects play the dominating role in determining the performance, power, reliability, and cost of the system. Therefore, it is necessary to consider an interconnect-centric design flow which considers interconnect estimation and planning, optimal interconnect synthesis, and efficient interconnect layout implementation at each level of the design process. Early interconnect estimation and planning are critical to assure the proper coupling between synthesis and layout, and enable the design convergence. Optimal interconnect synthesis is key to deliver the best possible interconnect performance and reliability under various design constraints. An efficient and flexible interconnect layout system is the foundation to support various interconnect design constraints and various interconnect optimization techniques, and cope with the rapid increase in layout design complexity.

Description: This project investigates an innovative interconnect-centric design flow and methodology, which emphasizes interconnect planning and synthesis throughout the design process in order to achieve the overall system performance, reliability, and cost optimization. It focuses on providing the following capabilities to support such an interconnect-centric design flow: (1) interconnect planning, which includes interconnect architecture planning, RTL-level interconnect planning and floorplanning, and physical-level interconnect planning and floorplanning; (2) interconnect synthesis, which determines the optimal or near-optimal interconnect topology, wire ordering, buffer locations and sizes, wire width and spacing, etc., to meet the performance and signal reliability requirements of one or multiple nets; (3) interconnect layout, which will be achieved by a flexible and highly efficient multi-layer general-area gridless routing system.

Schedules and Milestones:

- Year 1: Development of a computational model for interconnect architecture planning based on a given design characterization (specified in terms of target clock rate, interconnect distribution, depths of the logic network, etc.); Development and validation of very efficient but accurate noise models to relate the noise with the physical design parameters to guide the interconnect synthesis algorithm for signal reliability optimization.

- Year 2: Development of efficient algorithms for integrated interconnect planning and floorplanning capabilities at the physical level; Development of optimal or near-optimal interconnect synthesis algorithm for multiple spatially or temporally related signal nets for performance and signal reliability optimization; Completion of the ongoing effort on the development of a multi-layer general-area gridless routing system.

- Year 3: Development of efficient algorithms for integrated interconnect planning and floorplanning capabilities at the RTL-level; Development of models and efficient interconnect optimization algorithms for high-frequency signals with consideration of on-chip self and mutual inductance.

Task Leader: Prof. Jason Cong
SRC Monitor/Mentors: to be assigned (Do you have some? XXX)
Graduate Students: Lei He and David Zhigang Pan

2.2 Further Technical Discussions

The section provides additional technical information on our Year 1 accomplishments and proposed work for the coming proposal year.

2.2.1 Year 1 Accomplishments

Our first year of the SRC project went very well. We have made significant accomplishments, including the following three major areas:

Interconnect Delay and Area Estimations: We are the first group [?, ?] to provide systematic studies on interconnect delay estimation under interconnect optimization. In particular, we derived a set of simple delay estimation models (DEM) under various optimization techniques, e.g., optimal wire sizing (OWS), simultaneous driver and wire sizing (SDWS), and simultaneous buffer insertion/sizing and wire sizing (BISWS). These DEMs are shown to have 90% accuracy when compared with those obtained by running corresponding complex interconnect optimization algorithms (for example, those from the TRIO package in [?]) directly. These DEMs can be used in various design planning stages to provide accurate timing information without really going into the layout details.

Since OWS is the basis for deriving the delay estimation model for both SDWS and BISWS, we study it further and find that the delay and area using OWS can be approximated accurately by two simple wire sizing schemes, namely single-width sizing (1-WS) and two-width sizing (2-WS). When the coupling capacitance is considered explicitly, 2-WS outperforms 1-WS in terms of delay and area reduction, and achieves close to optimal solution compared to running global interconnect sizing and spacing (GISS) algorithm [?] directly.

We further study the delay/area trade-off using the closed-form interconnect estimation models from 1-WS and show that delay is not sensitive to certain variation of wire width around the optimal width. Therefore, we can achieve significant area reduction with a slight increase in delay. In particular, we show that the AT^4 (A–area, T–delay) metric works well to guide the area-efficient performance optimization and leads to more than 60% area reduction from OWS but with only about 10% delay increase.

The above study is mainly focused on two-pin nets. But the results for two-pin nets can be leveraged to handle multiple-pin nets with tree topologies. For multiple-pin nets, there are possibly many design objectives. We use two typical optimization objectives: (i) minimize the delay to a given single critical sink, (ii) minimize the maximum delay for all critical sinks (i.e, the *tree delay*, as defined in [?]). For each objective, we perform OWS or BISWS for performance optimization. Our main contributions include the following:

- Under objective (i), we formulate the original problem into a single-line-multiple-load (SLML) problem. We then transform SLML into an equivalent single-line-single-load (SLSL) problem, and use our closed-form estimation for 2-pin nets to obtain the delay and area estimation.

- Under objective (ii), we obtain a lower bound delay estimation for the optimal tree delay and show that in practice, this lower bound delay estimation is very *tight* and close to the optimal tree delay.

Interconnect Architecture Planning: Our delay and area sensitivity study for OWS further suggests that there exists some small set of "globally" optimal widths for a wide range of interconnect lengths. Therefore, we study the interconnect architecture planning for wire-width design at each metal layer. We derive such "globally" optimal 1-width and 2-width designs, and show rather surprisingly that using two "pre-designed" widths, we are still able to achieve close to optimal performance compared with those obtained by GISS using many possible widths. For $0.10\mu m$ technology, our 2-width design leads to optimal 2-WS solution which is only no more than 7% away from those by GISS, for *any* wire length distributions.

We have performed interconnect architecture planning for all major technology generations listed in NTRS'97 from $0.25\mu m$ to $0.07\mu m$. Our recommendation is based on the optimal 2-width design considering the area-efficient performance optimization metric AT^4. The results are shown in Table 1. It suggests the minimum widths for local interconnects in Tier1. For Tier2 to Tier4, there are two different pre-determined wire widths with 1:2 ratio. Therefore, we have a wiring hierarchy on different metal layers such that Tier2 is about 1-2 times wider than Tier1, Tier3 is about 2-3 times wider than Tier2, and Tier4 (if available) is about 4-5 times wider than Tier3. Such a wiring hierarchy can effectively minimize the interconnect delays for all local, semi-global and global interconnects while ensuring high routing density and highly simplified routing solutions.

Tech. (μm)		0.25	0.18	0.13	0.10	0.07
Tier1	$W_1'^*$	0.25	0.18	0.13	0.10	0.07
	$W_2'^*$	0.25	0.18	0.13	0.10	0.07
Tier2	$W_1'^*$	0.25	0.18	0.13	0.10	0.08
	$W_2'^*$	0.50	0.36	0.26	0.20	0.16
Tier3	$W_1'^*$	0.65	0.47	0.24	0.22	0.23
	$W_2'^*$	1.30	0.94	0.48	0.44	0.46
Tier4	$W_1'^*$	-	-	0.98	1.00	1.06
	$W_2'^*$	-	-	1.96	2.00	2.12

Table 1: 2-width design (in μm) for area-efficient performance optimization.

Interconnect Inductance Extraction:

The following papers were published or submitted in the past one year under the SRC project.

1. J. Cong and D. Z. Pan, "Interconnect performance estimation models for synthesis and design planning," in *IEEE/ACM Int. Workshop on Logic Synthesis*, June, 1998.

2. J. Cong and D. Z. Pan, "Interconnect delay estimation models for logic and high level synthesis, " in *SRC TECHCON*, September, 1998. (**Best Paper in Session**).

3. J. Cong and D. Z. Pan, "Interconnect delay estimation models for synthesis and design planning," in *Proc. Asia and South Pacific Design Automation Conf.*, January, 1999.

4. J. Cong and D. Z. Pan, "Interconnect estimation and planning for deep submicron designs," submitted to *Proc. Design Automation Conf*, 1999.

5. J. Cong and D. Z. Pan, "Interconnect delay and area estimation for multiple-pin nets," submitted to *TAU'99*.

2.2.2 Proposed Work

For Year 2 of this SRC project, we will continue our efforts for the interconnect-centric design flow with early interconnect planning, optimal interconnect synthesis and efficient interconnect layout.

Interconnect Planning: We plan to work on simultaneous module floorplanning and interconnect planning. We will use our delay and area estimation models to couple with the current simulated-tempering slicing floorplanning []. We can either add the interconnect delay (say longest path) as part of the objective function, or as a constraint.

Interconnect Synthesis: We will continue our effort to develop efficient yet accurate crosstalk noise model and incorporate it into our global interconnect sizing and spacing framework for both delay and noise optimization.

Interconnect Layout:

2.3 Technology Transfer Plan

Most of research results from this task will be transferred to the SRC member companies through research reports and publications (will be listed in the SRC Research Catalog and also distributed directly to the member company mentors), presentations at the SRC site visit, and our visit to member companies. A list of our current contacts at several SRC member companies are listed in the next subsection.

We also expect to produce several prototype software tools based on the theory and algorithms developed in the proposed research, which may be transferred directly to the SRC member companies. In particular, we expect that the following prototype tools will be available:

- An interconnect architecture planning tool for determining the optimal interconnect physical architecture: Given a design characterization (specified in terms of target clock rate, interconnect distribution, depths of the logic network, etc.) and device models, it determines the optimal number of routing layers, the nominal width and spacing in each layer, the thickness of each interconnect and isolation layer, etc., for overall system-level performance and power optimization (subject to the manufacturing constraints).

- An interconnect synthesis tool which can determine the optimal routing topology, pin assignment and wire ordering, buffer insertion and driver/buffer/receiver sizing, simultaneous wire sizing and wire spacing, and layer assignment under performance and signal reliability constraints for a set of spatially and temporally related signal nets.

We expect that these tools will become mature in the second or third year of the project. Their availability will be announced in the SRC progress report and during the SRC site visits. These tool will be developed in the C++ language with well-defined file interfaces or APIs, so that interested parties from the member companies can easily evaluate and apply these tools in their design environments.

We strongly suggest that the SRC member companies collectively contribute a set of design benchmarks which reflects the rapid growing complexity of today's (and hopefully tomorrow's) designs, so that university researchers can test their tools on realistic cases. These designs may be edited by the original owners so that they can be released through SRC to university researchers under non-disclosure agreements. Such benchmark circuits will be very useful to validate many ideas and results from the universities and help the successful technology transfer from the universities to the industry.

2.4 List of SRC Member Companies Providing Mentors

We do not have an active SRC contract at this point. Therefore, we do not have any mentor from SRC companies. However, we have established good working relationship with the following individuals and teams in several SRC companies through exchanging research problems, ideas, results, and providing graduate students and summers interns to these companies:

- Ganapati Srinivasa, Dr. Mosur K. Mohan, (Managers of two advanced physical design groups) and Dr. Soumyanath Krishnamurty (Microprocessor Research Lab) at Intel.
- Dr. Norman Chang and Dr. S. Y. Oh (Project Lead and Lab Manager of ULSI Technology Lab) at Hewlett-Packard Laboratories,
- Dr. David LaPotin (Manager of Computer-aided Design and Analysis) at IBM Research at Austin,
- Sury Maturi (Executive Software Engineering Manager) at National Semiconductor Corp.,
- Dr. Larry Jones (Manager, Physical Design Technology Group) at Motorola.

We expect that our working relations with these companies and groups will continue and be strengthened if the proposed effort is funded by SRC. We will also be glad to work with other SRC companies on the topics related to the proposed research.

3 Personnel

3.1 Curriculum Vitae of PI

Jason Cong received his B. S. degree in computer science from the Peking University in 1985, and his M. S. and Ph. D. degrees in computer science from the University of Illinois at Urbana-Champaign in 1987 and 1990, respectively. Currently, he is a Professor and Co-Director of VLSI CAD Laboratory in the Computer Science Department of University of California, Los Angeles.

Dr. Cong's research interests include layout synthesis and logic synthesis for high-performance low-power VLSI circuits, design and optimization of high-speed VLSI interconnects, FPGA synthesis, rapid prototyping, and reconfigurable computing. He has published over 100 research papers and led over 20 research projects funded by DARPA, NSF, California MICRO program, and a number of industrial sponsors in these areas. He served as the General Chair of 1993 ACM/SIGDA Physical Design Workshop, the Program Chair and the General Chair of 1997 and 1998 International Symposiums on FPGAs, respectively, and in program committees of a number of VLSI CAD conferences, including DAC, ICCAD, and ISCAS. He is an Associate Editor of ACM Trans. on Design Automation of Electronic Systems. He serves on the ACM/SIGDA Advisory Board and has been a consultant to the Intel Corporation since 1994.

Dr. Cong received the Best Graduate Award from the Peking University in 1985. He received the Ross J. Martin Award for Excellence in Research from the University of Illinois at Urbana-Champaign in 1989. He received the National Science Foundation Research Initiation Award in 1991 and the National Science Foundation Young Investigator Award in 1993. He received the Northrop Corporation Outstanding Junior Faculty Research Award from UCLA in 1993. He received IEEE Trans. on CAD Best Paper Award from the IEEE Circuit and System Society in 1995.

Selected Publications

1. Cong, J. and C. L. Liu, "On the Over-the-Cell Channel Routing Problem". *IEEE Trans. Computer-Aided Design*, April, 1990, Vol. 9, pp. 408–418. (**1992 IEEE CAS Outstanding Young Author Award Candidate**)
2. Cong, J. and C. L. Liu, "On the k-Layer Planar Subset and Topological Via Minimization Problems". *IEEE Trans. on Computer-Aided Design*, Aug. 1991, Vol. 10, pp. 972–981.
3. Cong, J., "Pin Assignment with Global Routing for General Cell Design". *IEEE Trans. on Computer-Aided Design*, Nov. 1991, Vol. 10, pp. 1401–1412.
4. Cong, J., A. Kahng, G. Robins, M. Sarrafzadeh and C. K. Wong, "Provably Good Performance-Driven Global Routing". *IEEE Trans. on Computer-Aided Design*, June 1992, Vol. 11, No. 6, pp. 739–752.
5. Khoo, K. Y. and J. Cong, "A Fast Multilayer General Area Router for MCM Designs". *IEEE Trans. on Circuits and Systems (Special Issue on Simulation, Modeling, and Electrical Design of High-Speed and High-Density Interconnects)*, Nov. 1992, pp. 841–851.
6. Cong, J., M. Hossain and N. Sherwani, "A Provably Good Multilayer Topological Planar Routing Algorithm In IC Layout Designs". *IEEE Trans. on Computer-Aided Design*, Jan. 1993, pp. 70–78.
7. Cong, J., B. Preas and C. L. Liu, "Physical Models and Efficient Algorithms for Over-the-Cell Routing in Standard Cell Designs". *IEEE Trans. on Computer-Aided Design*, May 1993, pp. 723–734.
8. Cong, J., A. B. Kahng and G. Robins, "Matching-Based Methods for High-Performance Clock Routing". *IEEE Trans. on Computer-Aided Design*, Aug. 1993, Vol. 12, No. 8, pp. 1157–1169.
9. Cong, J. and Y. Ding, "FlowMap: An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup-Table Based FPGA Designs". *IEEE Trans. on Computer-Aided Design*, Jan. 1994, Vol. 13, No. 1, pp. 1–12. (**1995 IEEE Trans. on Computer-Aided Design Best Paper Award**)

10. Cong, J. and C. K. Koh, "Simultaneous Driver and Wire Sizing for Performance and Power Optimization". *IEEE Trans. on VLSI Systems*, Dec. 1994, pp. 408–425.
11. Cong, J. and K. S. Leung, "Optimal Wiresizing Under Elmore Delay Model". *IEEE Trans. on Computer-Aided Design*, Mar. 1995, pp. 321–336.
12. Khoo, K. Y. and J. Cong, "An Efficient Multilayer MCM Router Based on Four-Via Routing". *IEEE Trans. on Computer-Aided Design*, Oct. 1995, pp. 1277–1290.
13. Cong, J., W. J. Labio, and N. Shivakumar "Multiway VLSI Circuit Partitioning Based on Dual Net Representation". *IEEE Trans. on Computer-Aided Design*, April, 1996, pp. 396–409.
14. Cong, J. and L. He, "Optimal Wiresizing for Interconnects with Multiple Sources", *ACM Trans. on Design Automation of Electronic Systems*, Vol. 1, No. 4, Oct. 1996, pp. 478–511.
15. Cong, J., L. He, C. K. Koh, ad P. Madden, "Performance Optimization of VLSI Interconnect Layout", *Intergration, the VLSI Journal*, Vol. 21, 1996, pp. 1–94.
16. Cong, J. and B. Preas, "A New Algorithm for Standard Cell Global Routing". *Proc. Int'l Conf. on Computer-Aided Design*, Nov., 1988, pp. 176–179. (**Highlighted paper**)
17. Dong, S., J. Cong and C. L. Liu, "Constrained Floorplan Design for Flexible Blocks". *Proc. Int'l Conf. on Computer-Aided Design*, Nov., 1989, pp. 488–491.
18. Cong, J., L. Hagen, and A. Kahng, "Net Partitions Yield Better Module Partitions". *Proc. ACM/IEEE 29th Design Automation Conference*, June 1992, pp. 47–52. (**Best Paper Award Candidate**)
19. Boese, D., J. Cong, A. Kahng, K. S. Leung, and D. Zhou, "On High-Speed VLSI Interconnects: Analysis and Design". *Proc. IEEE Asia-Pacific Conference on Circuits and Systems*, Dec. 1992, pp. 35–40. (**Invited paper**)
20. Cong, J., K. S. Leung, and D. Zhou, "Performance-Driven Interconnect Design Based on Distributed RC Delay Model", *Proc. ACM/IEEE 30th Design Automation Conference*, June 1993, 606–611.
21. Cong, J. and M. Smith, "A Parallel Bottom-up Clustering Algorithm with Applications to Circuit Partitioning in VLSI Designs", *Proc. ACM/IEEE 30th Design Automation Conference*, June 1993, 755–760.
22. Cong, J., Z. Li, and R. Bagrodia, "Acyclic Multiway Partitioning of Boolean Networks", *Proc. 31st IEEE/ACM Design Automation Conf.*, June 1994, pp. 670–675.
23. Cong, J. and C. K. Koh, "Minimum-Cost Bounded-Skew Clock Routing", *Proc. Int'l Symp. on Circuits and Systems*, Seatle, Washington, May 1995, pp. 215–218.
24. Cong, J. and P. Madden, "Performance Driven Routing with Multiple Sources", *Proc. Int'l Symp. on Circuits and Systems*, Seatle, Washington, May 1995, pp. 203–206.
25. Cong, J. and Dongmin Xu, "Exploiting Signal Flow and Logic Dependency in Standard Cell Placement", *Proc. Asia and South Pacific Design Automation Conf.*, Chiba, Japan, Aug. 1995, pp. 399–404.
26. Cong, J., A. B. Kahng, C. K. Koh, and C. W. Tsao, "Bounded-Skew Clock and Steiner Routing Under Elmore Delay", *Proc. Int'l Conf. on Computer-Aided Design*, Nov. 1995, 66–71.
27. Okamoto, T. and J. Cong, "Buffered Steiner Tree Construction with Wire Sizing for Interconnect Layout Optimization", *Proc. IEEE Int'l Conf. on Computer-Aided Design*, San Jose, CA., Nov. 1996, pp. 44–49.
28. Cong, J. and L. He "An Efficient Approach to Simultaneous Transistor and Interconnect Sizing", *Proc. IEEE Int'l Conf. on Computer-Aided Design*, San Jose, CA., Nov. 1996, pp. 181–186.
29. Cong, J., "Modeling and Layout Optimization of VLSI Devices and Interconnects In Deep Submicron Design", *Proc. Asia and South Pacific Design Automation Conf.*, Chiba, Japan, Jan. 1997, pp. 121–126. (**Invited Talk**)
30. J. Cong and L. He. Simultaneous transistor and interconnect sizing based on the general dominance property. In *Proc. ACM SIGDA Workshop on Physical Design*, pages 34–39, Apr. 1996.

31. J. Cong, C.-K. Koh, and K.-S. Leung. Simultaneous buffer and wire sizing for performance and power optimization. In *Proc. Int. Symp. on Low Power Electronics and Design*, pages 271–276, Aug. 1996.

32. J. Cong and L. He. An efficient approach to simultaneous transistor and interconnect sizing. In *Proc. Int. Conf. on Computer-Aided Design*, pages 181–186, Nov. 1996.

33. C.C. Chang and J. Cong. An efficient approach to multi-layer layer assignment with an application to via minimization. In *Proc. Design Automation Conf*, pages 600–603, 1997.

34. J. Cong, L. He, A. B. Kahng, D. Noice, Shirali N., and S. H.-C. Yen. Analysis and justification of a simple, practical 2 1/2-d capacitance extraction methodology. In *Proc. Design Automation Conf*, pages 627–632, 1997.

35. J. Cong, L. He, C.-K. Koh, and Z. Pan. Global interconnect sizing and spacing with consideration of coupling capacitance. In *Proc. Int. Conf. on Computer Aided Design*, pages 628–633, 1997.

36. J. Cong and C.-K. Koh. Interconnect layout optimization under higher-order RLC model. In *Proc. Int. Conf. on Computer Aided Design*, pages 713–720, 1997.

37. J. Cong, H. P. Li, S. K. Lim, T. Shibuya, and D. Xu. Large scale circuit partitioning with loose/stable net removal and signal flow based clustering. In *Proc. Int'l Conf. on Computer-Aided Design*, pages 441–446, 1997.

38. J. Cong and L. He. An efficient technique for device and interconnect optimization in deep submicron designs. In *Proc. Int. Symp. on Physical Design*, April 1998.

4 Financial

See attached forms.