A Provably Passive and Cost Efficient Model for Inductive Interconnects

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***Abstract*— To reduce the model complexity for inductive interconnects, the vector potential equivalent circuit (VPEC) model was introduced recently and a localized VPEC model was developed based on geometry integration. In this paper, we show that the localized VPEC model is not accurate for interconnects with non-trivial sizes. We derive an accurate VPEC model by inverting inductance matrix under the partial element equivalent circuit (PEEC) model, and prove that the effective resistance matrix under the resulting full VPEC model is *passive and strictly diagonal dominant*. This diagonal dominance enables truncating small-valued off-diagonal elements to obtain a sparsified VPEC model named truncated VPEC (tVPEC) model with guaranteed passivity. To avoid inverting the entire inductance matrix, we further present another sparsified VPEC model with preserved passivity, the windowed VPEC (wVPEC) model based on inverting a number of inductance sub-matrices. Both full and sparsified VPEC models are SPICE compatible. Experiments show that the full VPEC model is as accurate as the full PEEC model but consumes less simulation time than the full PEEC model does. Moreover, the sparsified VPEC model is orders of magnitude (1000X) faster and produces waveform with small errors (3%) compared to the full PEEC model, and the wVPEC uses less (up to 90X) model building time yet is more accurate compared to the tVPEC model.**

Index Terms: **Circuit Simulation, Interconnect Modeling, Inductance Sparsification**

I. Introduction

As VLSI technology advances with decreasing feature size as well as increasing operating frequency, inductive effects of on-chip interconnects become increasingly significant in terms of delay variations, degradation of signal integrity and aggravation of signal crosstalk [1], [2]. Since inductance is defined with respect to the closed current loop, the loop-inductance extraction needs to simultaneously specify both the signal-net current and its returned current. To avoid the difficulty of determining the path of the returned current, the Partial Element Equivalent Circuit (PEEC) model [3] can be used, where each conductor forms a virtual loop with the infinity and the *partial inductance* is extracted.

To accurately model inductive interconnects in the high frequency region, RLCM (M here stands for mutual inductance) networks under the PEEC formulation are generated from discretized conductors by volume decomposition according to the skin-depth and longitudinal segmentation according to the wavelength at the maximum operating frequency. The extraction based on this approach [4]–[6] has high accuracy but typically results in a huge RLCM network with densely coupled partial inductance matrix L. A dense inductively coupled network sacrifices the sparsity of the circuit matrix and slows down the circuit simulation or makes the simulation infeasible. Because the primary complexity is due to the dense inductive coupling, efficient yet accurate inductance sparsification becomes a need for extraction and simulation of inductive interconnects in the high-speed circuit design.

Because the partial inductance matrix in the PEEC model is not diagonal dominant, simply truncating off-diagonal elements leads to negative eigenvalues and the truncated matrix loses passivity [7]. There are several inductance sparsification methods proposed with the guaranteed passivity. The return-limited inductance model [8] assumes that the current for a signal wire returns from its nearest power/ground (P/G) wires. This model loses accuracy when the P/G grid is sparsely distributed. The shift-truncation model [9] calculates a sparse inductance matrix by assuming that the current returns from a shell with shell radius r_0. But it is difficult to determine the shell radius to obtain the desired accuracy. Because the inverse of the inductance matrix, called K-element (susceptance) matrix is strictly diagonal dominant, off-diagonal elements can be truncated without affecting the passivity [10], [11]. Because K is a new circuit element not included in conventional circuit simulator such as SPICE, new circuit analysis tools considering K have been developed [12], [13]. Alternatively, the double-inversion based approaches have been proposed in [11], [14]. Using the control volume to extract adjacently coupled effective resistances to model inductive effects, the Vector Potential Equivalent Circuit (VPEC) model is recently introduced [15]. Its sparsified and SPICE-compatible circuit model is obtained based on a locality assumption that the coupling under the VPEC model exists only between adjacent wire filaments.

This paper presents an in-depth study on the VPEC model. We find that the locality assumption in [15] does not hold in general, and its integration-based extraction becomes impractical for large sized interconnects as it requires to optimize the size of the control volume for each filament. We rigorously derive an accurate full VPEC model considering the coupling between any pair of filaments by inverting the partial inductance matrix. We further prove that the resulting circuit matrix for the full VPEC model is passive and strictly diagonal dominant. The diagonal dominance enables truncating small-valued off-diagonal elements to obtain a sparsified VPEC model named truncated VPEC (tVPEC) model with guaranteed passivity. To avoid inverting the entire inductance matrix, we also present another sparsified VPEC model with preserved passivity, the windowed VPEC (wVPEC) model by

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inverting a number of inductance sub-matrices. Both full and sparsified VPEC models are SPICE compatible.

The rest part of the paper is organized as follows. In Section II, we introduce an accurate *inversion* based VPEC model with detailed derivation in the Appendix. The resulting full VPEC model considers coupling between any pair of filaments. In contrast, the VPEC model in [15] is integration based, localized but not accurate in general. In Section III, we prove that the effective resistance matrix $\hat{G}$ in the full VPEC model is passive and strictly diagonal dominant. In Section IV, we present a truncation-based sparsification that leverages the passivity of $\hat{G}$ matrix. It truncates small valued off-diagonal elements of the $\hat{G}$ matrix obtained from the full inversion of inductance matrix. In Section V, we further present a more efficient sparsification approach based on windowing. It avoids inverting the full inductance matrix, and is more efficient and more accurate compared to the truncation-based sparsification. In Section VI, we further present the scalability of the runtime and model size for the sparsified VPEC, full VPEC and PEEC model. Finally, we conclude the paper in Section VII.

II. Inversion Based Full VPEC Model

The VPEC model from [15] considering coupling only between adjacent filaments can be called *localized VPEC model*. In this section, we first derive the system equation of the full VPEC to model the inductive effect between any pair of filaments, and show that the localization assumption in [15] does not hold in general. We then introduce the inversion-based method to calculate the full VPEC model. Finally, we present experiments to show that the full VPEC is as accurate as the PEEC model.

A. Full Vector Potential Equivalent Circuit

Same as in FastHenry [5] with the magneto-quasi-static assumption, the conductor can be divided into a number of rectilinear *filaments*. The current density is *constant* over the cross-section of the filament. In this paper, we use superscripts x, y, z to denote spatial components of a vector variable. Let $\mathbf{A}$ be the *vector potential*, determined by the distribution of the current density J. Then J^k and A^k are the components in k-direction ($k = x, y, z$). We further use the subscript i for variables associated with filament a_i ($i \in N$), and every filament a_i has a length l by adequately discretizations in the k-direction. Table I summarizes the notations used in this paper with detailed definitions in the Appendix.

To extract the vector potential equivalent circuit, the integration-based approach in [15] needs to determine the *localized flux* $\mathcal{B}^k_{ij}$ ($j \in n_i$), where n_i is the set of filaments adjacent to a_i. The explicit calculation of $\mathcal{B}^k_{ij}$ is hard, and only considering the localized flux as in [15] loses the accuracy. The integration-based VPEC model in [15] needs to use a control volume for each filament, but no method was presented in [15] to find an accurate control volume. To avoid explicitly calculating $\mathcal{B}^k_{ij}$ and using the locality assumption, we derive a full VPEC model and then present an inversion-based extraction in Section II.B. The detailed derivation of the full

a_i	ith filament
A^k	kth component of vector potential A
A^k_i	kth component f of averaged A at a_i
$\mathcal{B}^k_{ij}$	kth component of the flux from a_i to a_j
$\mathcal{B}^k_{i0}$	kth component of the flux from a_i to vector potential ground;
I^k_i	kth component of electrical branch current at a_i
$\hat{I}^k_i$	kth component of magnetic branch current at a_i
R^k_{ij}	kth component of coupling effective resistance between a_i and a_j
$\hat{R}^k_{i0}$	kth component of ground effective resistance of a_i
V^k_i	kth component of electrical branch voltage at a_i
$\hat{V}^k_i$	kth component of magnetic branch voltage at a_i

TABLE I
TABLE OF NOTATIONS.

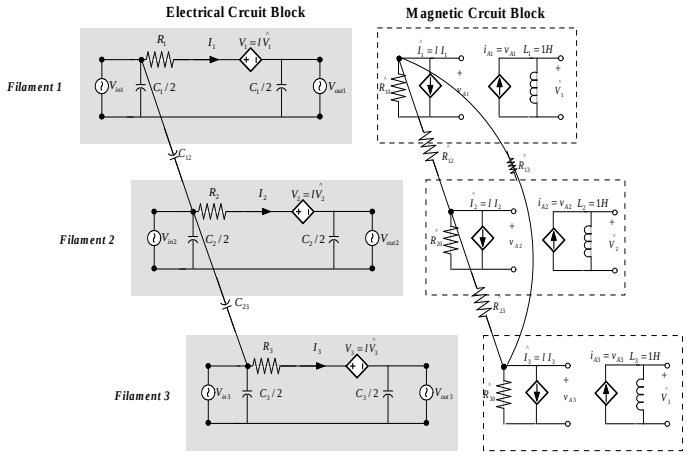

Fig. 1. The Vector Potential Equivalent Circuit model for three filaments.

VPEC model is presented in the Appendix, where we obtain following two KCL and KVL equations:

$$\frac{A^k_i}{\hat{R}^k_{i0}} + \sum_{j \neq i, i, j \in N} \frac{(A^k_i - A^k_j)}{\hat{R}^k_{ij}} = \hat{I}^k_i \tag{1}$$

$$\frac{\partial A^k_i}{\partial t} = \hat{V}^k_i \tag{2}$$

where the vector potential current and voltage are related to the electrical branch current and voltage by

$$\hat{I}^k_i = l I^k_i \qquad \hat{V}^k_i = V^k_i / l \tag{3}$$

Clearly, we can see the physical meaning of the effective resistance by equation (1): *Given a unit current change at ith filament, the vector potential observed at jth filament is exactly $\hat{R}^k_{ij}$ when all other filaments are connected to vector potential ground.* Furthermore, (2) describes the relation between the vector potential and its corresponding electrical voltage drop caused by inductive effect.

We present a SPICE compatible VPEC model for three filaments in Fig.1. The model consists of two blocks: the electrical circuit (PEEC resistance and capacitance) and the magnetic circuit (VPEC effective resistance and unit inductance). They are connected by the controlled sources. It includes following components:

1) The resistance R_i and capacitance C_i in the electrical circuit are the same as those in the PEEC model;
2) A dummy voltage source to sense current I_i^k in the electrical circuit controls $\hat{I}_i^k$ in the magnetic circuit (see (32) in the Appendix);
3) A voltage controlled current source is used to relate $\hat{V}_i^k$ and $\hat{I}_i^k$ with gain $g = 1$ in the magnetic circuit;
4) A voltage source V_i^k in the electrical circuit is controlled by $\hat{V}_i^k$ in the magnetic circuit (see (34) in the Appendix);
5) Effective resistances including ground $\hat{R}_{i0}^k$ and coupling $\hat{R}_{ij}^k$ (see (30) and (29) in the Appendix) are used to represent the strength of inductances in the magnetic circuit;
6) A unit inductance L_i in the magnetic circuit is to: (i) take into account time derivative of A_i^k (see (2)); and (ii) preserve the magnetic energy from electrical circuit.

Although the number of magnetic circuit blocks increases with more filaments, sparsified VPEC models will be introduced in Sections III - V to greatly reduce coupling resistances in magnetic circuit blocks with preserved passivity. Moreover, because the VPEC model largely reduces reactive elements (i.e. inductance) and its effective resistance is less densely stamped in the MNA (modified nodal analysis) matrix compared to the partial inductance under the PEEC model, the full VPEC model reduces the simulation time compared to the PEEC model (See experiments in Section VI).

Note that the summation in KCL (1) for the full VPEC model is carried out over each pair of filaments. In contrast, this summation in [15] is carried out only for adjacent filaments. The author of [15] obtained the localized model by modeling the flux $\mathcal{B}_{ij}^k$ as a "current" flow through $\hat{R}_{ij}^k$. It is based on the analogy with the conducting current flow at a surface S (*Ohm's Law*):

$$\mathbf{I} = -\sigma \int_S \nabla\phi \cdot d\mathbf{S} \tag{4}$$

(4) means the conducting current $\mathbf{I}(x, y, z)$ is locally related to the flux of the electrical field $\mathbf{E}(x, y, z)$ $(-\nabla\phi)$ on the surface S. (4) is correct because electrons only locally transport in the conductor. However, for the magnetic coupling problem, the flux $\mathcal{B}_{ij}^k$ is caused by the magnetic field that is not localized. Therefore, we still need non-local resistances to accurately model the long-range effect of inductance. Hence the KCL equation (1) in our paper is related to not only the localized $\hat{R}_{ij}^k$ $(j \in n_i)$, but also all other $\hat{R}_{ij}^k$ $(j \neq i, j \in N)$. The experimental results below will show that compared to the PEEC model, the full VPEC model considering all filaments is accurate, but not the localized VPEC model from [15].

B. VPEC via PEEC Inversion

Due to the difficulty to explicitly determine $\mathcal{B}_{ij}^k$, there is no efficient calculation method for effective resistances in [15]. In this part, we will derive the circuit-level system equation based on the VPEC effective resistance matrix $\hat{G}$, and then present an efficient method to calculate effective resistances from the inversion of the partial inductance matrix.

We take the time derivative at both sides of (1) and then use (2) to replace the time derivative of vector potential. Consequently, we obtain:

$$(\frac{1}{\hat{R}_{i0}^k} + \sum_{j\neq i} \frac{1}{\hat{R}_{ij}^k})V_i^k + \sum_{j\neq i}(-\frac{1}{\hat{R}_{ij}^k})V_j^k = l^2 \frac{\partial I_i^k}{\partial t} \tag{5}$$

We define the circuit matrix $\hat{G}$ of VPEC model

$$\hat{G}_{ij}^k = -\frac{1}{\hat{R}_{ij}^k}, \qquad \hat{G}_{ii}^k = (\frac{1}{\hat{R}_{i0}^k} + \sum_{j\neq i} \frac{1}{\hat{R}_{ij}^k}) \tag{6}$$

Then, the system equations can be rewritten as:

$$\hat{G}_{ii}^k V_i^k + \sum_{j\neq i} \hat{G}_{ij}^k V_j^k = l^2 \frac{\partial I_i^k}{\partial t} \tag{7}$$

Compared to the system equation based on inductance matrix L^k and its inverse $S^k = (L^k)^{-1}$:

$$\begin{aligned} L_{ii}^k \frac{\partial I_i^k}{\partial t} + \sum_{j\neq i} L_{ij}^k \frac{\partial I_j^k}{\partial t} &= V_i^k \\ S_{ii}^k V_i^k + \sum_{j\neq i} S_{ij}^k V_j^k &= \frac{\partial I_i^k}{\partial t} \end{aligned} \tag{8}$$

we find that $\hat{G}^k$ and S^k only differ by a geometrical factor l^2:

$$\hat{G}^k = l^2 S^k \tag{9}$$

Therefore starting with the L matrix under the PEEC model, we first obtain the inverse of L, and then have the following extraction formula for $\hat{R}$ under the VPEC model:

$$\hat{R}_{ij}^k = -\frac{1}{l^2 S_{ij}^k}, \qquad \hat{R}_{i0}^k = \frac{1}{l^2 S_{ii}^k + \sum_{j\neq i} l^2 S_{ij}^k} \tag{10}$$

Because the major computation effort is the inversion of L matrix, we call this method as *inversion* based VPEC model, which leverages the existing PEEC extractor. In contrast, the localized VPEC model is *integration* based and it needs to explicitly calculate the local flux $\mathcal{B}_{ij}^k$ $(j \in n_i)$ from scratch, where its accuracy is sensitive to the size of the control volume during the integration [15]. Therefore, it has a high accuracy only for few number of filaments and needs to optimize the size of the control volume for each filament when system has large number of filaments. Clearly, it becomes impractical for the full-chip extraction.

Note that the above (7)-(10) can be used to derive the K-element (susceptance) based model in [10], [11] from first principles. Although K-element method and VPEC are both derived from the inverse of L, the VPEC model is realized quite differently from K-element: (i) the VPEC model is SPICE compatible but the K-element needs introduce the new circuit-element to the simulator; and (ii) the current K-element simulator is based on the nodal analysis [13], where

the admittance form of K-element is $\Gamma = A_l L^{-1} A_l^T / s$ (A_l is incident matrix for inductance) in frequency domain. Clearly, Γ matrix becomes indefinite when $s \to 0$. Therefore it will lose correct dc information. On the other hand, the VPEC model can be stamped in the MNA matrix with the correct dc information in both frequency and time-domain simulation [16], which enables the correct circuit-reduction [17] to further reduce the model order.

C. Accuracy Comparisons

In this part, we use the aligned parallel bus to compare the PEEC model with the full VPEC model and localized VPEC model.

1) PEEC model extraction: The experiment setting is illustrated as follows. We assume the copper conductor ($\rho = 1.7 \times 10^{-8}\Omega \cdot m$) and low-k ($\epsilon = 2$) dielectric. The conductor is volume-discretized according to the skin-depth and longitudinal segmented by one tenth of the wave length. The capacitance is extracted by a lookup table [18] interpolated from FastCap [4]. Because capacitive coupling is a short-range effect, only adjacent couplings are considered. The partial inductance is extracted by FastHenry [5] at 10GHz (as the maximum operating frequency), where each wire segment is modeled by one filament, and coupling between any pair of segments (including segments in a same line) is considered. We then generate the distributed π-type RLCM circuit under the PEEC model. Furthermore, interconnect driver and receiver are modeled by resistance $R_d = 120\Omega$ and loading capacitance $C_L = 10fF$. All circuit models are simulated by HSPICE on a SUN Ultra-5 workstation. Note that the same experiment setting is applied for all other experiments in this paper unless specified otherwise.

2) Simulation of aligned parallel bus: We consider a five-bit bus, with one-segment per line. Each bus line is $1000\mu m$ long, $1\mu m$ wide and $1\mu m$ thick. The space between lines is $2\mu m$. With the extracted RLCM parameters under the PEEC model, we further construct the full VPEC model (with coupling $\hat{R}_{ij}$ between all bits) from this paper, and the localized VPEC model (with coupling $\hat{R}_{ij}$ between adjacent bits) from [15]. We measured responses at far-end of all five bits, and compared waveforms of the second bit in Fig. 2 (a) and (b), for both time-domain and frequency domain simulations, where a 1-V step voltage with 10ps rising time is used for time-domain transient simulation, and a 1-V ac voltage for frequency-domain (1Hz $\sim$ 10GHz) simulation. Clearly, the full VPEC model and PEEC model obtain identical waveforms in both frequency and time domain simulations, but the localized VPEC model introduces non-negligible error and is not accurate compared to the PEEC model, where the time-domain response shows 15% waveform difference and the frequency-domain response shows large deviation beyond 5GHz.

Note that when the number of conductors is small, there is no simulation speedup observed. However, for larger sized interconnect examples in Sections IV - VI, the simulation time of the full VPEC model (without sparsification) is less than that for the PEEC model. The detailed analysis of complexity scaling can be found in Section VI. Furthermore, in our comparison, we did not use the implementation of the localized model from [15], which depends on the height of the integration box (i.e., the size of the controlled volume) and is an approximated solution without a method to find the accurate size of the controlled volume. Instead, we find an accurate full VPEC model and then only keep the adjacently coupled resistances to obtain an accurate localized VPEC model [1].

III. Inductance Sparsification under VPEC Model

In this section, we first derive the magnetic energy under the VPEC model and then prove that the circuit matrix $\hat{G}$ under the VPEC model is positive definite. Moreover, we prove that $\hat{G}$ is also strictly diagonal dominant. This property enables the passivity preserved matrix sparsification methods. Finally, we present our sparsification flow for the VPEC model.

A. Magnetic Energy in VPEC Model

Generally, the magnetic energy is given by the following space integral [19]:

$$\begin{aligned} u_m &= \frac{1}{2}\int_\tau \mathbf{A}\cdot\mathbf{J}d\tau \\ &= \sum_{k=x,y,z} u_m^k \end{aligned} \tag{11}$$

For the full VPEC model, (11) can be rewritten by:

$$\begin{aligned} u_m^k &= \frac{1}{2}\int_\tau A^k J^k d\tau \\ &= \frac{1}{2}\sum_i A_i^k \cdot l \cdot I_i^k \\ &= \frac{1}{2}\sum_i A_i^k \hat{I}_i^k \end{aligned} \tag{12}$$

Furthermore, when we rewrite the KCL equation (31) in terms of $\hat{G}$ matrix,

$$\sum_j G_{ij}^k A_i^k = \hat{I}_i^k \tag{13}$$

we have the following relation for the magnetic energy under the full VPEC model:

$$u_m^k = \frac{1}{2}\sum_{i,j} G_{ij}^k A_i^k A_j^k \tag{14}$$

Below we prove that the $\hat{G}$ matrix is positive definite.

[1] Based on the communication with the author of [15], the localized VPEC model used in this paper has a similar accuracy compared to the one used in [15].

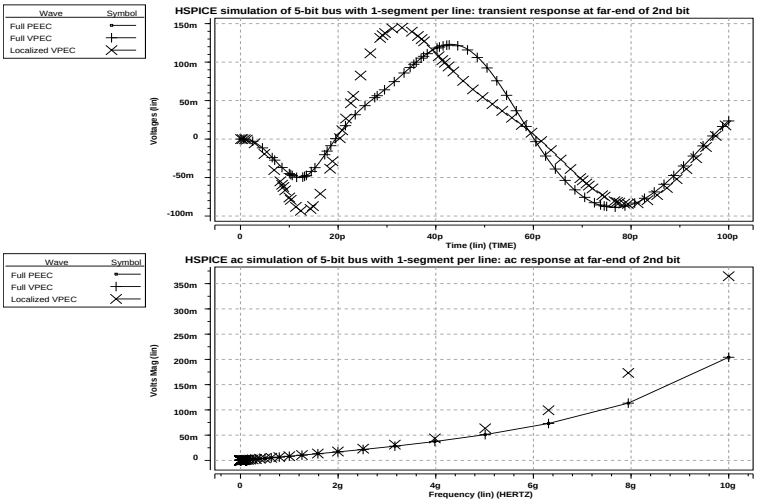

Fig. 2. For five-bit bus, (a) a 1-V step voltage with 10ps rising time and (b) a 1-V ac voltage are applied to the first bit and all other bits are quiet. The responses of the PEEC model, full VPEC model, and localized VPEC model are measured at the far end of the second bit.

B. Property of $\hat{G}$ Matrix

Theorem 1: Circuit matrix $\hat{G}^k$ $(k = x, y, z)$ in the VPEC model is positive definite.

Because $\hat{G}$ only differs from K matrix by a positive geometric constant, the proof of the matrix property (passivity and strict diagonal dominance) for K is equivalent for $\hat{G}$. The existing proofs in [10], [13] are based on the analogy: $[L] = \mu\epsilon[C^{-1}]$, which holds when $[C][L] = constant$. However, this relation does not hold in general as shown in [20]. Below, we present a direct proof for the VPEC model.

Proof: According to (14), because the energy u_m^k $(k = x, y, z)$ is positive, it automatically results in a positive definite matrix $\hat{G}^k$ [21].

Therefore, the corresponding VPEC model is passive. However, to further guarantee a passive model after truncating small-valued off-diagonal elements from the original positive definite matrix, we will prove that the matrix $\hat{G}$ is *strictly diagonal dominant* [21], i.e., $\hat{G}_{ii}^k > \sum_j |\hat{G}_{ij}^k|$.

Lemma 1: All the effective resistances $\hat{R}_{i0}^k$ and $\hat{R}_{ij}^k$ $(k = x, y, z)$ in the VPEC model are positive.

Proof: We present the proof based on the KCL equation (31). Since effective resistances are only determined by the geometry of the filaments, it will not depend on the applied external sources. Without loss of generality, we assume that an impulse current I_i^k is applied at filament a_i along z direction, and all other filaments a_j are connected to the vector potential ground. Note that for filament a_i, its average vector potential A_i^k is in the same direction of I_i^k; for any other grounded filament a_j, its average vector potential A_j^k is zero, but its *induced* current $-I_j^k$ is in the *opposite* direction to I_i^k according to *Lenz's Law*. Hence for filament a_j, (31) becomes

$$\frac{(A_j^k - A_i^k)}{\hat{R}_{ij}^k} = \frac{-A_i^k}{\hat{R}_{ij}^k} = -lI_j^k$$

where the induced current I_j^k is determined by the coupling flux between a_i and a_j. (15) can be further rewritten by:

$$\hat{R}_{ij}^k = \frac{A_i^k}{lI_j^k} > 0 \tag{15}$$

The positiveness of the ground resistance $\hat{R}_{i0}^k$ can be easily proved in a similar fashion. With this Lemma, we can further prove the following Theorem:

Theorem 2: Circuit matrix $\hat{G}^k$ $(k = x, y, z)$ in the VPEC model is strictly diagonal dominant.

Proof: According to (6) we have

$$\sum_{j \neq i} |\hat{G}_{ij}^k| = \sum_{j \neq i} \frac{1}{\hat{R}_{ij}^k} \tag{16}$$

and

$$\sum_{j \neq i} |\hat{G}_{ij}^k| < \frac{1}{\hat{R}_{i0}^k} + \sum_{j \neq i}^{N} \frac{1}{\hat{R}_{ij}^k} = \hat{G}_{ii}^k$$

or

$$\hat{G}_{ii}^k > \sum_{j \neq i} |\hat{G}_{ij}^k| \tag{17}$$

I.e., the circuit matrix $\hat{G}$ is strictly diagonal dominant. Note that truncating small off-diagonal entries from a strictly diagonal dominant matrix still leads to a positive definite matrix, i.e., a passive circuit model [21]. Based on Theorem 2, such a truncation-based sparsification still leads to passive circuit models. Intuitively, truncating small off-diagonal entries in $\hat{G}$ matrix (equivalent to truncating larger off-diagonal entries in $\hat{R}$ matrix) results in ignoring larger resistors in the equivalent resistance network. Because larger resistors are less sensitive to and also contribute less to current change, the resulting sparsified model can still have a good waveform accuracy as presented in Section IV. Moreover, our proof assumes that wires can be decomposed into short wires with a similar length. Therefore, in our experiments, we always segment

wires according to the one tenth of maximum operating frequency when wire lengths are different (see spiral inductor in Section V).

C. VPEC-Based Inductance Sparsification

With Theorem 2, we present the flow below for the inductance sparsification based on the VPEC model:

- Generate partial inductance matrix L by FastHenry or formula from [22], [23].
- (Option 1: truncated VPEC (tVPEC) model) Invert the full L matrix to obtain matrix $\hat{G}$, $\hat{R}$, and full VPEC model, and then generate sparsified VPEC model by truncating the full VPEC model.
- (Option 2: windowed VPEC (wVPEC) model) Find a sparse approximated inverse matrix S' of L to obtain $\hat{G}'$, $\hat{R}'$, and the sparsified VPEC model simultaneously.

Note that during the inductance extraction at low frequency, we assume each wire segment is modeled by one filament. When frequency is beyond 10GHz, the volume filament [5] or conduction mode [24] based decomposition can be applied to consider the skin and proximity effects. In this paper, we use the 3D frequency dependent solver FastHenry [5] to accurately extract the partial inductance matrix. Because inductance has weak dependence on geometry, the formula [23] or lookup-table [25] based approaches can be also applied to efficiently obtain the full-chip inductance.

As further discussed in Sections IV and V, we will apply two sparsifications that depend on the scale of the interconnect: (1) When the scale of interconnect is small (less than 1000 wires), the direct LU or Cholesky factorization based inversion is sufficiently efficient ($O(N^3)$), and we can apply the simple truncation-based sparsifications; (2) When the scale of interconnect is large, we extend a window-based extraction [11] to obtain a *sparse approximated inverse* of L and simultaneously extract a sparsified VPEC model. It reduces the computation expense to $O(Nb^3)$, where b is the size of the window. As shown by experiments, the windowed VPEC model also reduces the error introduced by the sparsification when compared to the truncated VPEC model.

IV. Truncated VPEC Model

In this section, we present the truncated VPEC (tVPEC) model. After the full inversion of L, we obtain a strictly diagonal dominant matrix $\hat{G}$. As explained in Section III, its small-valued off-diagonal elements can be truncated without loss of passivity. We present two truncating approaches below: the geometrical (gtVPEC) and numerical (ntVPEC) truncation. The first one is applicable to the aligned parallel bus, and the second is applicable to conductors of any shapes.

A. Geometrical Truncation

For the aligned parallel bus we can define a *truncating window* (N_W, N_L) for each wire segment, where N_W and N_L are the numbers of coupled segments in directions of wire width and length, respectively. The coupling along wire length is the *forward* coupling, and the one along wire width is the *aligned* coupling. Because of the symmetry introduced by aligning and paralleling, each wire segment will have the same sized truncating window. As a result, the tVPEC model only contains $\hat{R}_{ij}$ within the truncating window for each wire segment, and is called gtVPEC in Table II.

Models and Window Sizings	No. of Elements	Run-Time (s) and Speedup	Avg. Volt. Difference (V)	Standard Deviation (V)
Full PEEC	32896	2535.48 (1X)	0	0
Full VPEC(32,8)	32896	772.89 (3X)	1.00e-5	6.26e-4
gtVPEC(32,2)	11392	311.22 (8X)	5.97e-5	1.84e-3
gtVPEC(16,2)	3488	152.57 (16X)	-1.23e-4	4.56e-3
gtVPEC(8,2)	2240	85.14 (32X)	-2.17e-4	8.91e-3

TABLE II
SETTINGS AND RESULTS OF GEOMETRICAL tVPEC MODELS

We consider a 32-bit bus with 8-segments per line and four differently sized truncating windows: (32, 8), (32, 2), (16, 2) and (8, 2), and summarize the experiment setting and result in Table II. Clearly, there is a smooth trade-off between runtime and accuracy for different truncating window sizes, where the average voltage differences and associated standard deviations are calculated for all time steps in SPICE simulation. We first compare results of different truncating windows. The truncating window (8, 2) achieves the highest speedup of 30X and the largest difference of about 0.2mV on average, less than 2% of the noise peak, and the truncating window (32, 2) has the highest accuracy with 0.06mV on average but a reduced speedup of 10X. Furthermore, the small difference between windows (32, 8) and (32, 2) implies that the forward couplings between non-adjacent segments are negligible. However, an N_W larger than N_L (as shown in Table II) is needed to achieve a high accuracy. This implies that the aligned coupling is stronger than the forward coupling, and considering only the adjacent aligned coupling may lead to a large error.

B. Numerical Truncation

For the numerical truncation, we define the *coupling strength* as the ratio of an off-diagonal element to its correspondent diagonal element at each row of $\hat{G}$. We then truncate those off-diagonal elements with coupling strength smaller than a specified threshold.

Fig. 3 plots simulation results under the numerical sparsification for the non-aligned parallel bus with 128-bit and one segment per line. The sparse factor is the ratio between the numbers of circuit elements in the truncated and full VPEC models. The waveform difference is small in terms of the noise peak for sparse factors up to 30.5%. Table III summarizes the truncation setting and simulation result, where values in parentheses of column 1 are truncating thresholds, and the runtime includes both SPICE simulation and matrix inversion in case of VPEC models. One can see from the table that up to 30X speedup is achieved when the average waveform differences is up to 0.377mV, less than 1% of the noise peak. A larger speedup factor can be expected as a higher waveform difference can be tolerated in practice. We also compare the full VPEC model and the PEEC model. The full VPEC simulation is 7X faster and has a negligible waveform difference.

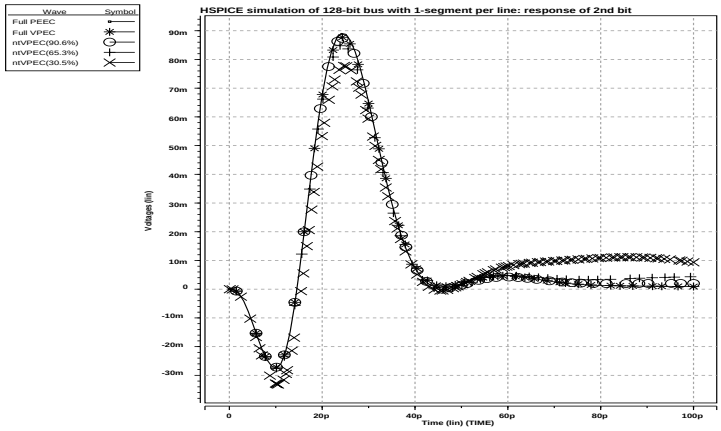

Fig. 3. For 128-bit bus by the numerical truncation, a 1-V step voltage with 10ps rising time is applied to the first bit, and all other bits are quiet. The responses of the PEEC model, the full VPEC model, and the tVPEC model are measured at the far end of second bit.

Models and Trunc-Thresholds	No. of Elements	Run-Time (s) and Speedup	Avg. Volt. Difference (V)	Standard Deviation (V)
Full PEEC	8256	281.02 (1X)	0	0
Full VPEC(0.0)	8256	36.40 (7X)	-1.64e-6	3.41e-4
ntVPEC(5e-5)	7482	30.89 (9X)	4.64e-6	4.97e-4
ntVPEC(1e-4)	5392	19.55 (14X)	1.29e-5	1.37e-3
ntVPEC(5e-4)	2517	8.35 (28X)	3.77e-4	5.20e-3

TABLE III

SETTINGS AND RESULTS OF NUMERICAL tVPEC MODELS

V. WINDOWED VPEC MODEL

The sparsification in Section IV needs the full matrix inversion and becomes computational expensive for the large sized interconnect. Furthermore, the directly truncated matrix $\hat{G}$ may be not accurate enough to represent the original full $\hat{G}$ matrix. As shown in [11] all entries of the L inverse matrix can be approximately reconstructed just from entries of the sub-matrices in L corresponding to the coupling window of the active aggressor. Using this windowing technique, we further present two windowed VPEC (wVPEC) models based on the geometry (gwVPEC) and numerical value (nwVPEC) respectively.

A. Geometrical Windowing

Owing to the regularity of the aligned parallel bus, we can also define a *coupling window* with uniform size b for each wire. For each wire in turn as the aggressor, we first construct N small sub-matrices (coupling windows) all with size b. Then we invert each sub-matrix and build a *sparse approximated inverse* for L. It is described in details as following two steps:

1) Sub-matrix Construction: For aggressor m and all its victims within a window of size b, we construct a sub-matrix $L^{(m)}$ that:

$$L_{ij}^{(m)} = \begin{cases} L_{ij} & \text{if (i, j) inside the window;} \\ 0 & \text{if (i, j) outside the window.} \end{cases}$$

We then solve vector $\mathbf{s}^{(m)}$ from: $L^{(m)}\mathbf{s}^{(m)} = \mathbf{i}^{(m)}$, where $\mathbf{i}^{(m)}$ is the unit vector, correspondent to applying a unit current source at mth aggressor, i.e., $\mathbf{i}_n^{(m)} = \delta_{mn}$. With further iterating above procedure for all conductors in turn as the active aggressor, we obtain N dimension-reduced vectors $\mathbf{s}^{(m)}$. Because this process is only related to the sub-matrix, the complexity of full inversion is reduced from $O(N^3)$ to $O(Nb^3)$ when b is small.

2) Heuristic Selection: We then merge all $\mathbf{s}^m$ vectors into one complete and sparse matrix S' that can approximate L^{-1}, the inverse of inductance matrix. The entry of S' is

$$S'_{mn} = S'_{nm} = max(\mathbf{s}_n^{(m)}, \mathbf{s}_m^{(n)}) \tag{18}$$

where $\mathbf{s}_n^{(m)}$ is the element between the mth aggressor and its nth victim inside the coupling window of the mth aggressor. Note that $\mathbf{s}_n^{(m)}$ is always negative with sufficient discretizations [13]. The circuit matrix of a stable system needs to be symmetric positive definite (s.p.d). This is guaranteed by the heuristic in (18). I.e., we always have

$$S'_{mm} \geq \sum_{n \neq m} |S'_{mn}| \tag{19}$$

As a result, we can construct the sparsified yet passive VPEC model based on (10) with this sparse approximated inverse S'.

We first compare the extraction efficiency of geometrical tVPEC and wVPEC models in Fig. 4 by extracting the VPEC model for buses up to 2000 bits. The size for geometrical truncation is (N_W, N_L) = (8, 1) and for the geometrical wVPEC is b = 8. The extraction time for truncation-based method includes the full inversion and truncation. When the scale of interconnects is small (below 128-bit), the truncation-based method is actually as efficient as the window-based method. But when the scale of interconnects becomes larger, the window-based extraction is faster than the truncation-based approach with a 90X speedup for the 2048-bit bus (8.6s vs. 543.1s). Therefore it is more efficient to apply the winnowed VPEC model for the large scale interconnects.

We further compare the waveform between the gtVPEC and wtVPEC models for the 128-bit bus with one segment per

Waveform Diff.(V)	b=64	b=32	b=16	b=8
gtVPEC (Avg.$\pm$ STD)	-3.47e-4 $\pm$ 2.74e-3	-5.19e-4 $\pm$ 4.85e-3	-6.32e-4 $\pm$ 6.72e-3	-1.57e-3 $\pm$ 1.06e-2
gwVPEC (Avg.$\pm$ STD)	-3.28e-4 $\pm$ 1.27e-3	-5.02e-4 $\pm$ 2.31e-3	-5.28e-4 $\pm$ 3.29e-3	-1.12e-3 $\pm$ 5.13e-3

TABLE IV

WAVEFORM ACCURACY COMPARISONS OF gtVPEC AND gwVPEC MODELS

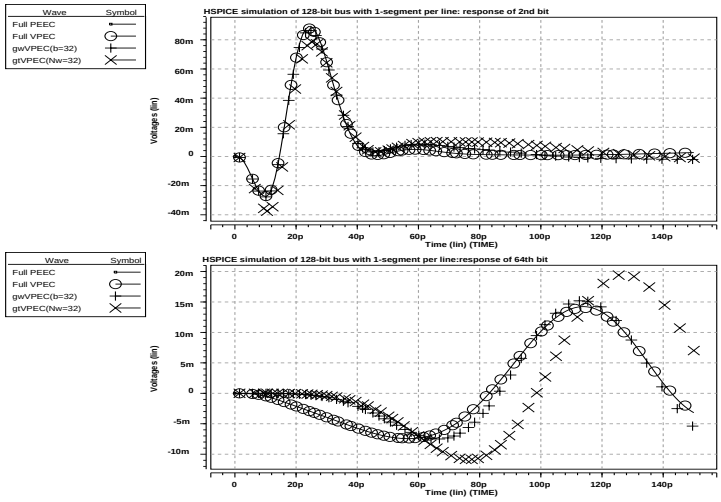

Fig. 5. For 128-bit bus by the geometrical windowing, a 1-V step voltage with 10ps rising time is applied to the first bit, and all other bits are quiet. The responses of the PEEC model, full VPEC model, gtVPEC model and gwVPEC model are measured at the far end of second bit and 64th bit respectively.

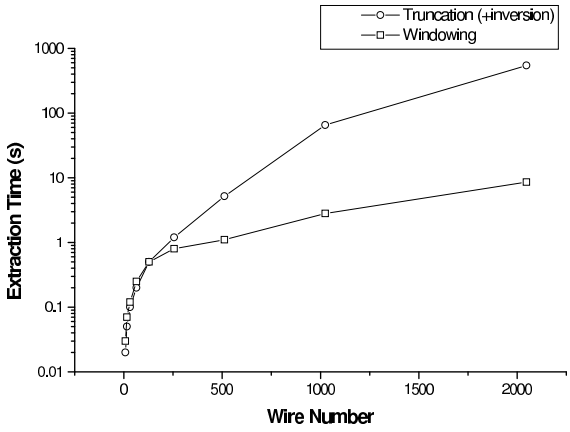

Fig. 4. Extraction time comparisons of bus lines with one segment each line using geometrical tVPEC and wVPEC models.

line. We apply a pulse voltage at the first bit, and observe the transient responses at the far ends of second and 64th bit bus, respectively. The window size is b = 32 for the gwVPEC model and $(N_W, N_L) = (32, 1)$ is set for the gtVPEC model to achieve the same sparsification ratio. Fig. 5 shows waveforms of the PEEC model, full VPEC model, gtVPEC model and gwVPEC model. Compared to accurate models such as the PEEC model and full VPEC model, gwVPEC model and gtVPEC model have virtually no error at the second bit bus. But for the 64th bit, the gtVPEC model has non-negligible error but the gwVPEC model still has a high accuracy. More accuracy comparisons are presented in Table IV by changing the window size b to 64, 32, 16, and 8, where the waveform difference is calculated from responses at far ends of the 64th bit between the sparsified VPEC models and PEEC model. We find that the window-based extraction has 2X higher accuracy than the truncation-based approach on average. It is due to the fact that the matrix element generated from windowing is interpolated with other elements in the inductance matrix.

B. Numerical Windowing

The coupling window usually has different sizes for different wires because the general layout does not have the regularity as the aligned parallel bus. Therefore, we need first determine the size of coupling window for each wire. Similar to the numerical truncation approach, we define the coupling strength as the ratio of an off-diagonal element to its correspondent diagonal element at each row of the L matrix. We then construct the coupling window by only considering those off-diagonal elements that have coupling strength larger than a specified threshold value. With the heuristic selection (18) we can build the sparse approximated inverse and consequently a sparsified VPEC model.

As an example shown in Fig. 6, we extract the partial inductance by FastHenry at 10GHz for a three-turn spiral inductor on the lossy substrate. The heavily doped substrate modeled as lossy ground plane with $\rho = 1.0 \times 10^{-5}\Omega \cdot m$. The metal is volume-discretized according to the skin-depth and longitudinal segmented by the one tenth of the wave length resulting 92 segments. The substrate is also discretized according to [26], and its contribution (Eddy current loss) is lumped to the segmented conductor on top of the substrate.

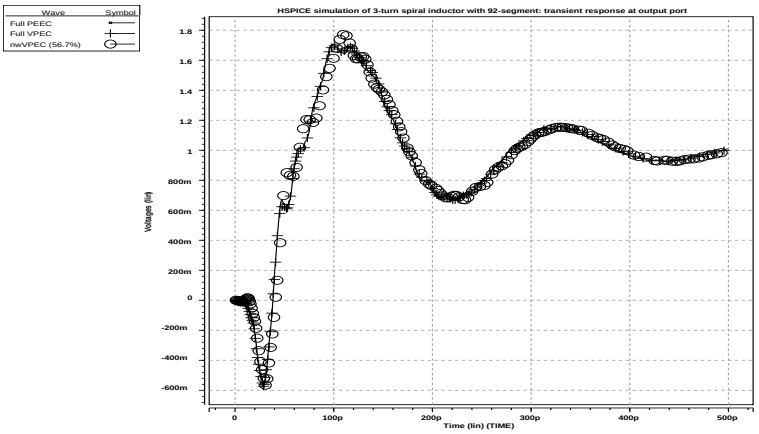

Fig. 7. For three-turn spiral inductor with 92 segments by the numerical windowing, a 1-V step voltage with 10ps rising time is applied to the input port. The responses of the PEEC model, full VPEC model and nwVPEC model are measured at the output port.

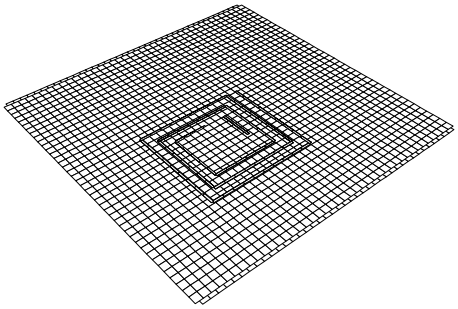

Fig. 6. Discretized spiral inductor on the lossy substrate for the generation of the distributed RLCM PEEC/VPEC model.

We construct the distributed RLCM PEEC model with 5120 circuit elements and then apply the numerical window-based method by setting the threshold as 1.5e-4. It results in a 56.7% sparsification ratio. To check the accuracy of the resulting model, we apply 1-V pulse voltage at input and observe the response at output port. Fig. 7 shows the waveforms obtained by the PEEC model, full VPEC model and nwVPEC model. The three waveforms are virtually identical to each other but the wVPEC model results in a 8X times runtime speedup compared to the full PEEC model (9.3s vs 70.5s).

VI. Complexity Scaling of VPEC Models

We further compare the runtimes and model size by extracting and simulating a number of aligned parallel buses using the PEEC model, full VPEC model, and gwVPEC model (b=8), respectively. The runtime for the full or wVPEC model includes both VPEC extraction and SPICE simulation time. The model size refers to the file size of the resulting SPICE netlists. We plot the runtime vs. the bus size in Fig. 8 (a) and the model size vs. the bus size in Fig. 8 (b).

Due to the additional introduced circuit elements, the size of SPICE netlist for full VPEC model is around 10% larger than the full PEEC model on average. Further when the scale of wire number is small, there is no runtime speedup observed for the full VPEC model. However, when the scale of wire becomes larger (greater than 64-bit), the runtime of

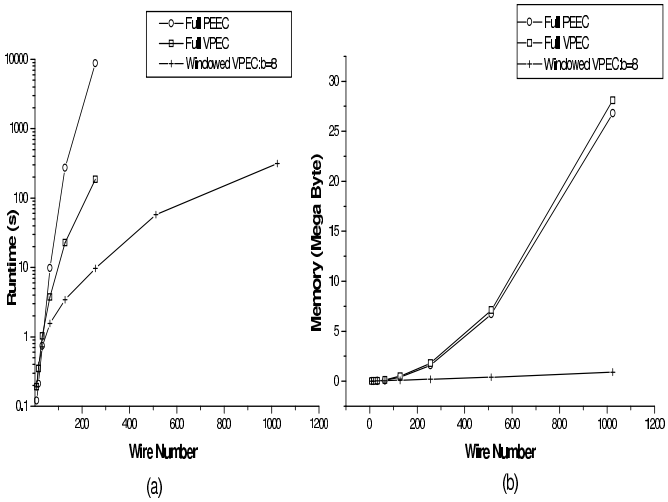

Fig. 8. Runtime and memory usage comparisons of bus lines with one segment each line using the PEEC model, full VPEC model, and gwVPEC model (b=8).

the full VPEC model is found 10X times faster than the PEEC model on average. For the 256-bit bus, the full VPEC model is 47X (185.39s vs. 8726.85s) faster than the PEEC model. This is due to the facts that: (i) its resultant network has fewer *reactive* elements (i.e. inductances); and (ii) its resultant MNA matrix in SPICE is sparser than the direct inductance formulation. SPICE converges faster with fewer time derivatives and integrals, and its internal sparse solver is more efficient for a less dense matrix.

Moreover, both the PEEC model and full VPEC model can only handle the bus circuit with up to 256-bit due to the memory limitation. On the other hand, the gwVPEC model (b=8) can handle larger size up to thousand bits. Moreover, it is easy to see that the scalability of the gwVPEC models shows a slow increase with respect to the increase of the bus line numbers. For example, it achieves over 1,000X (9.71s vs. 8726.85s) speedup for 256-bit bus in runtime compared to the

PEEC model. In all the simulation, the wVPEC model has a very small waveform difference (less than 3%) in terms of delay when compared to the PEEC model.

VII. Conclusions

Using the equivalent resistance network and controlled voltage and current sources to replace the inductance network, we develop the full VPEC model that is as accurate as the PEEC model but takes less simulation time. Although the full VPEC model has a slightly higher circuit complexity compared to the PEEC model, SPICE can handle the VPEC model more efficiently because the VPEC model has fewer reactive elements (i.e., inductances) and the modified nodal admittance matrix becomes sparser under VPEC model than that under the PEEC model.

Moreover, the resulting circuit matrix $\hat{G}$ for the equivalent resistance network in the full VPEC model is passive and strictly diagonal dominant. This enables truncation-based sparsification methods with guaranteed passivity. We have presented the truncation-based method and have achieved orders of magnitude speedup in circuit simulation with small errors compared to the PEEC model. Furthermore, the window-based extraction method has been developed to avoid the full inductance matrix inversion and can obtain a higher accuracy compared to the truncation-based approach. We have also shown that the matrix $\hat{G}$ can be used to justify the K-element or susceptance based simulation [10]–[14] from first principles. Note that SPICE is able to directly simulate VPEC model but not K-element based model.

The primary contribution of this paper is to derive the inversion based full VPEC model for multiple inductive interconnects and illustrate how to build sparsified VPEC for SPICE simulation with guaranteed passivity. To further reduce the complexity of the resulting sparsified VPEC models, we intend to develop model order reduction for the VPEC model.

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Appendix

To model the inductive effect, we start with differential Maxwell equations in terms of $\mathbf{A}$ [19]:

$$\nabla^2 A^k = -\mu J^k \tag{20}$$

$$\frac{\partial A^k}{\partial t} = -E^k \tag{21}$$

where the vector potential $\mathbf{A}$ is in the z-direction same as the current density $\mathbf{J}$, $\mathbf{E}$ is the electrical field, and μ is the

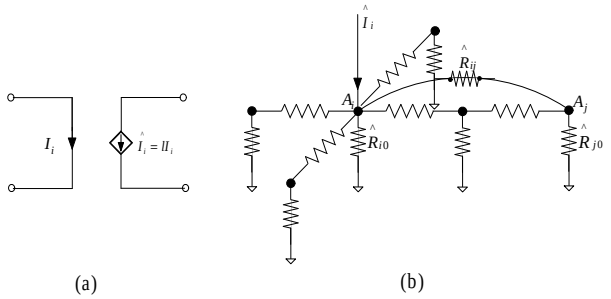

Fig. 9. (a) The electronic current controlled vector potential current source; (b) The Kirchoff current law for vector potential circuit. An invoking vector potential current source is employed at a_i, and the responding vector potential at a_j is A_j^k determined by the full effective resistance network.

permeability constant. Note that the resistive voltage drop by $(-\nabla^k \phi)$ is not included in (21) since we are interested in the inductive voltage drop here. Given the distribution of the current density J^k, the vector potential A^k is determined by

$$A^k = \frac{\mu}{4\pi} \int \frac{J^k}{|\mathbf{r} - \mathbf{r}_i'|} d\tau(\mathbf{r}_i') \tag{22}$$

To construct the system equation in form of the integral equation, we apply the volume and line integration to (20) and (21) respectively. For filament a_i, when (20) is integrated within the volume τ_i of filament a_i, using *Gauss' Law*:

$$\int_S \mathbf{a} \cdot d\mathbf{S} = \int_\tau \nabla \cdot \mathbf{a} d\tau, \tag{23}$$

we can obtain

$$\begin{aligned} -\mu \int_{\tau_i} J^k d\tau &= \int_{S_i} \nabla A^k \cdot d\mathbf{S} \\ &= \mathcal{B}_{i0}^k + \sum_{j \neq i} \mathcal{B}_{ij}^k \end{aligned} \tag{24}$$

Note that the surface integral $\int_{S_i} d\mathbf{S} \cdot \nabla A^k$ is actually the *flux of the gradient of kth component of the vector potential* caused by the filament current of a_i in τ_i. It consists of following parts [15]: (i) the flux to the infinity (vector potential ground) $\mathcal{B}_{i0}^k$

$$\mathcal{B}_{i0}^k = \int_{S_{i0}} \nabla A^k \cdot d\mathbf{S}, \tag{25}$$

and (ii) the flux to all other filaments a_j $(j \in N, j \neq i)$ $\mathcal{B}_{ij}^k$

$$\mathcal{B}_{ij}^k = \int_{S_{ij}} \nabla A^k \cdot d\mathbf{S}. \tag{26}$$

However, to explicitly determine the value of $\mathcal{B}_{ij}^k$ is difficult because it is hard to partition the flux between filament a_i, all other filament a_j, and the vector potential ground.

Moreover, integrating (21) along the projected length in k-direction of filament a_i leads to:

$$\int_{l_i} \frac{\partial A^k}{\partial t} dl = -\int_{l_i} E^k \cdot dl \tag{27}$$

Based on (24) and (27), we can further construct the circuit-level system equation in the matrix form. By defining the *filament vector potential* [15] as the *average* volume integral of A^k within τ_i (surrounded by the surface S_i):

$$A_i^k = \frac{1}{\tau_i} \int_{\tau_i} A^k(\mathbf{r}) d\tau(\mathbf{r}) \tag{28}$$

We can define an effective coupling resistance

$$\hat{R}_{ij}^k = -\mu \frac{(A_i^k - A_j^k)}{\mathcal{B}_{ij}^k} \tag{29}$$

to model (i.e., replace) the mutual inductive coupling between a_i and a_j. In addition, there also exists an effective ground resistance to model the self inductive effect:

$$\hat{R}_{i0}^k = -\mu \frac{A_i^k}{\mathcal{B}_{i0}^k} \tag{30}$$

Because the filament current is invariant along k-direction, the volume integral of the current density inside the volume τ_i is reduced to lI_i^k, where I_i^k is the electrical current at the cross section of a_i. Therefore (24) becomes the *Kirchoff Current Law* (KCL) under the full VPEC model:

$$\frac{A_i^k}{\hat{R}_{i0}^k} + \sum_{j \neq i} \frac{(A_i^k - A_j^k)}{\hat{R}_{ij}^k} = lI_i^k \tag{31}$$

where a vector potential current source $\hat{I}_i^k$ can be defined:

$$\hat{I}_i^k = lI_i^k \tag{32}$$

which is controlled by the electrical current I_i^k. An equivalent circuit to illustrate the VPEC KCL equation (31) is shown in Fig. 9. Clearly, we can see the physical meaning of the effective resistance: *Given a unit current change at ith filament, the vector potential observed at jth filament is exactly $\hat{R}_{ij}^k$ when all other filaments are connected to vector potential ground.*

Similarly for (27), we have the following *inductive* nodal voltage equation:

$$l \frac{\partial A_i^k}{\partial t} = {V_i}^k \tag{33}$$

which describes the relation between the vector potential and its corresponding electrical voltage drop caused by inductive effect. As a result, a voltage-controlled vector potential voltage source $\hat{V}_i^k$ is:

$$\hat{V}_i^k = V_i^k / l \tag{34}$$