Vector Potential Equivalent Circuit Based on PEEC Inversion

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***Abstract*— The geometry-integration based vector potential equivalent circuit (VPEC) was introduced to obtain a localized circuit model for inductive interconnects in [1]. In this paper, we show that the method in [1] is accurate only for the two-body problem. We derive N-body VPEC models based on geometry integration and inversion of inductance matrix under the PEEC model, respectively. Both VPEC models are derived from first principles and are accurate compared to the full PEEC model. The resulting circuit matrix $\hat{G}$ can be analyzed directly by existing simulation tools such as SPICE, and the simulation time of VPEC model is $47X$ smaller than that for PEEC model for a bus structure with 256 wire segments. It is also passive and strictly diagonal dominant, which leads to efficient circuit sparsification methods such as numerical and geometry based sparsifications. Compared to the full PEEC model, the sparsified VPEC models are orders of magnitude faster and produce waveforms with very small error.**

I. Introduction

As VLSI technology advances with decreasing feature size as well as increasing operating speed and global interconnect length, an increasing portion of interconnects should be modeled as RLC circuits [2]. Although these interconnects can be accurately modeled by Partial Element Equivalent Circuit (PEEC) [3], the resulting full PEEC circuit may have an extremely high complexity for circuit analysis. Because the partial inductance matrix in PEEC is not diagonal dominant, simply truncating off-diagonal elements leads to negative eigenvalues such that the truncated matrix loses the property of passivity [4]. Several inductance sparsification methods have been proposed with guaranteed passivity. The return-loop inductance model [5] assumes that the current for a signal wire returns from the nearest ground wires sandwiching the signal wire. It loses accuracy by ignoring coupling between signal wires not in the same "halo". The shift-truncation model [6] directly calculates a sparse inductance matrix by assuming that the current returns from a shell with radius r_0. However, it is difficult to define r_0 to obtain the desired accuracy. The inverse-truncation model [7] replaces the inductance matrix by its inversion, called K matrix or susceptance. K matrix is diagonal dominant and small-valued off-diagonal elements can be truncated without affecting the passivity. Because K is a new circuit element that is not considered in conventional circuit analysis such as SPICE, new circuit analysis tools need to be developed [8]. Further, inversion of truncated K matrix is proposed to avoid using K in simulation [9], and wire duplication is used to construct a complexity-reduced circuit that is equivalent to the circuit under the inductance matrix or under the truncated K matrix [10].

Using equivalent magnetic resistance to model inductive interconnects, the geometry-integration based vector potential equivalent circuit (VPEC) is introduced in [1]. The resulting circuit model can be analyzed by SPICE, and shows a good potential for circuit sparsification. This paper presents an in-depth study on VPEC. In Section 2, we show that the VPEC method in [1] is accurate only for the two-body problem, and derive an accurate N-body VPEC models based on geometry integration. In Section 3, we introduce a new N-body VPEC model using inversion of inductance matrix under the PEEC model. Both VPEC models are derived from first principles and are accurate compared to the full PEEC model. The integration based VPEC model needs a FastHenry [11]-like three-dimensional field solver developed from scratch, but the inversion based VPEC model can be easily obtained using the partial inductance matrix generated by FastHenry. Further, we prove that the circuit matrix $\hat{G}$ resulting from the VPEC model is passive and strictly diagonal dominant. As a by-product, the $\hat{G}$ matrix can be used to justify from first principles the K matrix (or susceptance) based sparsification methods. In Section 4, we present efficient circuit sparsification methods leveraging the passivity of $\hat{G}$ matrix. We conclude the paper in Section 5.

II. Integration Based VPEC

In this section, we first use the two-body problem to illustrate the concept of VPEC model, then extend VPEC to the N-body problem.

A. Two-Body Problem

Same as in FastHenry [11], the long and thin conductor in integrated circuits can be divided into a number of rectilinear *filaments*. Given the magneto-quasi-static assumption, the current is *constant* in the current direction assumed as z-axis in this paper, and it is uniform over the cross-section of the current flow (i.e., uniform over the cross-section of filament). For VPEC, the region of filament is extended to include the space between two adjacent filaments as shown in Fig. 1, such that the two extended regions touch each other. To be precise, we call the extended filament as *hyper-filament* (in short, *h-filament*). If the original filaments already touch each other, the h-filaments are equivalent to the filaments. In this paper, we use the superscripts x, y, z to denote spacial components of a vector variable. Let $\mathbf{A}$ be the *vector potential*, then A^z

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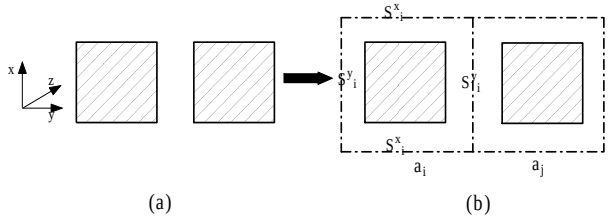

Fig. 1. Expansion of two filaments in (a) to hyper-filaments in (b). The surface S_i^y locates in the middle of two h-filaments.

is its z-direction component. We use the subscripts i and j for variables associated with h-filaments a_i and a_j. Without loss of generality, two h-filaments with cross-section in $x-y$ plane and an identical length l in z-direction are studied in the two body problem. We start with the differential Maxwell equations in the formalism of A^z:

$$\nabla^2 A^z = -\mu J^z \tag{1}$$

$$\frac{\partial A^z}{\partial t} = -E^z - \nabla^z \phi \tag{2}$$

where the vector potential $\mathbf{A}$ is in z-direction same as current density $\mathbf{J}$, $\mathbf{E}$ is electrical field, and ϕ is the scalar potential. Because $J^z = J_i^z + J_j^z$, the total vector potential is $A^z = A_i^z + A_j^z$, where A_i^z is determined by J_i^z of h-filament a_i:

$$A_i^z = \frac{\mu}{4\pi} \int d\mathbf{r}_i' \frac{J_i^z}{|\mathbf{r} - \mathbf{r}_i'|} \tag{3}$$

where $|\mathbf{r} - \mathbf{r}_i'|$ is the distance between the source and destination points. A_j^z of h-filament a_j can be obtained similarly. Furthermore if (1) is integrated within the volume Ω_i of h-filament a_i, using *Gauss' law*:

$$\int_S d\mathbf{S} \cdot \mathbf{a} = \int_\Omega d\Omega \nabla \cdot \mathbf{a}, \tag{4}$$

we can obtain the following integral equation:

$$\int_{S_i} d\mathbf{S} \cdot \nabla A^z + \mu \int_{\Omega_i} d\Omega J_i^z = 0 \tag{5}$$

where S_i is the surface of h-filament a_i, including S_i^x and S_i^y (see Fig. 1), and only the contribution of J_i^z is counted because the integration is inside a_i. An effective resistance (called equivalent magnetic resistance, in short, EMR) is defined as

$$\hat{R}_{ij} \quad = \quad \mu \frac{(A_i^z|_{S_i} - A_j^z|_{S_i})}{\int_{S_i} d\mathbf{S} \cdot \nabla A^z|_{S_i}} \tag{6}$$

to model (i.e., replace) the mutual inductive coupling between a_i and a_j. Its value is determined by the *average* of A_i^z and A_j^z, both evaluated at surface S_i. Note that the definition of EMR in this paper is slightly different from [1] but more precise. For the simplicity of presentation, we define:

$$A_i = A_i^z|_{S_i}, \qquad A_j = A_j^z|_{S_i} \tag{7}$$

Note that the gradients of A_i^z and A_j^z at surface S_i are opposite to each other.

Moreover, there exists a ground EMR taking into account the self inductive effect. The ground EMR of a_i is given by:

$$\hat{R}_{i0} = \mu \frac{A_i^z|_{S_i}}{\int_{S_i} d\mathbf{S} \cdot \nabla A_i^z|_{S_i}} \tag{8}$$

Because the current is constant along z-direction, the volume integral of current density is reduced to lI_i, where I_i is the electrical current at a_i. Therefore (5) is simplified as:

$$\frac{A_i}{\hat{R}_{i0}} + \frac{(A_i - A_j)}{\hat{R}_{ij}} = -lI_i \tag{9}$$

A vector potential current source $\hat{I}_i$ can be defined as:

$$\hat{I}_i = lI_i \tag{10}$$

which is controlled by the electrical current I_i.

On the other hand, integrating (2) along z-direction at the h-filament surface S_i leads the following *inductive* electro-potential drop at a_i:

$$l\frac{\partial A_i}{\partial t} = -V_i \tag{11}$$

Consequently the voltage-controlled vector potential voltage source $\hat{V}_i$ is defined as:

$$\hat{V}_i = V_i/l \tag{12}$$

The VPEC model for two h-filaments includes following components [1] (see Fig. 2): (i) four nodes (IN_i, n_{i1}, n_{i2}, OUT_i) for each h-filament a_i; (ii) the pre-calculated resistance and capacitance between IN_i and n_{i1}; (iii) an electrical current source I_i between n_{i1} and n_{i2} controlling a vector potential current source $\hat{I}_i$ (see (10)); (iv) a vector potential voltage source $\hat{V}_i$ controlled by the vector potential current source $\hat{I}_i$; (v) an electrical voltage source V_i between n_{i2} and OUT_i controlled by the vector potential voltage source $\hat{V}_i$ (see (12)); (vi) effective resistances including ground $\hat{R}_{i0}$ (see (8)) and coupling $\hat{R}_{ij}$ (see (6)) resistances to account for the strength of inductances; and (vi) a unit inductance L_i to account for time derivative of the electrical current source I_i. It can be easily extended for the general three dimensional current distribution by adding two more VPEC circuits for x and y components. In essence, the VPEC model uses a resistance network plus unit self inductance and controlled voltage/current sources to replace the mutual inductance network. Although the VPEC model introduces more circuit elements, experiments in Section IV will show that it reduces simulation time for interconnects with non-trivial size.

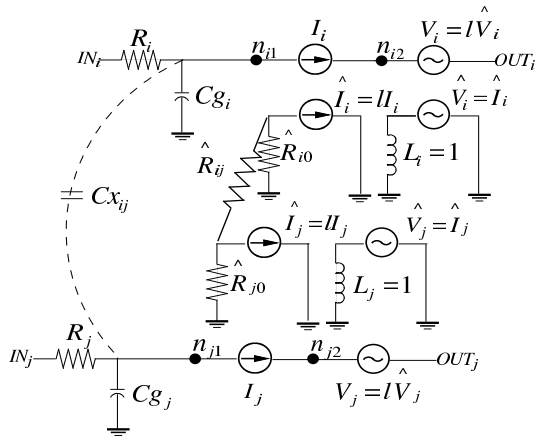

Fig. 2. The Vector Potential Equivalent Circuit model for two h-filaments.

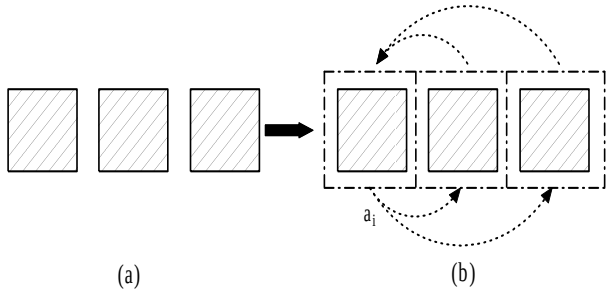

Fig. 3. Expansion of three filaments in (a) to hyper-filaments in (b). The magnetic flux starting from or ending at h-filament a_i is not local.

B. N-Body Problem

We first expand N filaments into h-filaments as illustrated in Fig. 3, and extend the VPEC model to the N-body problem by collocating all possible coupling pairs *independently*. Collocation is a common approach to construct the system equations [11], [12]. We collocate the vector potential drops from a_i to all the other h-filaments, and obtain the following equation at a_i:

$$\frac{A_i}{\hat{R}_{i0}} + \sum_{j \neq i} \frac{(A_i - A_j)}{\hat{R}_{ij}} = -l I_i \tag{13}$$

Note that the above summation is not local. However, in [1] the summation is local, and there are at most six coupling $\hat{R}_{ij}$ for each h-filament in three-dimension. The author obtained the localized model based on the analogy between (5) and the conduction current flow at a surface S: $\mathbf{I} = -\sigma \int_S d\mathbf{S} \cdot \nabla\phi$. The later is exactly the *Ohm's law*, which means the conduction current $\mathbf{I}$ at S is only related to the flux of the electrical field $\mathbf{E}$ ($-\nabla\phi$) at that surface. In the electro-quasi-static condition, $\mathbf{E}$ is along the same direction of $\mathbf{I}$ because no charge accumulated at the surface. However, for our N-body magneto-quasi-static problem, the flux in (5) is not along the conduction current direction z. Therefore it is related not only to the localized $\hat{R}_{ij}$ ($j = i \pm 1$), but also to all other $\hat{R}_{ij}$ ($j \neq i$). The experiments in Section 4.1 also show that compared to the full PEEC model, our VPEC model considering all neighbors is accurate, but the localized VPEC model from [1] is not accurate.

Furthermore there is no rigorous methodology to extract the equivalent magnetic resistance in [1]. We propose the following integration based method to obtain the EMRs: (i) calculate the distribution of $\mathbf{A}$ for the given input current distribution by (1) and (3); (ii) evaluate both the average vector potential difference between A_i^z and A_j^z and the surface integral by gradient of A^z at S_i according to (6) and (8). However, it is difficult to determine the appropriate size for each h-filament in numerical integration. In the next section, we propose a new inversion-based VPEC model without using integration.

III. VPEC Via PEEC Inversion

In this section we first present a closed-form relation between VPEC and the inversion of PEEC, then prove that the new circuit matrix $\hat{G}$ for VPEC model is passive and strictly diagonal dominant.

A. $\hat{G}$ Matrix

To obtain the circuit equation based on the *electrical* voltages and currents, we first take the time derivative at both sides of (13) and obtain

$$\frac{\partial A_i/\partial t}{\hat{R}_{i0}} + \sum_{j \neq i} \frac{(\partial A_i/\partial t - \partial A_j/\partial t)}{\hat{R}_{ij}} = -l \frac{\partial I_i}{\partial t} \tag{14}$$

and then use (11) to replace the time derivative of vector potential. Consequently we obtain:

$$\frac{V_i}{\hat{R}_{i0}} + \sum_{j \neq i} \frac{V_i - V_j}{\hat{R}_{ij}} = l^2 \frac{\partial I_i}{\partial t} \tag{15}$$

It leads to

$$(1/\hat{R}_{i0} + \sum_{j \neq i} 1/\hat{R}_{ij}) V_i + \sum_{j \neq i} (-1/\hat{R}_{ij}) V_j = l^2 \frac{\partial I_i}{\partial t} \tag{16}$$

We define the circuits matrix of VPEC model as:

$$\hat{G}_{ij} = -1/\hat{R}_{ij}, \qquad \hat{G}_{ii} = 1/\hat{R}_{i0} + \sum_{j \neq i} 1/\hat{R}_{ij} \tag{17}$$

The system equations can be written as:

$$\hat{G}_{ii} V_i + \sum_{j \neq i} \hat{G}_{ij} V_j = l^2 \frac{\partial I_i}{\partial t} \tag{18}$$

Compared to the following system equations based on K matrix [8] or the susceptance matrix S in [9]:

$$K_{ii} V_i + \sum_{j \neq i} K_{ij} V_j = \frac{\partial I_i}{\partial t} \tag{19}$$

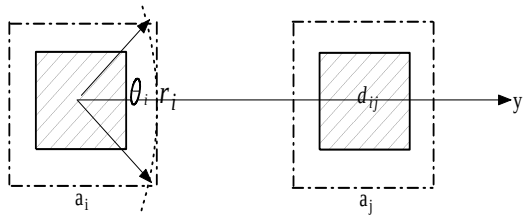

Fig. 4. Directly calculation $\hat{R}_{ij}$ of two long and thin h-filaments. They are not adjacent to each other in general.

where $K = L^{-1}$ and L is the partial inductance matrix, we find that $\hat{G}$ and K only differ by a factor of l^2, i.e.

$$l^2 K_{ij} = \hat{G}_{ij}, \qquad l^2 K_{ii} = \hat{G}_{ii} \tag{20}$$

Therefore starting with the L matrix under PEEC model, we can first obtain $\hat{G}$ matrix via (20), and then derive $\hat{R}$ matrix via (17). Because the major computation step is inversion of L matrix, we call this method as *inversion* based VPEC model. Furthermore, (20) can be viewed as how to derive the K-matrix based model in [7] from first principles.

B. Property

Lemma 1: Let I_i and I_j be currents for two h-filaments a_i and a_j, and l_i and l_j be lengths for a_i and a_j. If $I_i l_i = I_j l_j = Il$, then magnetic resistance $\hat{R}_{ij}$, $\hat{R}_{i0}$ and $\hat{R}_{j0}$ are all positive.

Proof: We assume that the centers of a_i and a_j are $(0, 0)$ and $(0, d_{ij})$ (see Fig. 4). The vector potentials of h-filaments a_i and a_j are given:

$$A_i^z = -\frac{\mu Il}{2\pi} ln(r/r_0), \qquad A_j^z = -\frac{\mu Il}{2\pi} ln(|r - d_{ij}|/r_0) \tag{21}$$

where $|r - d_{ij}| = \sqrt{(x - d_{ij})^2 + y^2}$, and r_0 is the dimension of filament. We define $\alpha_{ij} = \frac{|r_i - d_{ij}|}{r_i}$ describing the *distance difference* between a_i and a_j. Note that $\alpha_{ij} \geq 1$ as $d_{ij} \geq 2r_i$ according to the definition of h-filament.

The vector potential difference between A_i^z and A_j^z at surface S_i is:

$$(A_i^z - A_j^z)|_{S_i} = \frac{\mu Il}{2\pi} ln(\alpha_{ij}) \tag{22}$$

where r_i is the distance from the origin to the point on the surface S_i with coordinate (x_i, y_i).

Moreover, the magnetic flux at surface S_i is:

$$\int_{S_i} d\mathbf{S} \cdot \nabla (A_i^z + A_j^z)|_{S_i} = \frac{\mu Il}{2\pi} (l\theta_i)(1 - \alpha_{ij}^{-1}) \tag{23}$$

where $\theta_i (0 \leq \theta_i \leq 2\pi)$ is the angle for the surface integration at S_i with respect to the center of a_i. Therefore according to the definition of R_{ij} in (6), we have $\hat{R}_{ij} > 0$ for $j \neq i$. Similarly, we can prove $\hat{R}_{i0} > 0$ and $\hat{R}_{j0} > 0$. Both $\hat{R}_{i0}$ and $\hat{R}_{j0}$ are ground magnetic resistance for self inductance.

By refining h-filaments and segmenting the h-filament with larger current, we can always achieve $I_i l_i = I_j l_j$. For the application in PEEC inductance extraction, it means by segmenting the length of longer h-filaments according to shorter h-filaments, we can always obtain positive EMR elements for VPEC model. Therefore, we have the following Lemma 2:

Lemma 2: All magnetic resistances in VPEC model are positive.

We may prove the following theorem by Lemma 2:

Theorem 1: Circuit matrix $\hat{G}$ in VPEC model is passive [1] and strictly diagonal dominant.

Proof: According to (17) and Lemma 2, we have

$$\sum_{j \neq i} |\hat{G}_{ij}| = \sum_{j \neq i} 1/\hat{R}_{ij} \tag{24}$$

Because R_{i0} is also positive, we have

$$\sum_{j \neq i} |\hat{G}_{ij}| < 1/\hat{R}_{i0} + \sum_{j \neq i}^{N} 1/\hat{R}_{ij} = \hat{G}_{ii} \tag{25}$$

or

$$\hat{G}_{ii} > \sum_{j \neq i} |\hat{G}_{ij}| \tag{26}$$

I.e., the circuit matrix $\hat{G}$ is strictly diagonal dominant. Furthermore, it is also is passive according to the *Gersgorin Circle Theorem* [13].

Note that truncating off-diagonal entries from a strictly diagonal dominant matrix still leads a passive matrix. Intuitively, truncating small off-diagonal entries in $\hat{G}$ matrix (equivalent to truncating larger off-diagonal entries in $\hat{R}$ matrix) results in ignoring larger magnetic resistors in the equivalent magnetic resistances network. Based on Theorem 1, such truncation/sparsification leads to passive circuit models. Furthermore, larger magnetic resistors are less sensitive to and also contribute less to current change. Therefore, such sparsification may have a bounded accuracy loss, as shown by two sparsification procedures in Section 4.

IV. Experimental Results

We have implemented the inversion-based VPEC method in C code with the following steps: (i) generate partial inductance matrix L by FastHenry or formula from [14], [15]; (ii) inverse L by LU decomposition; (iii) calculate $\hat{G}$ and then $\hat{R}$; and (iv) generate VPEC model using $\hat{R}$. We assume each wire segment is modeled by one h-filament, and consider coupling between any pair of segments (including segments in a same line) unless specified otherwise.

The following simplified formula is employed for self-inductance of the long and thin h-filament [14]:

$$L_{ii} = \frac{\mu l_i}{2\pi} [ln(\frac{2l_i}{w_i + t_i}) + 0.5 + 0.2235\frac{w_i + t_i}{l_i}] \tag{27}$$

where l_i, w_i and t_i are the wire length, width and thickness

[1] Precisely, the matrix is positive definite, and the resulting circuit model is passive. In short, we say the matrix is passive in this paper.

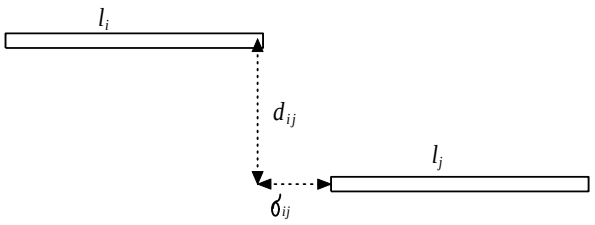

Fig. 5. Two parallel h-filaments with a geometric mean distance d_{ij} apart.

respectively. Furthermore, for the partial mutual inductance between two wires as shown in Fig. 5, the following simplified formula [14] is given:

$$L_{ij} = \frac{\mu}{4\pi}[\alpha sin^{-1}\frac{\alpha}{d_{ij}} - \beta sin^{-1}\frac{\beta}{d_{ij}} - \gamma sinh^{-1}\frac{\gamma}{d_{ij}} + \delta_{ij} sinh^{-1}\frac{\delta_{ij}}{d_{ij}} - \sqrt{\alpha^2 + d_{ij}^2} + \sqrt{\beta^2 + d_{ij}^2} + \sqrt{\gamma^2 + d_{ij}^2} - \sqrt{\delta_{ij}^2 + d_{ij}^2}] \quad (28)$$

where $\alpha = l_i + l_j + \delta_{ij}$, $\beta = l_i + \delta_{ij}$, and $\gamma = l_j + \delta_{ij}$. Note that δ_{ij} becomes negative when the two wires are overlapped. Furthermore, when the condition $l >> d$ holds, there are more efficient approximated formula can be employed as in [15].

We assume copper interconnect and low-k ($\epsilon = 2$) dielectric, and use FastCap to extract capacitance. Furthermore, interconnect driver and receiver are modeled by resistance $R_d = 100\Omega$ and loading capacitance $C_L = 2fF$. All circuit models are simulated by HSPICE. Below, we present results first for aligned parallel bus lines, and then for the on-chip spiral inductor. For all bus structures, a 1-V step voltage with 10ps rising time is applied to the first line, and all other lines are quiet. The outputs presented in Fig. 7, Fig. 10 and Fig. 11 are measured at the far ends of the last line.

A. Full VPEC Model

In this part we present the full VPEC model for various structures. We used both FastHenry and formula (27) and (28) to calculate the partial inductance for PEEC model. As shown in the experiment results, the difference of waveforms between the two methods is very small. Therefore we employ the PEEC calculated by formula to obtain the EMRs for VPEC model to efficiently simulate the complicated large systems.

1) Simple aligned parallel bus lines: We consider a five-bit bus, with one-segment per line. Each bus line is $1000\mu m$ long, $1\mu m$ wide and $1\mu m$ thick. The space between lines is $2\mu m$. The calculated L, K, $\hat{G}$ and $\hat{R}$ matrices are presented as follows:

$$L = \begin{bmatrix} 1.4816 & 1.1820 & 1.0437 & 0.9630 & 0.9059 \\ 1.1820 & 1.4816 & 1.1820 & 1.0437 & 0.9630 \\ 1.0437 & 1.1820 & 1.4816 & 1.1820 & 1.0437 \\ 0.9630 & 1.0437 & 1.1820 & 1.4816 & 1.1820 \\ 0.9059 & 0.9630 & 1.0437 & 1.1820 & 1.4816 \end{bmatrix} nH$$

$$K = \begin{bmatrix} 1.9696 & -1.2091 & -0.1904 & -0.1371 & -0.1749 \\ -1.2091 & 2.6964 & -1.1044 & -0.1231 & -0.1371 \\ -0.1904 & -1.1044 & 2.7052 & -1.1044 & -0.1904 \\ -0.1371 & -0.1231 & -1.1044 & 2.6964 & -1.2091 \\ -0.1749 & -0.1371 & -0.1904 & -1.2091 & 1.9696 \end{bmatrix} 10^9 H^{-1}$$

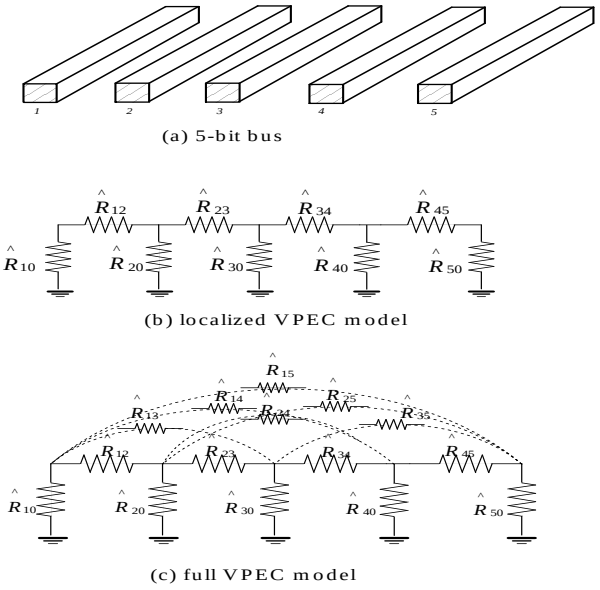

Fig. 6. The localized and full VPEC models for 5-bit bus lines. For simplicity of presentation, we only show the equivalent magnetic resistance, but not other circuit elements such as resistance, capacitance, and controlled voltage/current source (see Fig. 2).

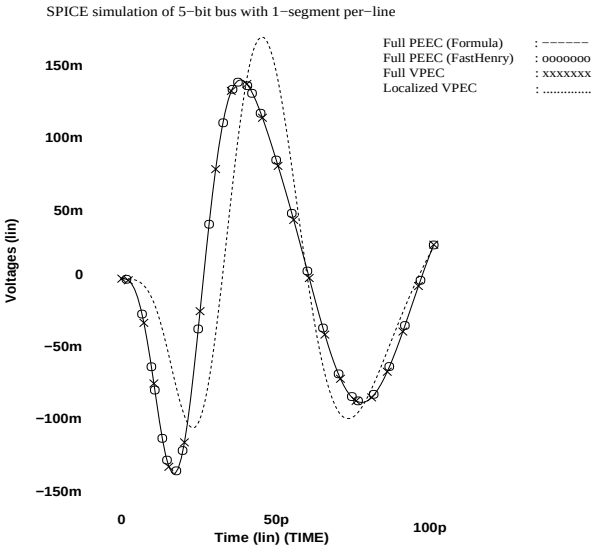

Fig. 7. Waveforms of 5-bit bus with one segment each line.

$$\hat{G} = \begin{bmatrix} 1.9696 & -1.2091 & -0.1904 & -0.1371 & -0.1749 \\ -1.2091 & 2.6964 & -1.1044 & -0.1231 & -0.1371 \\ -0.1904 & -1.1044 & 2.7052 & -1.1044 & -0.1904 \\ -0.1371 & -0.1231 & -1.1044 & 2.6964 & -1.2091 \\ -0.1749 & -0.1371 & -0.1904 & -1.2091 & 1.9696 \end{bmatrix} 10^3 H^{-1} m^2$$

$$\hat{R} = \begin{bmatrix} 3.8736 & 0.8270 & 5.2533 & 7.2964 & 5.7172 \\ 0.8270 & 8.1566 & 0.9054 & 8.1220 & 7.2963 \\ 5.2533 & 0.9054 & 8.6494 & 0.9054 & 5.2533 \\ 7.2964 & 8.1220 & 0.9054 & 8.1566 & 0.8270 \\ 5.7172 & 7.2964 & 5.2533 & 0.8270 & 3.8736 \end{bmatrix} 10^{-3} H m^{-2}$$

where $\hat{K}$ and $\hat{G}$ matrices differ only by a constant factor l^2. Similar to the "shielding" effect in the $\hat{K}$ matrix as pointed out in [8], the coupling $\hat{G}_{ij}$ ($\hat{R}_{ij}$) between non-adjacent lines is

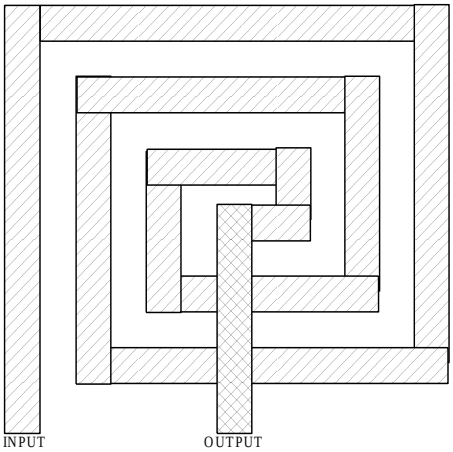

Fig. 8. The geometry of a 3-turn single layer on-chip spiral inductor.

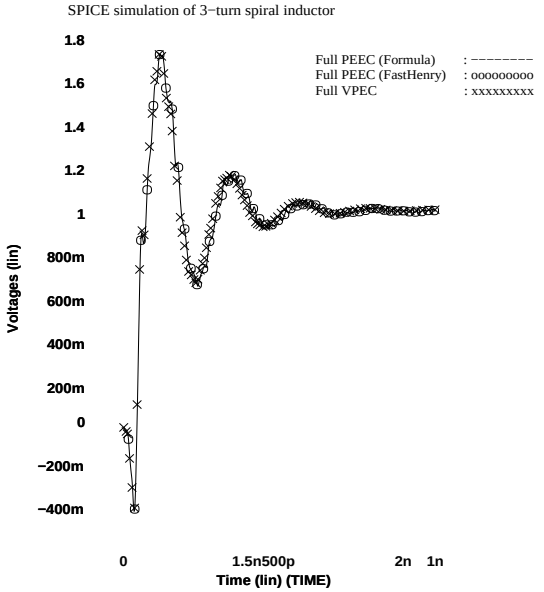

Fig. 9. Waveforms of the 3-turn single layer on-chip spiral inductor.

significantly smaller (larger) than that between adjacent lines. For a five-bit bus, we compare in Fig. 6 the circuit of the full VPEC model (with coupling $\hat{R}_{ij}$ between all lines) from this paper, and the circuit of the localized VPEC model (with coupling $\hat{R}_{ij}$ between adjacent lines) from [1]. Clearly as shown in Fig. 7, our full VPEC model and the full PEEC model by FastHenry and formula (27) and (28) obtain identical waveforms, but the localized VPEC model introduces non-negligible error and is not accurate compared to the full PEEC model.

2) Simulation of non-bus structures: The VPEC model can be employed to simulate monolithic spiral inductors as well as regular aligned parallel bus lines. The on-chip inductors are widely used in CMOS RF circuits, such as LNA and VCO [16], [17]. We have applied VPEC model for the single-layer spiral inductor in Fig. 8. The outer wire length is $1000um$, the wire width is $20um$, the thickness is $10um$, and the spacing between the centers of two adjacent wires is $100um$. We assume that wires are segmented as shown in Fig. 8 for both VPEC and PEEC models, apply 1-V voltage at the input port, and measure the response at the output port.

Furthermore, because the h-filaments now have different lengths, the system equation (16) is modified to:

$$(\frac{1}{l_i^2\hat{R}_{i0}} + \sum_{j\neq i}\frac{1}{l_i^2\hat{R}_{ij}})V_i + \sum_{j\neq i}(-\frac{1}{l_i l_j \hat{R}_{ij}})V_j = \frac{\partial I_i}{\partial t} \qquad (29)$$

It directly leads to the following general mapping relation with the K matrix

$$\hat{R}_{ij} = -\frac{1}{l_i l_j K_{ij}}, \qquad \hat{R}_{i0} = \frac{1}{l_i^2 K_{ii} + \sum_{j\neq i} l_i l_j K_{ij}} \qquad (30)$$

The simulation result is presented in Fig. 9. The PEEC models by FastHenry and formula (27) and (28) generate identical waveforms, and the VPEC model can reproduce the result of the PEEC model for the non-bus line structures as well. Therefore the VPEC model is suitable to be applied for the general layout. Note that when the number of the wires of the simulated system is small, there is no eminent simulation speedup observed. However, in the following experiments with larger wire segments, we found the simulation effort in the full VPEC model is much less than the full PEEC model, even without the sparsification.

B. Sparsification for VPEC Model

We study two sparsification procedures, numerical sparsification and 2D geometry based sparsification for various bus line structures in this part.

1) Numerical Sparsification: As explained in Section 3.2, $\hat{G}$ matrix is passive and diagonal dominant. Therefore, small-valued off-diagonal elements can be truncated without loss of passivity. For example, setting the truncating threshold as 0.09 where any off-diagonal element smaller than 0.09 of its correspondent diagonal element is truncated results in the following truncated $\hat{G}$ (denoted as *truncated* VPEC in Table I) for the above five-bit bus:

$$[\mathrm{G}] = \begin{bmatrix} 1.9696 & -1.2091 & -0.1904 & 0 & 0 \\ -1.2091 & 2.6964 & -1.1044 & 0 & 0 \\ 0 & -1.1044 & 2.7052 & -1.1044 & 0 \\ 0 & 0 & -1.1044 & 2.6964 & -1.2091 \\ 0 & 0 & -0.1904 & -1.2091 & 1.9696 \end{bmatrix} 10^3 H^{-1} m^2$$

Applying (17) to truncated $\hat{G}$ leads to the following truncated $\hat{R}$:

$$\left[\hat{R}\right] = \begin{bmatrix} 3.8736 & 0.8270 & 5.2533 & \infty & \infty \\ 0.8270 & 8.1566 & 0.9054 & \infty & \infty \\ \infty & 0.9054 & 8.6494 & 0.9054 & \infty \\ \infty & \infty & 0.9054 & 8.1566 & 0.8270 \\ \infty & \infty & 5.2533 & 0.8270 & 3.8736 \end{bmatrix} 10^{-3} H m^{-2}$$

Fig. 10 plots the simulation results under our numerical sparsification for a 128-bit bus with one segment per line, where the sparse factor is the ratio between the numbers of circuit elements in the truncated and full VPEC models. The waveform difference is small in terms of the noise peak for sparse factors up to 30.5%. Table I summarizes the truncation setting and simulation result, where the values in parentheses of column 1 are truncating thresholds, and the runtime includes both SPICE simulation and matrix inversion in case of VPEC models. The average voltage differences, and associated standard deviations are calculated for all time steps in SPICE simulation. One can see from the table that up to 30X

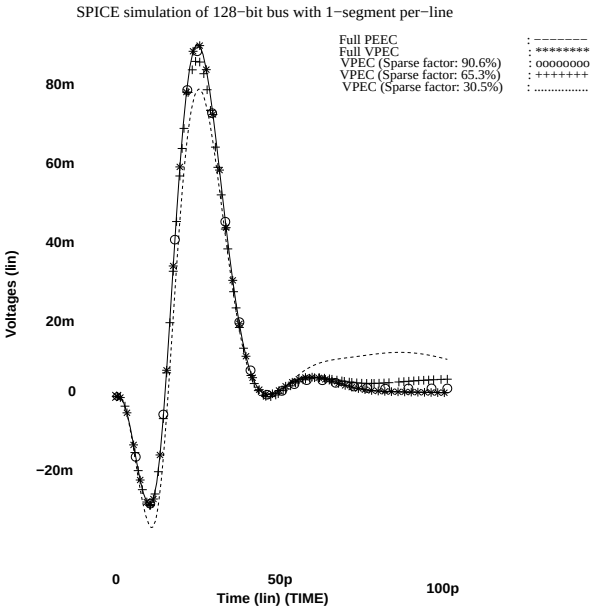

Fig. 10. Waveforms in numerical sparsification of VPEC model for 128-bit bus with one segment each line.

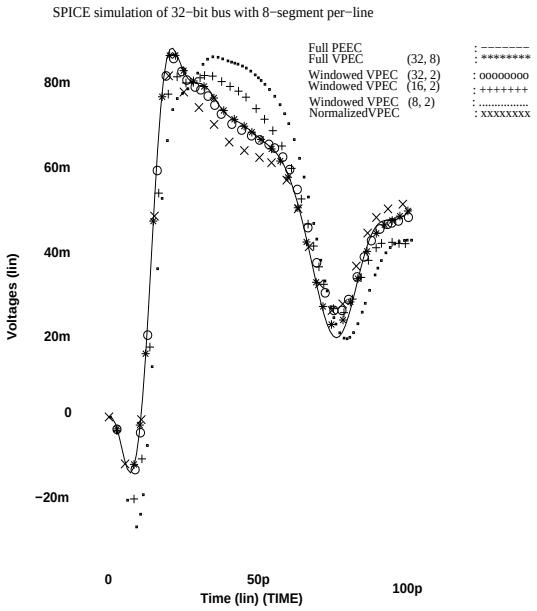

Fig. 11. Waveforms in geometry based sparsification of VPEC model for 32-bit bus with 8 segments each line.

speedup is achieved when the average waveform differences is up to 0.377mV, less than 1% of the noise peak. A much bigger speedup factor can be expected as a much higher waveform difference can be tolerated in practice. Compared to the full PEEC model, the full VPEC simulation is 7X faster, due to the fact that the VPEC model has a bit more resistances and coupled current/voltage sources but much fewer inductances. The negligible difference between the full VPEC and PEEC simulations is due to the numerical matrix inversion.

2) Geometry Based Sparsification: We study the geometry based sparsification for segmented buses by defining a truncating window (N_W, N_L), where N_W and N_L are the numbers of coupled segments in directions of wire width and length, respectively. We further define the couplings along wire length as the *forward* coupling same as in [18], and along wire width as the *aligned* coupling. For each wire segment, the circuit model only contains $\hat{R}_{ij}$ within the truncating window of the segment, and is called *windowed* VPEC model in Table II. We consider a 32-bit bus with eight segments per line and four different windows: (32, 8), (32, 2), (16, 2) and (8, 2). Furthermore, we apply the normalized model [19] to VPEC (called *normalized* VPEC model in Table II) for the bus lines with n segments per line. If the EMR between any two bus lines without segmentation is $\hat{R}_{ij}$, the EMR for each pair of aligned segments is $\hat{R}_{ij} \cdot n^2$, and is zero for non-aligned segments.

We plot simulations under different models in Fig. 11, and summarize the experiment setting and result in Table II. There is a smooth trade-off between runtime and accuracy for different window sizes. We first compare results of different truncating windows. The window (8, 2) achieves the highest speedup of 30X and the largest difference of about 0.2mV on average, less than 2% of the noise peak, and the window (32, 2) has the highest accuracy with 0.06mV on average but a reduced speedup of 10X. Furthermore, we compare the normalized model to the window (16, 2) with a similar complexity. The windowing technique is faster but has a larger standard deviation. The normalized model implicitly considers the forward coupling between all non-aligned segments, and the window (16, 2) considers forward coupling between adjacent segments only. The small difference between the two models implies that the forward couplings between non-adjacent segments may be negligible, which is also indicated by the small difference between windows (32, 8) and (32, 2). However an N_W much larger than N_L (as shown in Table II) is needed to archive a high accuracy. This implies that the aligned coupling is stronger than the forward coupling.

C. Runtime Scaling

We compare runtimes to analyze parallel bus structures using the full PEEC model, full VPEC model, and windowed VPEC model, respectively. The runtime for the full or windowed VPEC model includes both SPICE simulation and matrix inversion. We first consider one segment per line, and plot runtimes in Fig. 12 (a). The full PEEC and VPEC models can only handle the bus with up to 256 bit because SPICE can not further allocate enough memory. But the windowed VPEC model can handle the bus with up to 1024 bit. For the 256-bit bus, the full and windowed VPEC model is 47X (185.39s vs. 8726.85s) and over 1000X faster than the full PEEC model, respectively. Our experiment assumed a truncating window of (8, 1) because $N_W = 8$ for a truncating window (N_W, N_L) has a reasonably good error bound as shown in Table II. It is easy to see that the windowed VPEC has a slow runtime scaling with respect to the increase of the bus width.

We further conducted the experiment considering the distributed interconnect model with eight segments each line, and plot the runtimes in Fig. 12 (b). Based on Table II, we assume a (8, 2) truncating window for the windowed VPEC model.

The full PEEC and VPEC models can only handle 32-bit bus, but the window VPEC is able to handle the 128-bit bus at a much reduced runtime. The scaling of the runtime using the windowed VPEC model is super-linear, but its increase is much slower than that for the full PEEC and VPEC models.

In both experiments, the full VPEC model achieves identical waveform and the windowed VPEC model has a very small waveform difference when compared to the full PEEC model. The observation is similar to Fig. 11.

V. Conclusions and Discussions

The primary contribution of this paper is to derive from first principles both integration and inversion based VPEC models for multiple inductive interconnects. Using equivalent resistance network and controlled voltage and current sources to replace inductance network, the full VPEC model is as accurate as the full PEEC model but takes less simulation time. We have observed a speedup of 47X for simulating 256 wire segments in a bus structure. Further, the resulting circuit element matrix $\hat{G}$ in the VPEC model is passive and strictly diagonal dominant. This leads to easy sparsification methods with guaranteed passivity. We have presented both numerical and geometry based sparsification methods. When compared to the full PEEC and VPEC models, the sparsified VPEC models achieve orders of magnitude speedup in circuit simulation and produce waveforms with very small error.

Because matrix $\hat{G}$ and matrix K from [7] differ only by constant factors, our study can be used to justify from first principles the K matrix based sparsification methods. One can use geometry integration to calculate the matrices $\hat{R}$ and $\hat{G}$. Therefore, the matrix K can be calculated directly by geometry integration without inverting the partial inductance matrix. Note that SPICE is able to directly simulate VPEC model but not K-matrix based model.

In essence, our VPEC sparsification can be viewed as full VPEC generation followed by sparsification. Although we have shown that the locality of VPEC illustrated in [1] does not hold in general, the method in [1] can be viewed as a special case with the smallest truncating window size for the direct generation of a sparsified VPEC model. The direct method with bounded accuracy loss is attractive if it is more efficient compared to the inversion of the full inductance matrix as such inversion is needed by the sparsification methods in this paper. Efficient methods for direct sparsification with bounded accuracy loss are planned as our future work on VPEC model.

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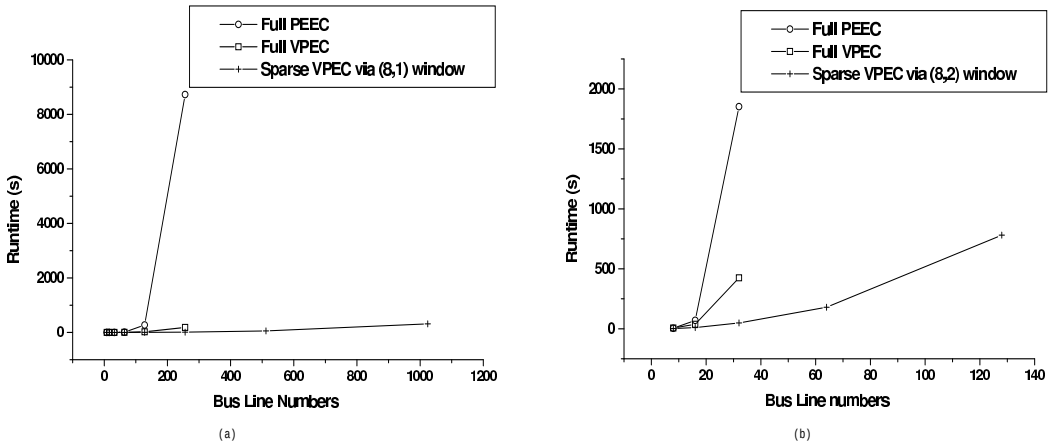

Fig. 12. Runtime to simulate multiple bus lines using the full PEEC, full VPEC, and sparsified VPEC models: (a) multiple bus lines with one segment each line; (b) multiple bus lines with eight segments each line.

Models and Truncating Thresholds	No. of Elements	Run-Time and Speedup	Avg. Volt. Difference	Standard Deviation
Full PEEC	8256	281.02s (1X)	0V	0V
Full VPEC(0.0)	8256	36.40s (7X)	-1.64e-6	3.41e-4V
Truncated VPEC(5e-5)	7482	30.89s (9X)	4.64e-6V	4.97e-4V
Truncated VPEC(1e-4)	5392	19.55s (14X)	1.29e-5V	1.37e-3V
Truncated VPEC(5e-4)	2517	8.35s (28X)	3.77e-4V	5.20e-3V

TABLE I

RESULTS OF NUMERICAL SPARSIFICATION

Models and Window Sizings	No. of Elements	Run-Time and Speedup	Avg. Volt. Difference	Standard Deviation
Full PEEC	32896	2535.48s (1X)	0V	0V
Full VPEC(32,8)	32896	772.89s (3X)	1.00e-5V	6.26e-4V
Windowed VPEC(32,2)	11392	311.22s (8X)	5.97e-5V	1.84e-3V
Windowed VPEC(16,2)	3488	152.57s (16X)	-1.23e-4V	4.56e-3V
Windowed VPEC(8,2)	2240	85.14s (32X)	-2.17e-4V	8.91e-3V
Normalized VPEC	4224	255.36s (10X)	-6.05e-4V	2.96e-3V

TABLE II

RESULTS OF GEOMETRY BASED SPARSIFICATION