ASPDAC Tutorial: Power, Timing & Signal Integrity in SoC designs Section II

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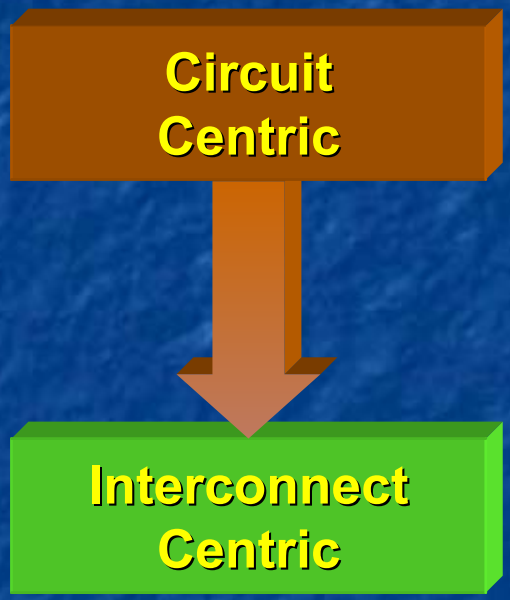
Section II: Modeling, noise, timing

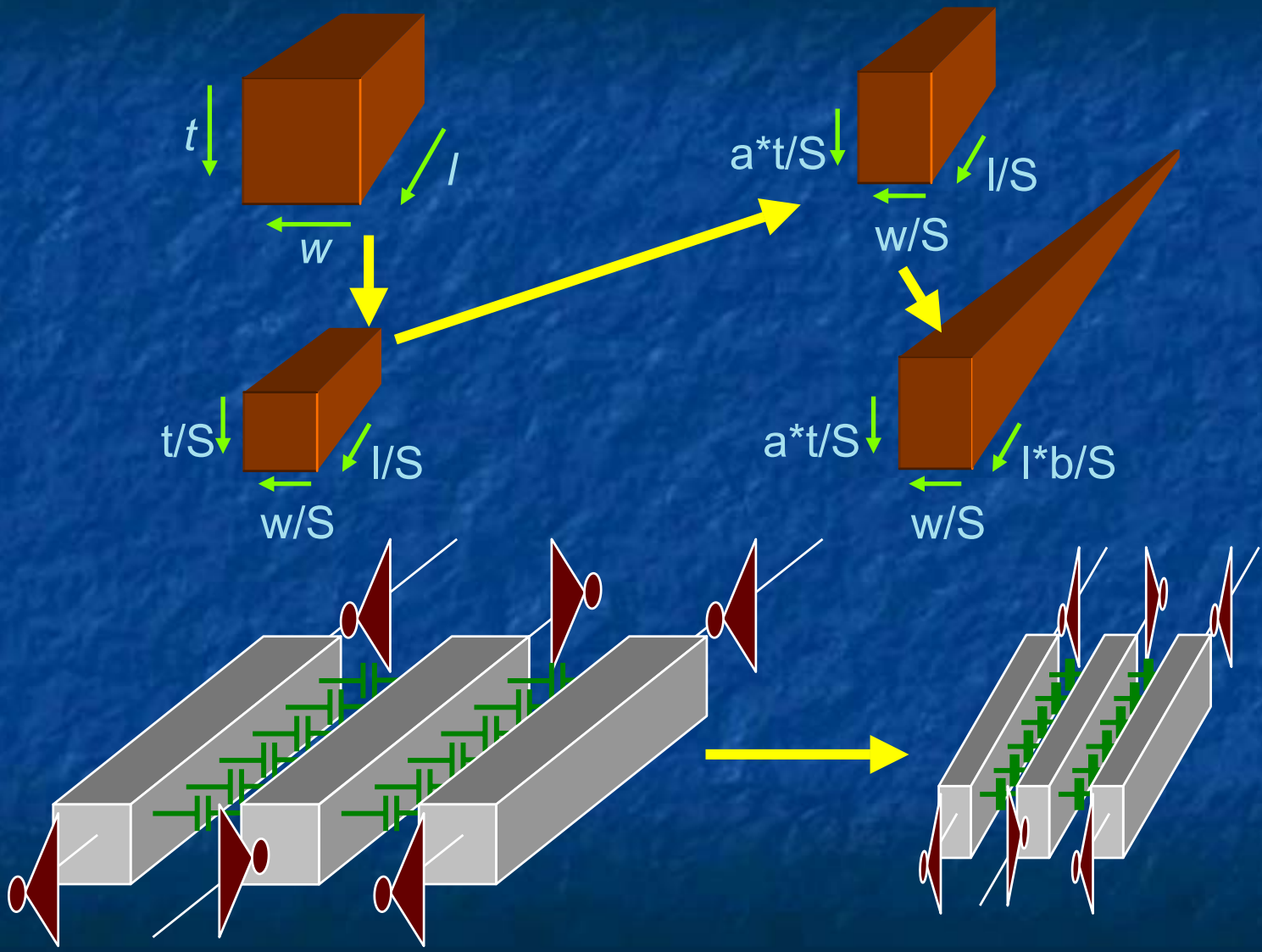
- The goals of this section is to:
  - Introduce scaling and the impact on models
  - Discuss the "interconnect problem"
    - Timing, noise, noise on timing
  - Give types of models used
    - Delay models
    - Moment models
    - PEEC models
  - Show inductance effects on-chip
    - Impact on modeling
  - Discuss model reduction

Design Paradigm Shift

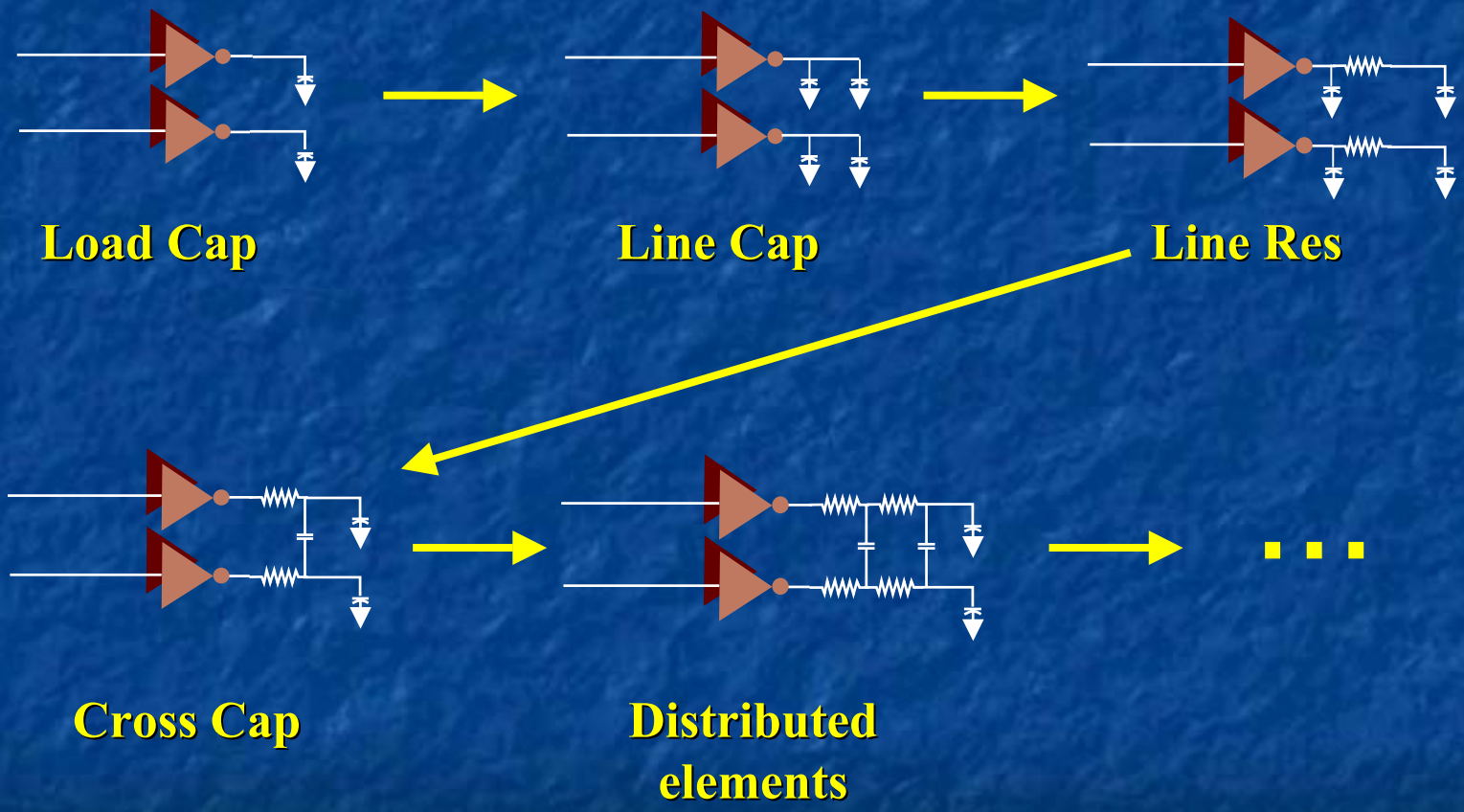


- **Circuit-centric**
  - Circuit poses major constraints
  - Slower convergence when interconnects weigh more
- **Interconnect-centric**
  - Interconnect dominated
  - Circuit built around interconnects

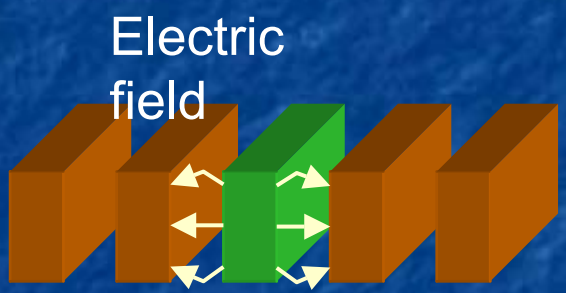
Interconnect scaling

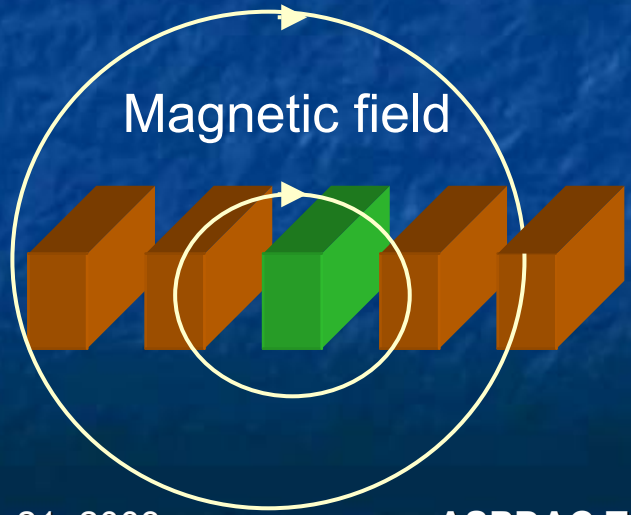


Models also scale…



Trend of interconnect effects

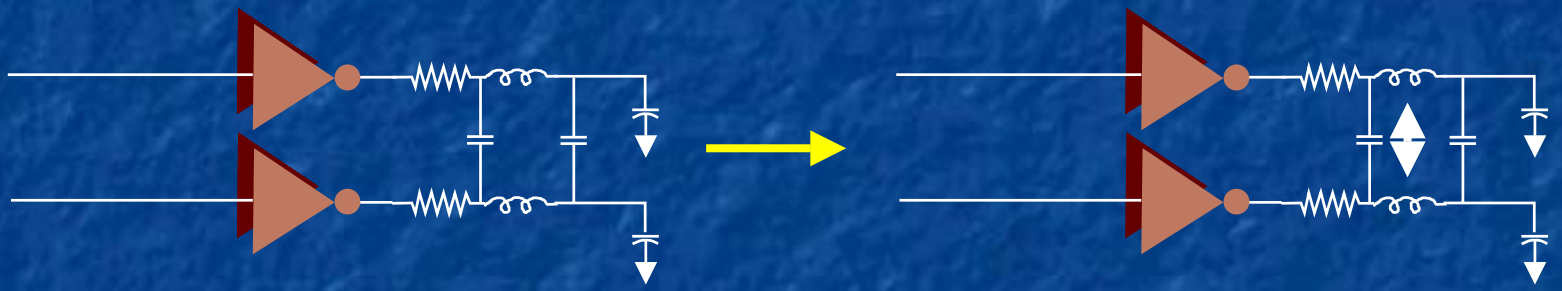




- Resistance
  - Very local
  - Only varies at high F
- Capacitance:
  - Electric field coupling
  - Very small and well defined interaction zone
- Inductance:
  - Magnetic field coupling
  - global interaction zone

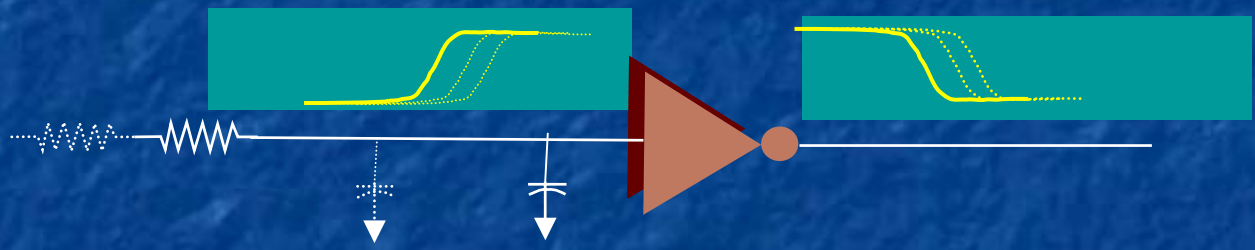
Opposed to digital design!

With more scaling?...



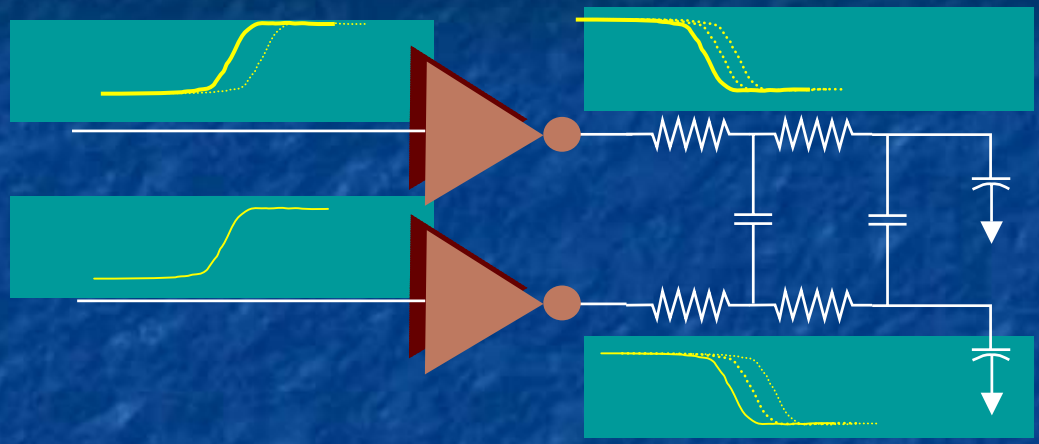
Line Inductance **Mutual Inductance**

Timing Variation Due to Parasitics



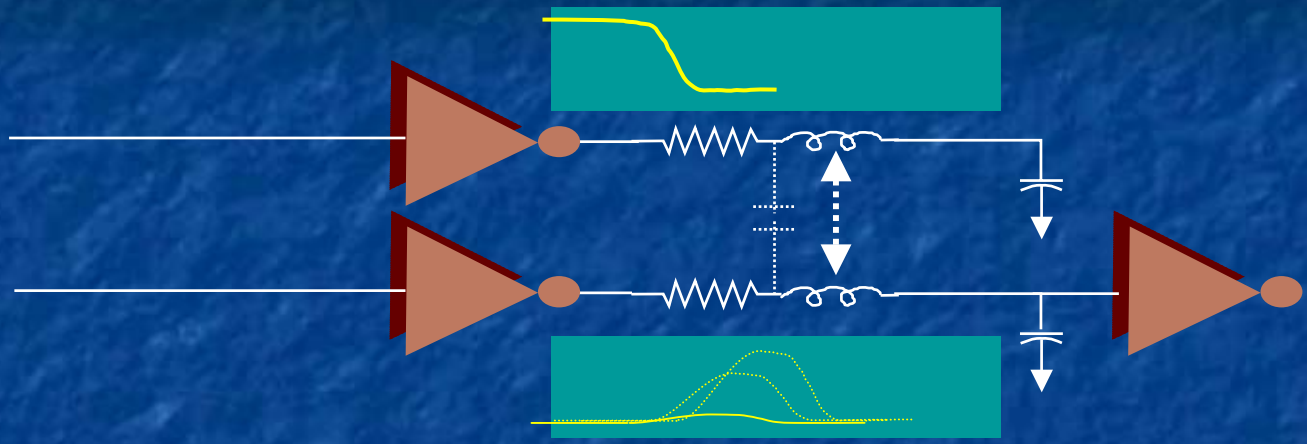
- Interconnect parasitic variation impacts delay
- Easiest of the interconnect effects to solve and include
  - Delay formulas
  - Simplified model synthesis
  - Model reduction

Timing Variation Due to Coupling



- Coupling variation increases delay variation (noise-on-timing)
  - Dynamic environmental variation
    - Interconnect coupling is spatially deterministic (fixed)
    - Patterns are temporally non-deterministic (usually)
  - Compare to process variation which is static (both spatially deterministic and non-deterministic)
- Analysis is more difficult because models extend the neighborhood of interaction (timing is path-based)

Noise Due to Coupling



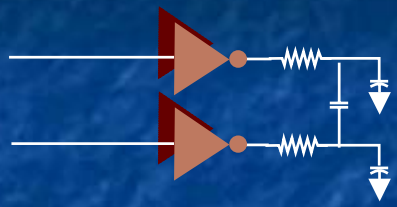
- Coupling increases noise
  - Change signals away from being digital
  - Coupling can be capacitive (important and probable) or inductive (can be more important, less probable)
  - Somewhat simpler analysis than noise-on-timing
    - victims assumed to be static
    - noise can be approximately linearly additive

Chip-level design

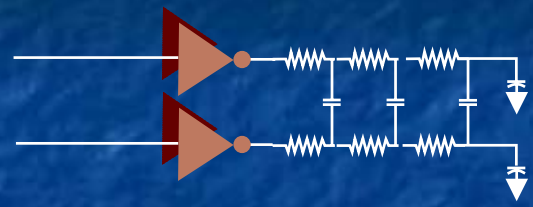
- Increasing effects on delay, timing and noise-on-timing from electric fields
- Design has become increasingly interconnect-heavy
  - R(L)C Interconnects form the majority of models and flood our design databases with 1,000,000's of elements!

- Need to understand the modeling and when it is needed and when it is not

Lumped and Distributed RC Models



Lumped RC



Distributed RC

- Interconnect RC delay modeled by lumped RC model or distributed RC model
- Lumped: all C is combined into one capacitor and all R is combined into one resistor regardless of length of line or value of load
- Distributed: series of R and C lumped components – more elements, but more accurate
  - typically 3-5 can give a high degree of accuracy

Elmore Delay Modeling

- Elmore characterized interconnect lines as a lumped T section with resistor and capacitor elements.
- Elmore delay equation (for one line C and R):

$$T_d = \frac{1}{2} RCl^2 + RC_L l + R_D Cl + R_D C_L$$

  - R is the resistance per unit length
  - C is the capacitance per unit length
  - l is the interconnect length
  - R_D is the driver resistance
  - C_L is the load capacitance

Sakurai Delay Modeling

- Sakurai studied distributed RC lines and modified Elmore delay equation for accuracy
- Sakurai delay equation:

$$T_d = 0.377RCl^2 + 0.693(RC_L l + R_D Cl + R_D C_L) \quad *$$

- Low 100's MHz: these models predict circuit behavior
- In gigahertz regime: these models may be inadequate

*error in the handout – see T. Sakurai, et al., "Approximation of wiring delay in MOSFET LSI", IEEE Journal of Solid-state circuits, Vol. SC-18, No. 4, Aug. 1983.

RC Parasitics at Medium Frequencies

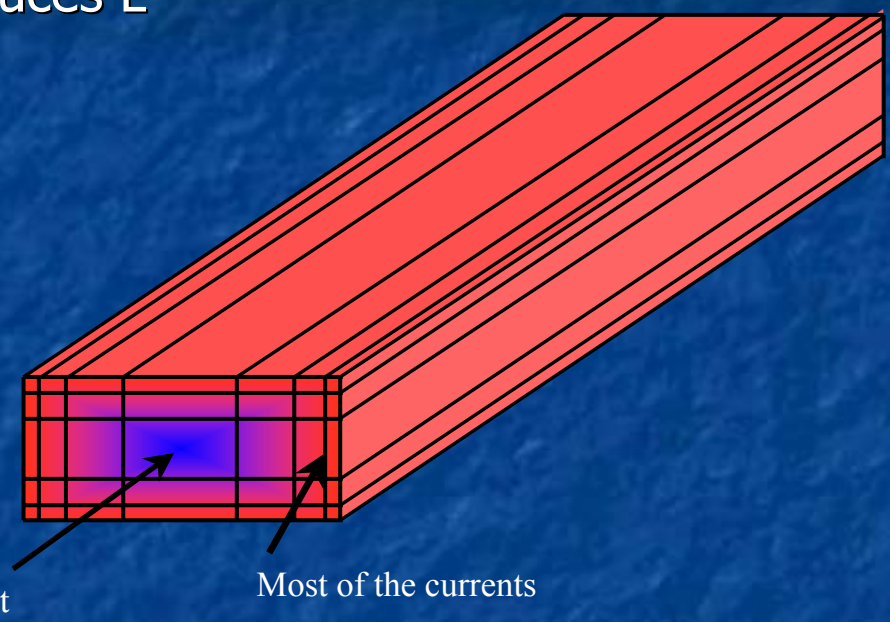
- Low frequencies, skin effect on resistance negligible - R considered frequency independent.
- If R >> ωL, L neglected and RC model adequate
  - R is interconnect resistance
  - L is interconnect inductance
  - ω is operating frequency
- Smaller features and higher frequencies - R and C affected by technology scaling in relation to line width.

Skin-effect & Skin depth

- Skin-effect increases R and reduces L

$$\delta = \frac{1}{\sqrt{\pi \cdot f \cdot \mu \cdot \sigma}}$$

  - σ is conductivity
  - μ is permeability
  - f is sig. frequency



- Skin-depth is the point at which current density inside a conductor decays to 1/e the surface value
- Skin effect typically occurs when the skin-depth approaches ½ the width or thickness of the conductor
- Not much skin effect on-chip unless thickness is large, modeling usually not done

When to Use RLC Modeling

- Check 1: Line cap-dominated $C_L < \frac{1}{8} Cl$
  - *CL* = load capacitance, *C* = per-unit-length coupling capacitance, *l* = length of the line
- Check 2: Line under-damped $\frac{Rl}{2} \leq \sqrt{\frac{L}{C}}$
  - *l* is length of interconnect
  - *R* is per-unit-length-resistance
  - *L* is per-unit-length self-inductance
  - *C* is per-unit-length coupling capacitance
- Check 3: Z magnitude $2\pi f_s Ll > \frac{Rl + Z_{DRV}}{2}$
  - Z_{DRV} is driver impedance
  - f_s is **significant** signal frequency based upon rise time
  - Is inductive impedance comparable to line resistance and driver impedance?

Multi-conductor RLC Modeling

- In general interconnects & power delivery systems with N number of conductors can be modeled using a system of NxN RLC matrices
- For each interconnect line, a corresponding row and column exists in the [R] matrix, [L] matrix, and [C] matrix.
  - G matrix is generally neglected in $Z=(R+sL)/(G+sC)$
- The off-diagonal terms represent the interaction or coupling between two interconnects
- A complete set of matrices (RLC) can be extracted for any given frequency by 2D EM modeling

Why Multi-conductor RLC Modeling?

- Multi-conductor modeling is expensive to use but always accurate
- For some n wire structures, the return path assumption can be applied to reduce to n-1
- Typically used for board level but also for detailed understanding (not full-chip flows)
- Common applications:
  - To analyze detailed noise coupling between groups of signals that switch simultaneously (i.e., a bus)
  - To analyze V_{CC} & V_{SS} return effects

Why think about inductance?

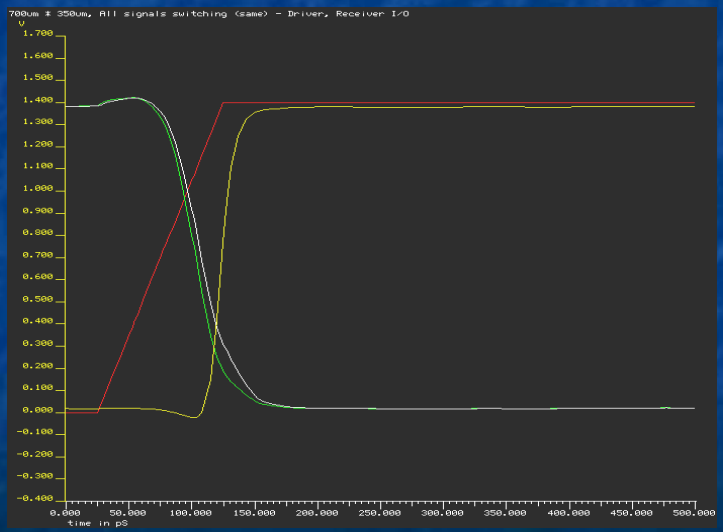
- NEW TECHNOLOGY
  - Fast switching times
  - Every pico-second is important in fast designs pushing limits
- SILICON observations
  - Divergence between silicon measurements and RC models
  - HP documented uP silicon failure due to inductance
- SIMULATION observations
  - Noise difference between RC and RLC models
  - Timing difference between RC and RCL models
  - Skew difference between RC and RLC models
- SPEED OF LIGHT limitations
  - We are approaching these regimes on chip so inductive effects must appear

Primary effects of on-die inductance

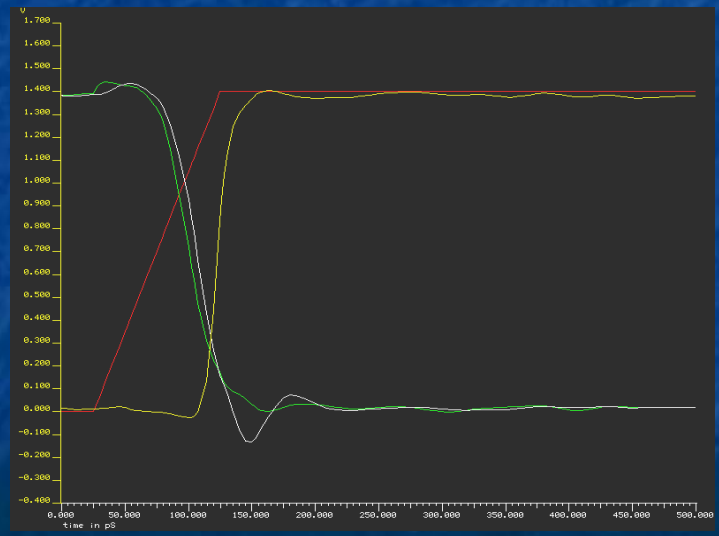
- Power grid noise (up to resonance):
  - di/dt rapidly grows per new technology
- Clock skew
  - inductance especially important due to wide wires and fast edges
- Delay (slope at receiver end):
  - under- or overestimated if inductive coupling is ignored
  - underestimated if return path resistance is neglected
  - impacts repeaters insertion methodology
- Propagation delay (flight time):
  - ignored (estimated as 0) if interconnect inductance is ignored;
  - (LC) per unit length $\geq \mu\varepsilon = 1/v^2$, v = speed of light in matter
  - SiO_2: $\varepsilon/\varepsilon_0 = 3.5$, v = 160 μm/psec, ~ 10,000 μm / 60 psec
- Overshoot-ringing:
  - severe reliability hazard
- Mutual noise:
  - mutual inductance can, on low probability, be higher than cross-cap noise

Inductive Effects

- Impact on signal nets
  - Oscillations, under/over shoot
  - inductive cross-talk
  - Increase in signal delay
  - reduction in transition time

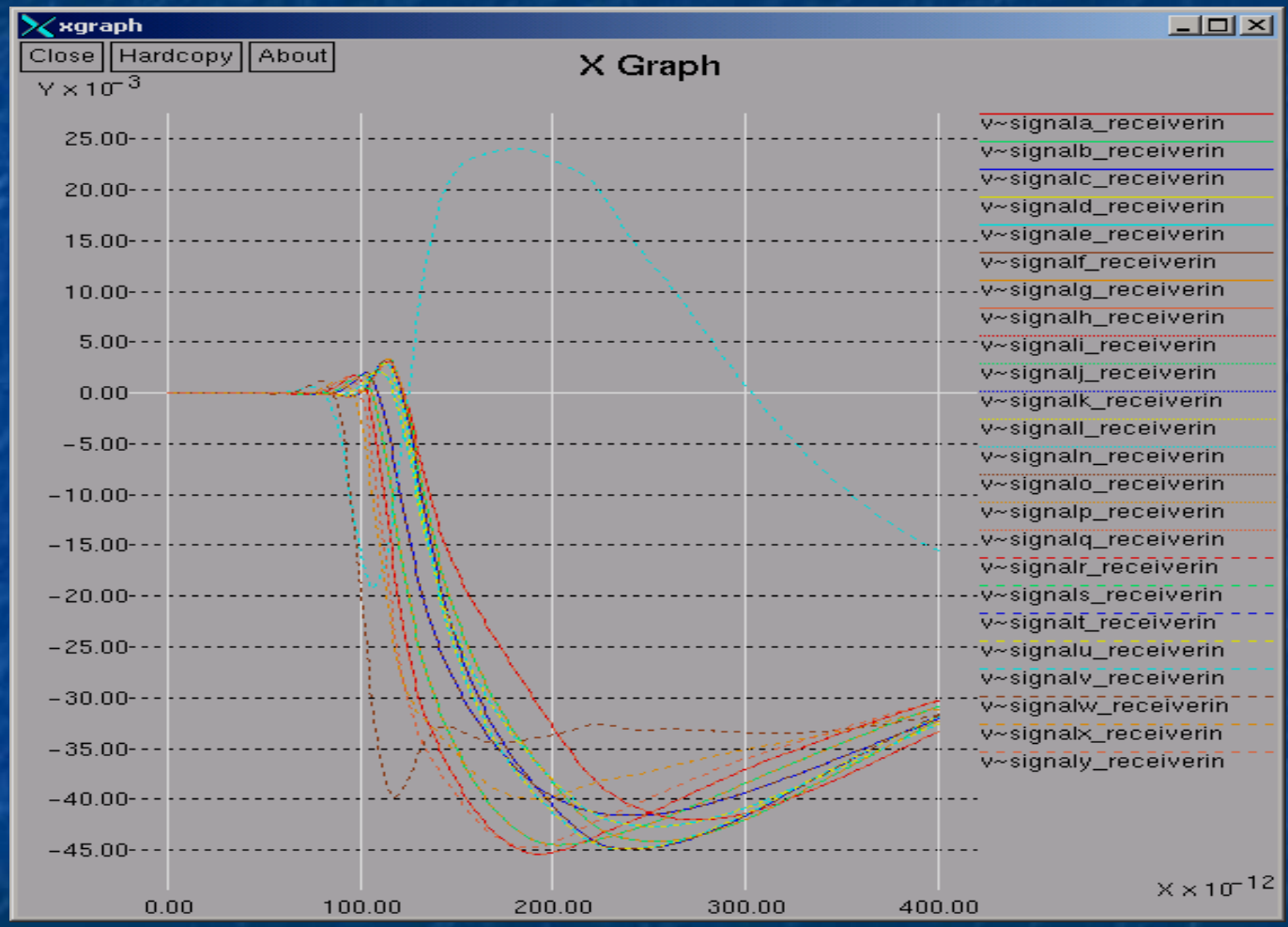


RC - MODEL



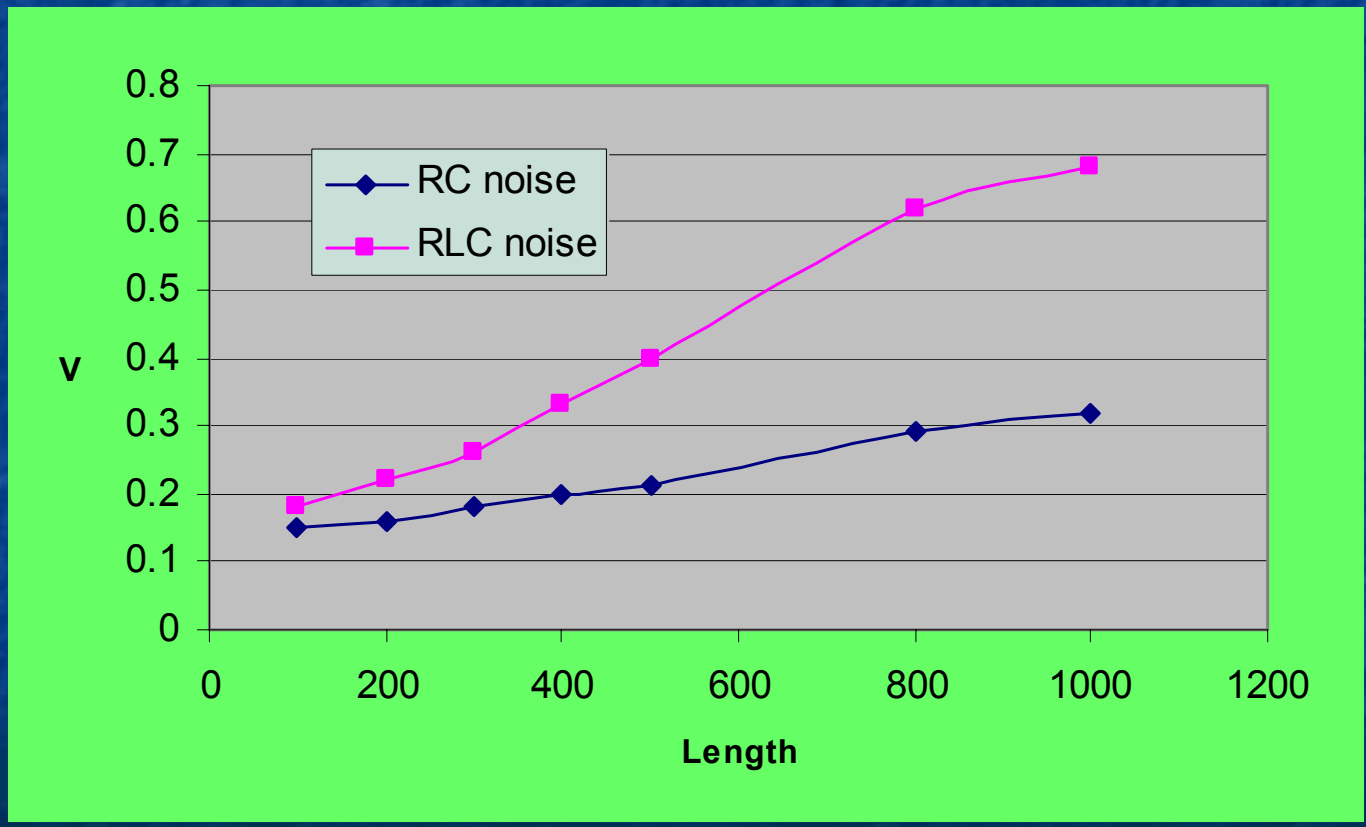
RLC - MODEL

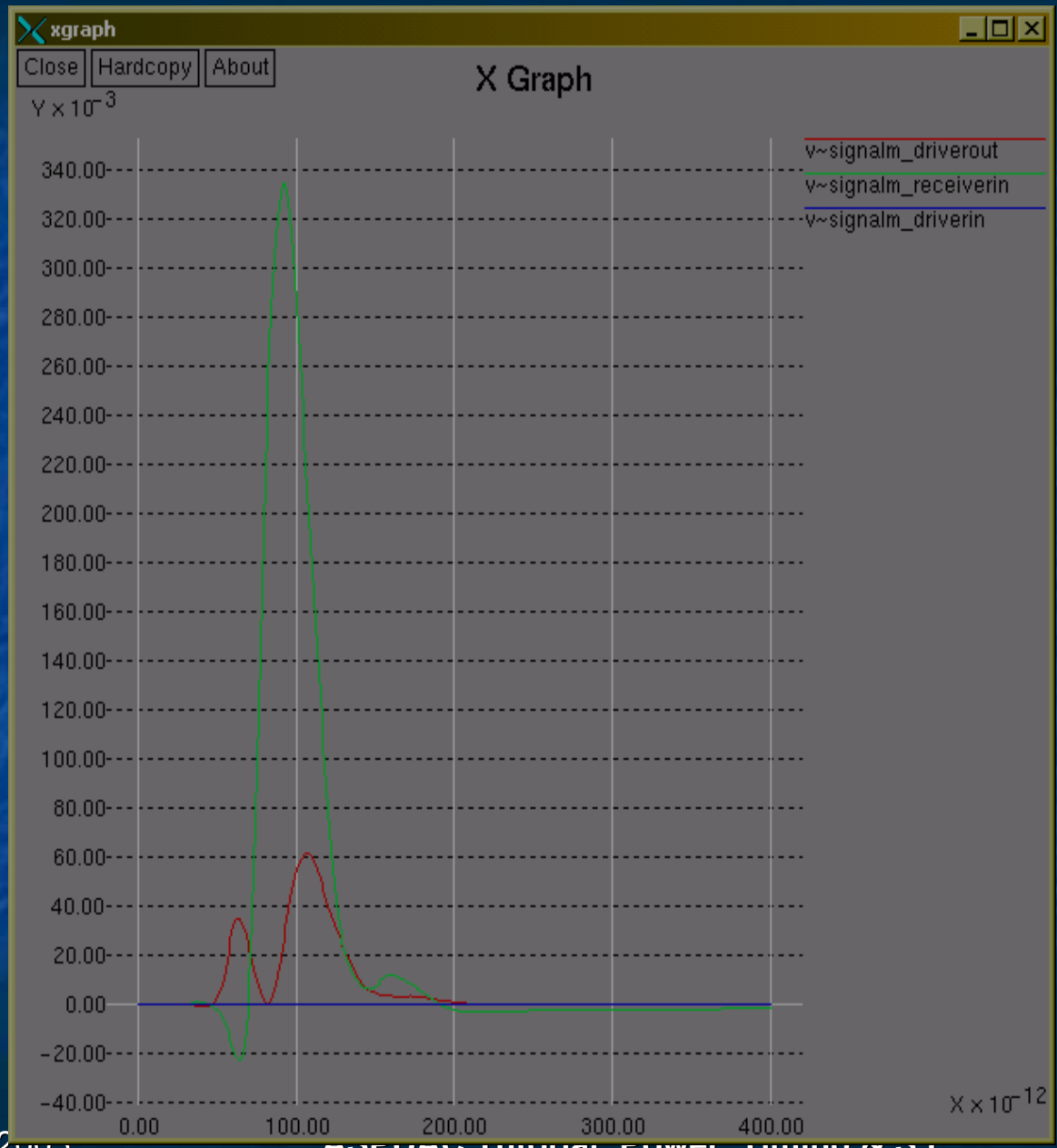
Noise input to the receivers for WC



RC/RLC noise difference

Rise time of the order of 30ps yielding noise





Noise

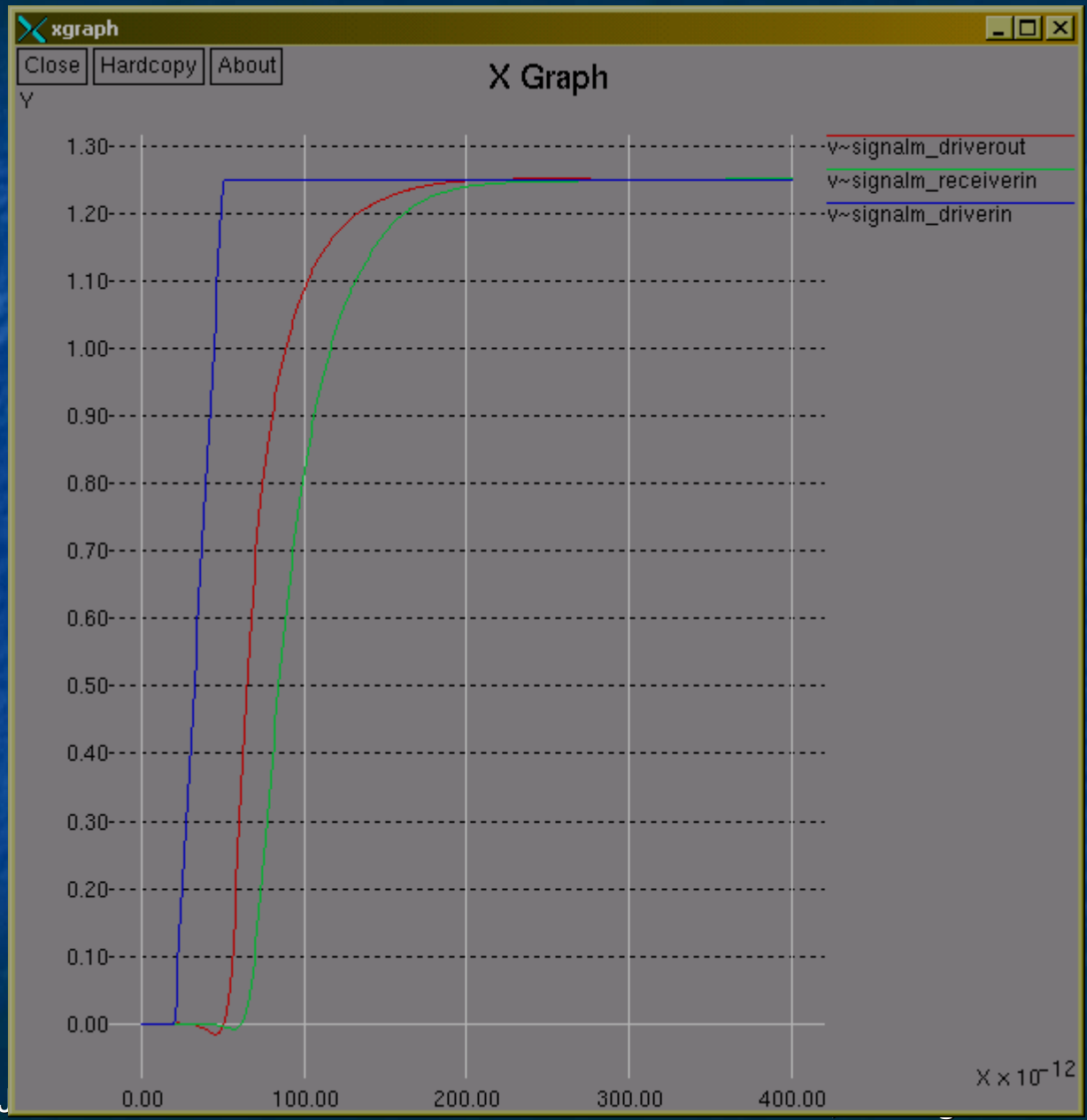
1000u line

25 signals

Victim at 0V

WC RLC noise (+)

Timing



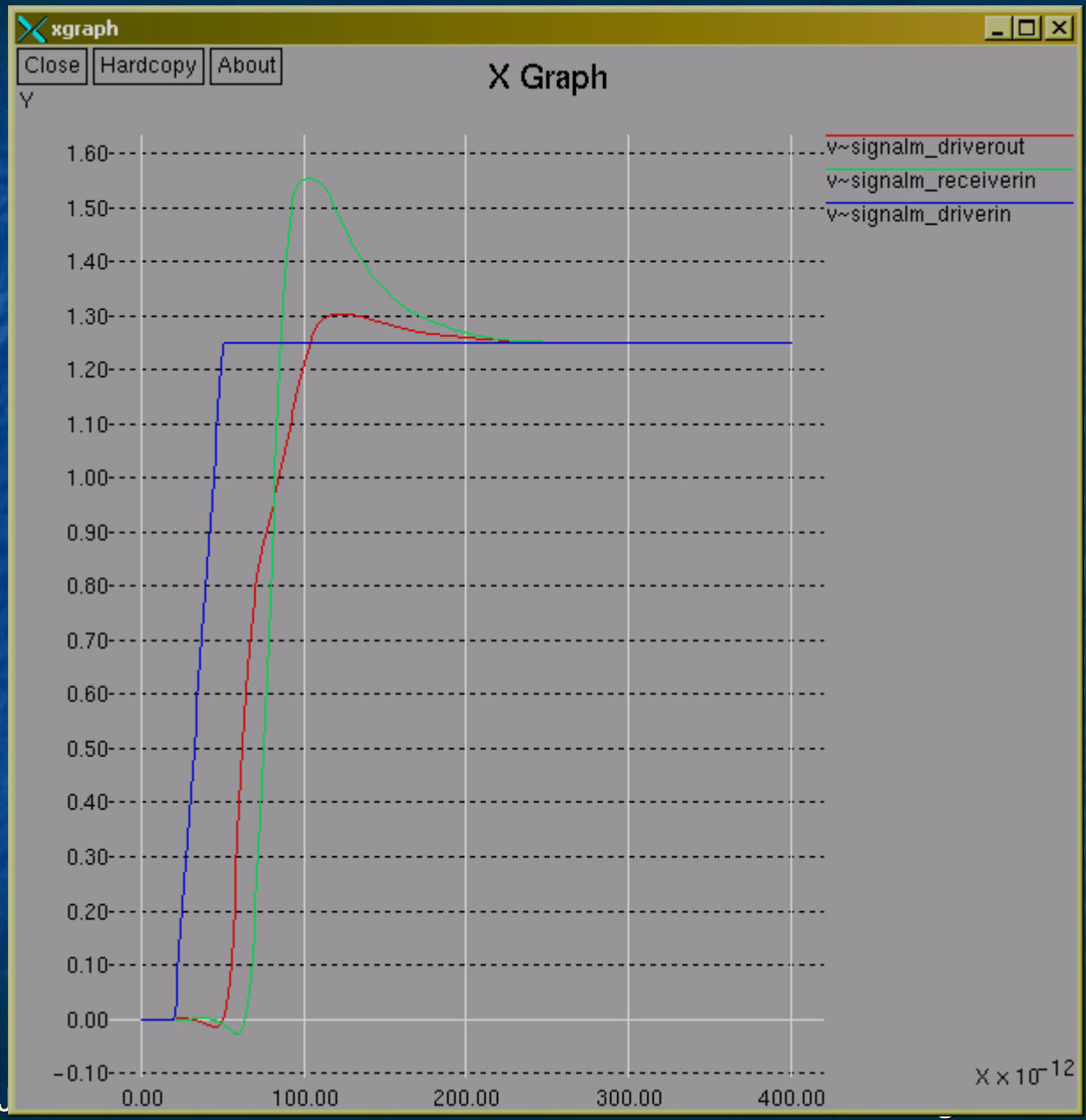
1000u line

25 signals

Victim up

NO RLC noise

Timing



- 1000u line
- 25 signals
- Victim up
- WC RLC noise (+)

Timing

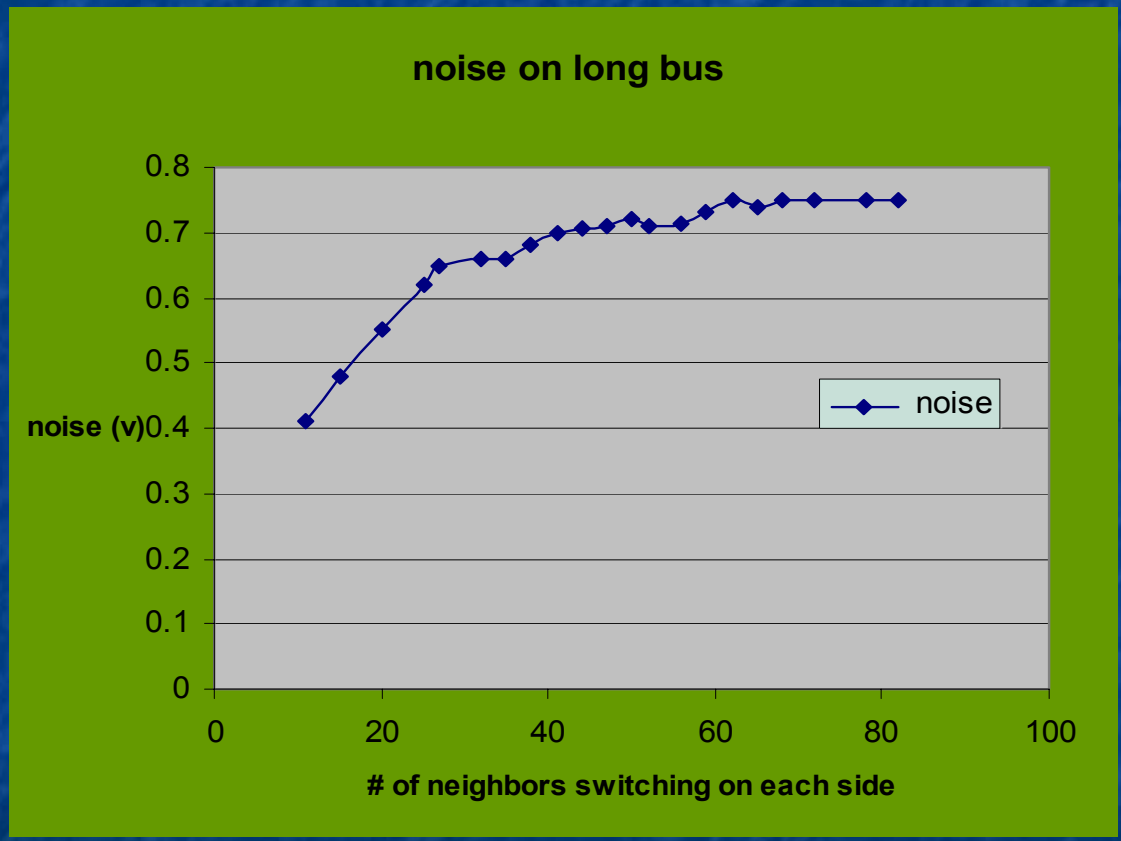
1000u line

25 signals

Victim up

WC RLC noise (-)

Window of influence



On-chip interaction: complex attack

Inductive neighborhood summary

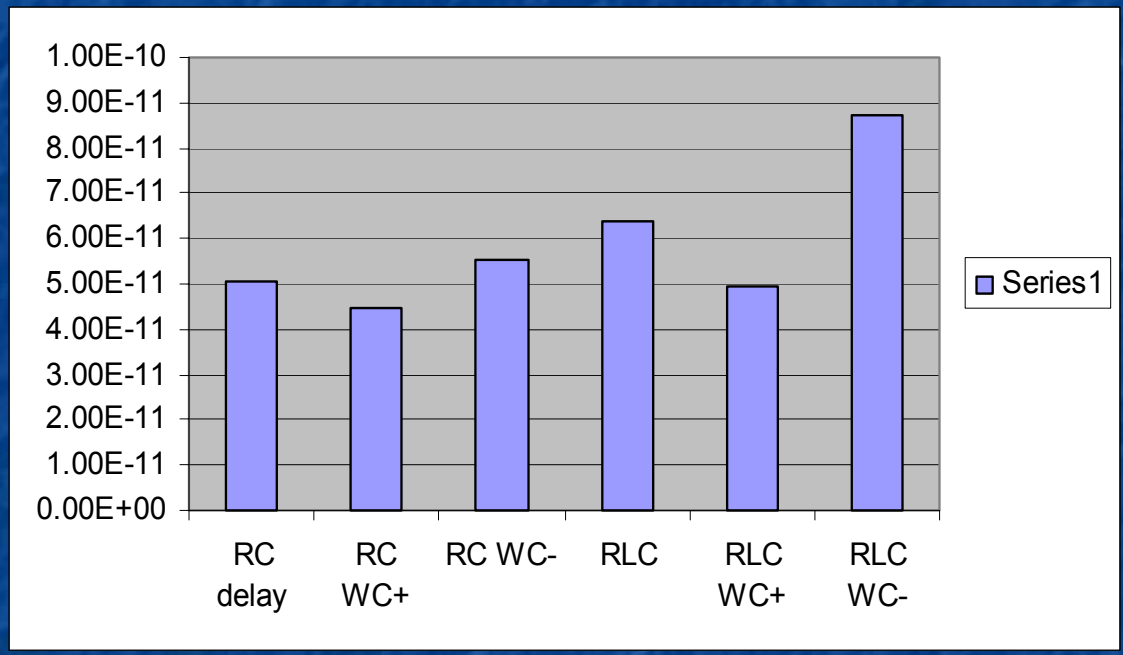
- Inductive attackers in a large neighborhood
  - On same layer
  - On other layers
  - If wrong way wires, not only on parallel wires
- Returns influence in a large neighborhood
  - Width and location of returns important

This gives rise to complexity – much more than capacitive extraction!

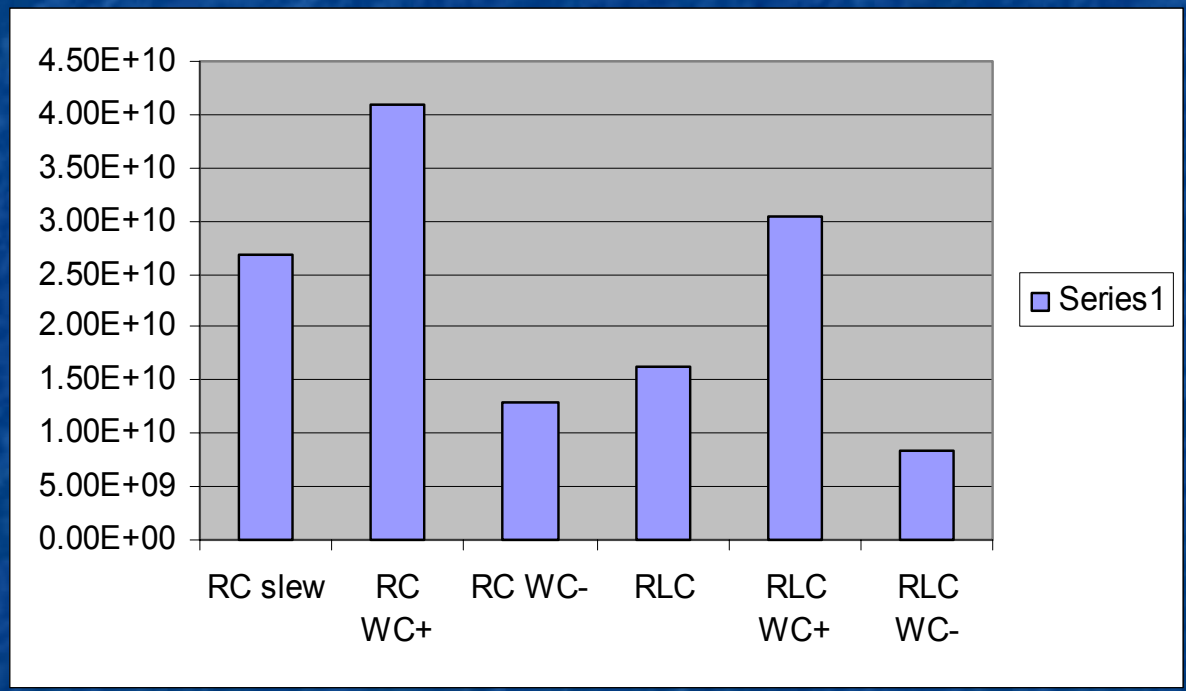
Multiple attackers

- Worst case scenario is terrible!
- If we used this, design could not be done
- Probability of worst case is almost zero
- However, a reasonable probability window must be chosen by designers
- **This choice of probability window can be the source of inaccuracy greater than inductive modeling!**
- Complexity – not accuracy.

Top metal delay: driver output



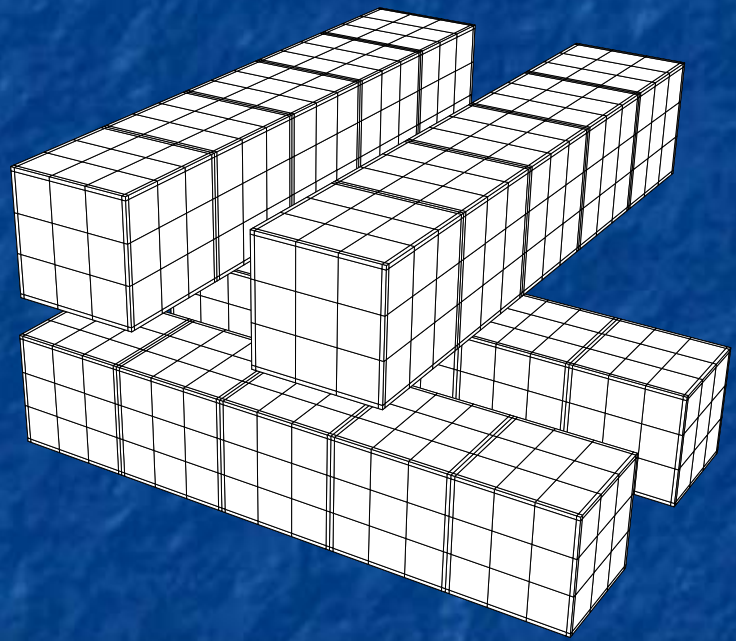
Top metal slew: receiver input



Overview of PEEC

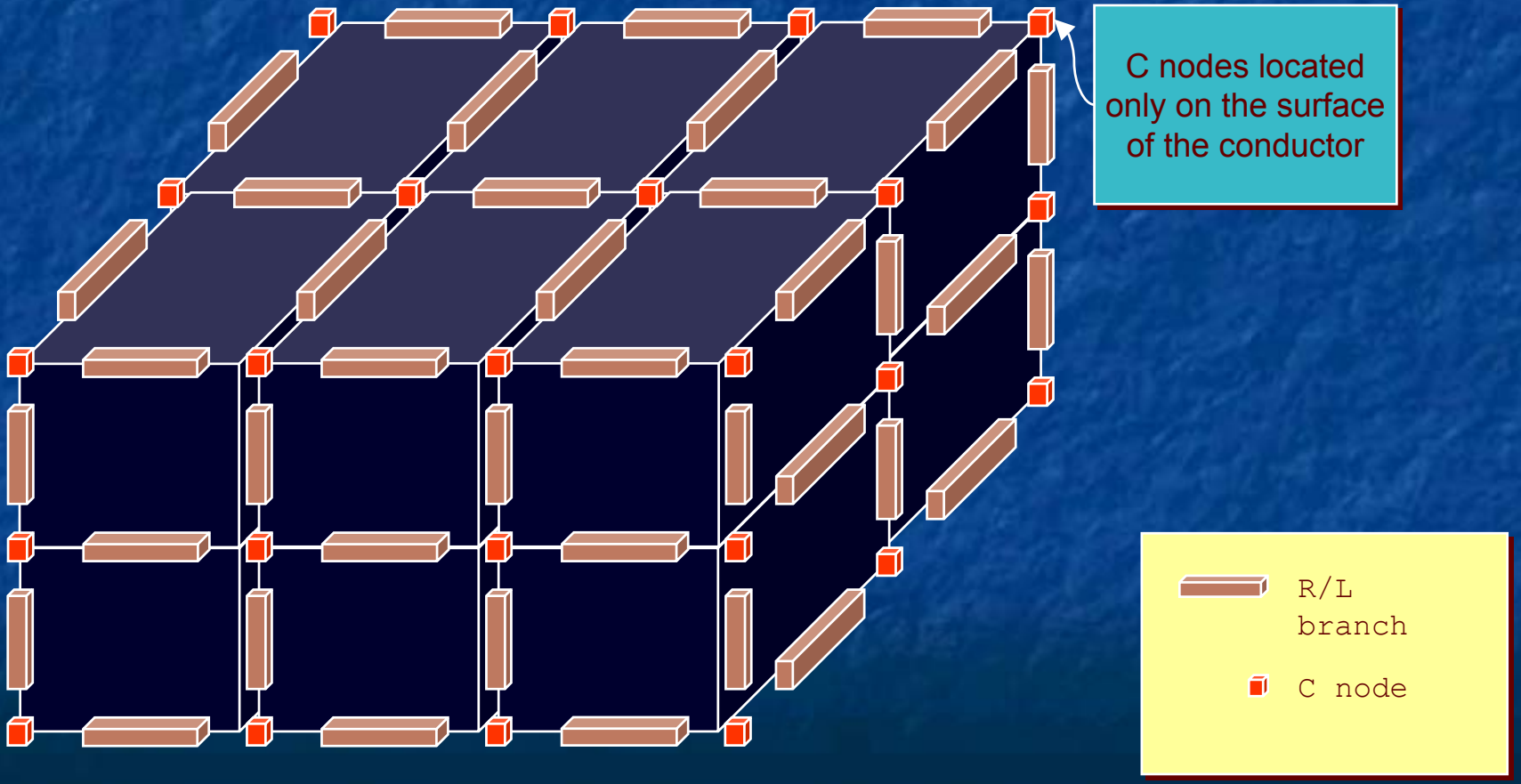
- "Equivalent circuit models for three dimensional multiconductor systems", IEEE Trans. MTT, A. E. Ruehli, 1974.
- The PEEC approximation is based upon the proper electromagnetic interpretation of the various terms in the electric field integral equation (EFIE)
- Elements in the resulting matrix solution are related to equivalent circuit elements which can be incorporated into a non-linear circuit simulator.
- The main advantages of this approach are
  - output is a SPICE netlist
  - Ability to model any electromagnetic interaction
  - Excellent for understanding of basic signal, power grid, clock effects
- The main disadvantages are
  - Too detailed for most on-chip applications

Discretization for PEEC



3D PEEC Model

- In general, conductors are modeled using a 3D PEEC model where current flows in x-, y-, and z-directions



Overview of the PEEC Concept

- The vector and scalar potential functions

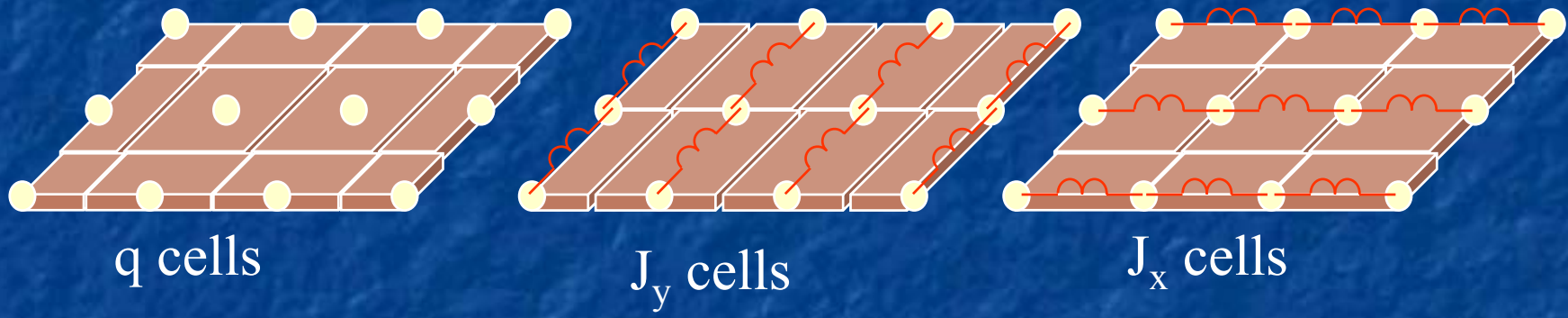
$$\bar{A}(\bar{r},t)=\frac{\mu}{4\pi}\sum_{k=1}^{K}\int_{v_k}\frac{\bar{J}(\bar{r}',t-|\bar{r}-\bar{r}'|/c)}{|\bar{r}-\bar{r}'|}dv'$$

$$\Phi(\bar{r},t)=\frac{1}{4\pi\varepsilon}\sum_{k=1}^{K}\int_{v_k}\frac{q(\bar{r}',t-|\bar{r}-\bar{r}'|/c)}{|\bar{r}-\bar{r}'|}dv'$$

$$\frac{\bar{J}(\bar{r},t)}{\sigma}+\frac{\mu}{4\pi}\frac{\partial}{\partial t}\sum_{k=1}^{K}\int_{vk}\frac{\bar{J}(\bar{r}',t')}{|\bar{r}-\bar{r}'|}dv'+\frac{1}{4\pi\varepsilon}\sum_{k=1}^{K}\nabla\left[\int_{vk}\frac{q(\bar{r}',t')}{|\bar{r}-\bar{r}'|}dv'\right]=0$$

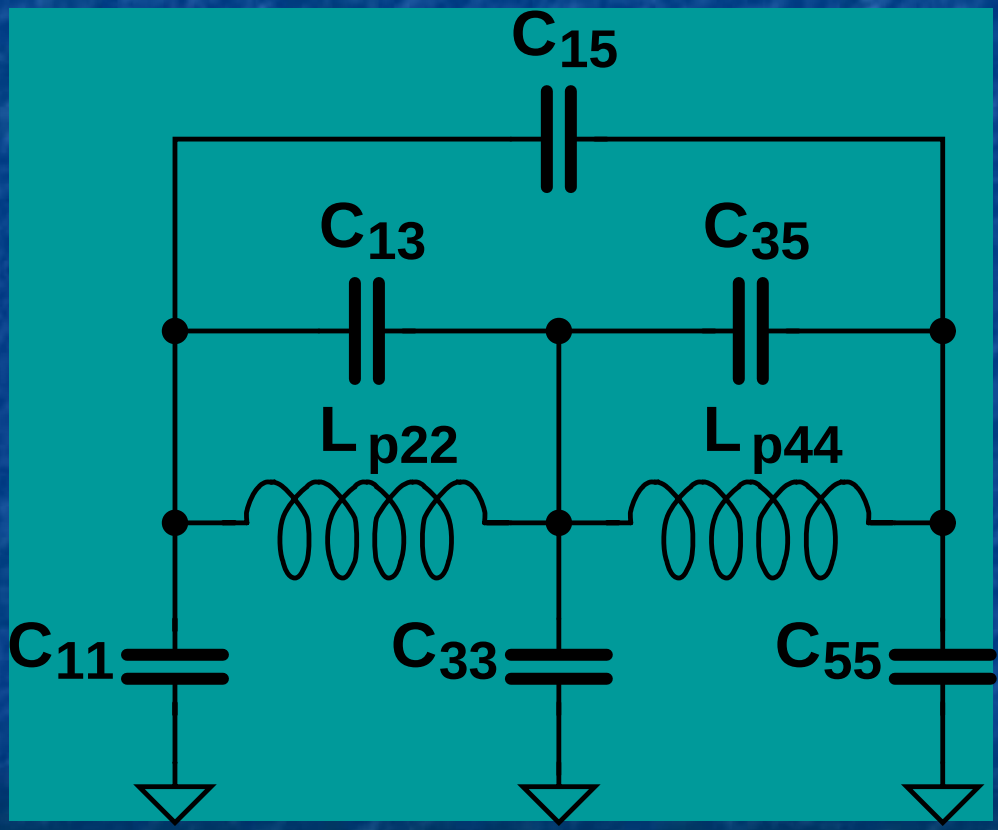
along with $J = \sigma E$ are substituted into the EFIE, resulting in

Basic PEEC cell



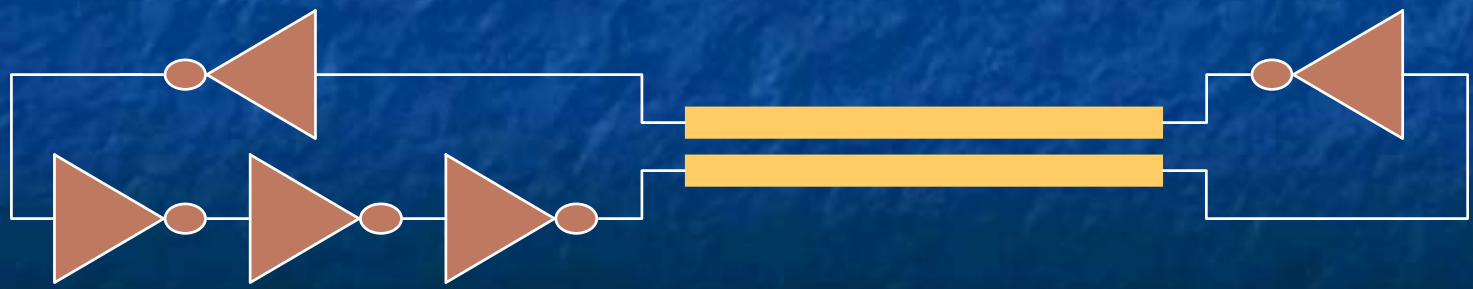
- The charge density, *q*, and current density, *J*, are discretized into capacitive and inductive/resistive cells, respectively

PEEC: basic circuit



The MR problem

- Circuit simulators (e.g. Spice) simulate nonlinear networks well but at high cost
- Extraction, packaging and interconnect modelling generate large linear (RLC) networks (especially in high speed GHz logic,clock and packaging design
- Nonlinear simulators too slow to simulate large linear networks



MR Requirements

- Reduce large linear networks for standalone time/frequency domain simulation
- Reduce and macromodel large linear networks for nonlinear simulation
- reduction with error control, and simulation transparently to the user
- Applicable to on-chip logic interconnect, clock, power and gnd nets, packaging pin and interconnect models
- tricky mathematical techniques necessary to accomplish this for all frequency ranges

MR: AWE approach

$$I(s) = H(s)V(s)$$

$$I(s) = (H_0 + H_1 s + H_2 s^2 + \ldots)V(s)$$

$$I(s) = \left(\frac{a_0 + a_1 s + a_2 s^2 + \ldots + a_{q-1} s^{q-1}}{b_0 + b_1 s + b_2 s^2 + \ldots + b_q s^q} \right) V(s)$$

$$I(s) = \left(\sum_{i=1}^{q} \frac{k_i}{s - p_i} \right) V(s)$$

$$i(t) = \left(\sum_{i=1}^{q} k_i e^{p_i t} \right) * v(t)$$

Problems with AWE

- Moments generated loose accuracy
- The number of poles is limited (may be ok for RC)
- Order of approximation is not chosen automatically (no idea about the error)
- Macromodelling not in block form in existing codes
- Krylov subspace provides greater range of accuracy for same initial cost as in AWE (DC decomposition)
- Block algorithm make MIMO possible
- Automatic error control for order of approximation based on residual

Krylov based iteration

$$E\dot{x} = Ax + Bu \qquad y = C^T x + Du$$

$$\hat{E}\dot{\hat{x}} = \hat{A}\hat{x} + \hat{B}u \qquad \hat{y} = \hat{C}^T\hat{x} + \hat{D}u$$

$$span\left\{(A-\sigma E)^{-1}B,(A-\sigma E)^{-1}E(A-\sigma E)^{-1}B,((A-\sigma E)^{-1}E)^2(A-\sigma E)^{-1}B,\ldots\right\} \Rightarrow V_j$$

- V is an orthogonal subspace

$$V_j^T(A-\sigma E)^{-1}E\dot{\hat{x}} = V_j^T(A-\sigma E)^{-1}AV_j\hat{x} + V_j^T(A-\sigma E)^{-1}Bu$$

$$\hat{y} = C^T V_j\hat{x} + Du$$

Residual based stopping criterion

$$X(s) = (sE - A)^{-1} B$$ Actual frequency response

$$\hat{X}(s) = V_j (s\hat{E} - \hat{A})^{-1} \hat{B}$$ Approximate response

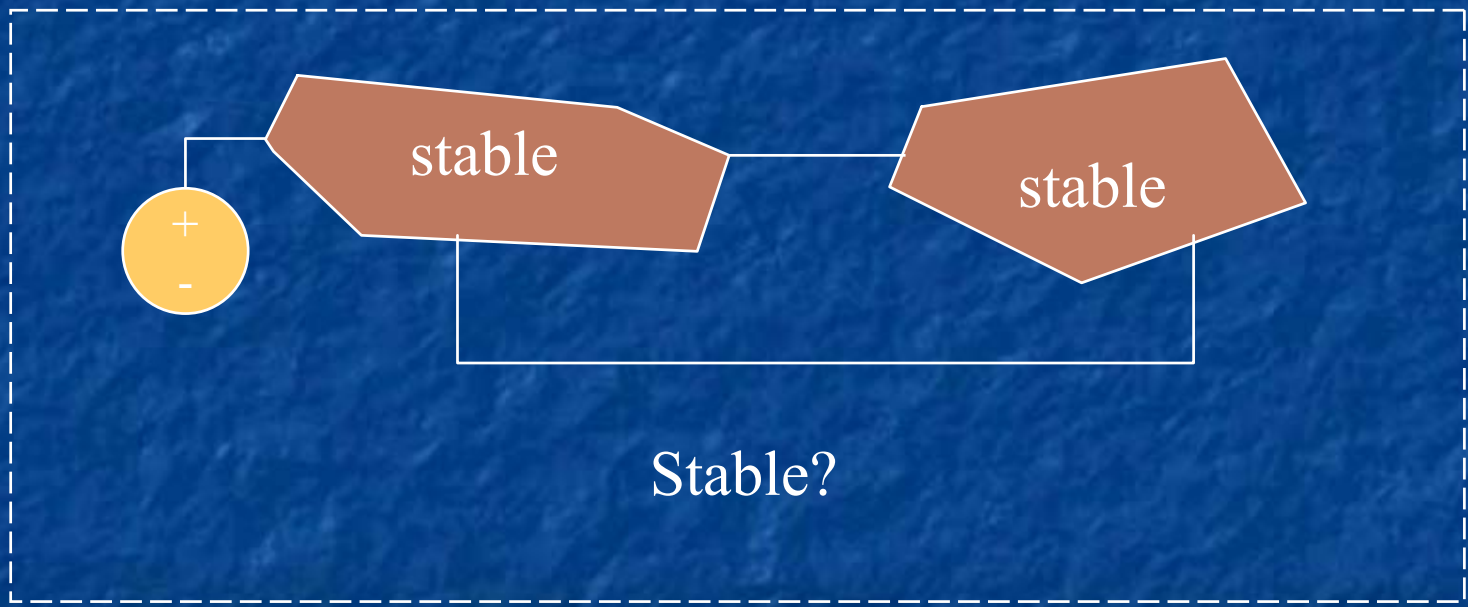
$$error = C^T (X(s) - \hat{X}(s))$$ Actual error (expensive!)

$$\hat{R}(s) = (sE - A)\hat{X}(s) - B$$
$$= (sE - A)V_j (s\hat{E} - \hat{A})^{-1} \hat{B} - B$$ Residual error (cheap!)

- residual error has a frequency indep component which gets calculated only once for a given model order and freq dependent component which is inexpensive to calculate for entire freq range
- residual weighted to get low freq and DC accuracy

Passivity

- Are stable systems a closed set? NO!



References and further study

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