Simultaneous Test Pattern Compaction, Ordering and X-Filling for Testing Power Reduction

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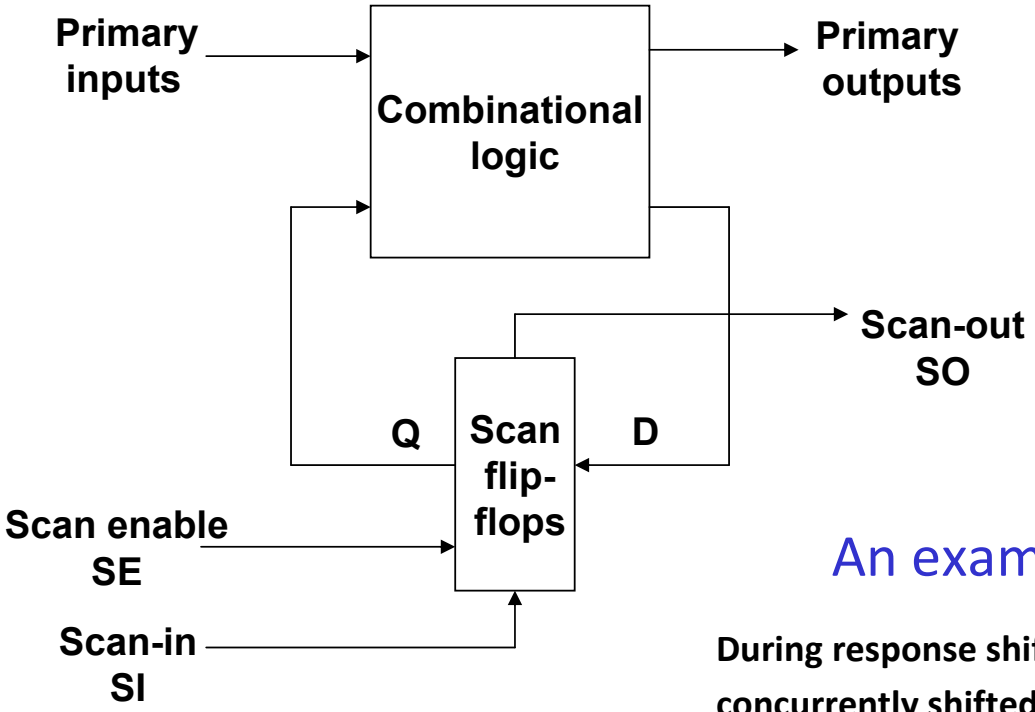
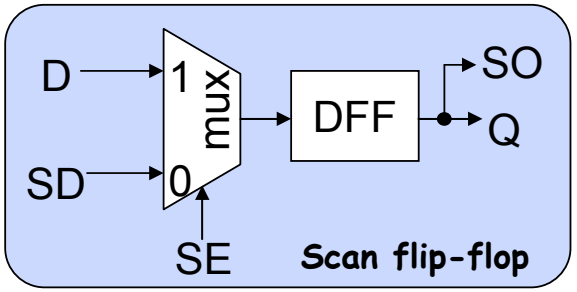
Outline

Scan-Based Testing

Sequential Circuit with Scan



Scan Flip-Flop



An example scan based test

During response shift-out, next pattern can be concurrently shifted in.

Increasing Testing Power Concerns

1. Testing power is several times higher than normal mode power
    - Requirements of test time reduction
        - Increasing test concurrency (Test multiple modules simultaneously)
        - Increasing frequency of scan shift
    - Requirements of test data volume reduction
        - Compression and compaction techniques elevate circuit switching
    - Various stressful conditions (voltage and temperature)
    - Redundant switching in circuit logic during scan shift

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     - Compression and compaction techniques elevate circuit switching
   - Various stressful conditions (voltage and temperature)
   - Redundant switching in circuit logic during scan shift
2. Excessive testing power causes
   - Low reliability
   - Structural damage to the silicon or package
   - Large voltage drop, leading to erroneous data

Test Power Breakdown

1. Average power vs. peak power
   - Average power: reliability (temperature, EM)
   - Peak power: packaging issues, IR drop

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   - High Frequency Shifts: Peak and Average power becomes a concern
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   - High Frequency Shifts: Peak and Average power becomes a concern
   - Capture power: Fast capture pulses in transition patterns cause Peak power (IR drop) issues
3. Our approach
   - considers both shift and capture power
   - can be applied to both average and peak power

Existing Techniques for Testing Power Reduction

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   - Test patterns consist of care bits and don't-care bits, e.g., a pattern (0XXX1XX) has 5 don't care bits and 2 care bits
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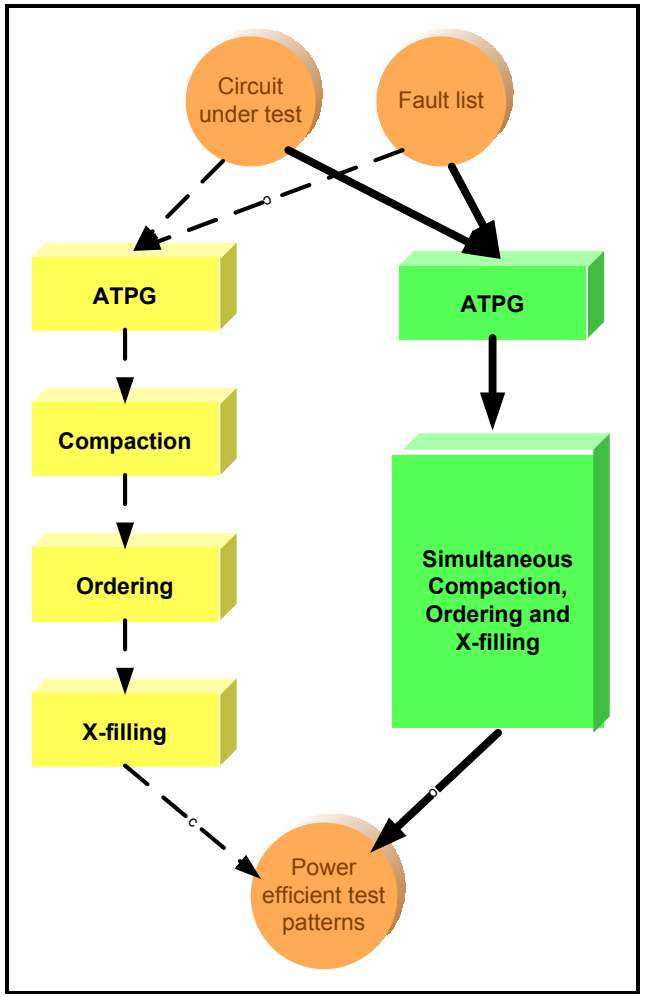
3. Three major techniques for power-aware ATPG have been proposed, i.e., compaction, ordering and X-filling
4. However, most previous researches perform the three optimizations sequentially, which may cause loss of optimality

Major Contributions

1. Propose an optimal formulation for simultaneous test pattern compaction, ordering and X-filling for test mode power minimization.
    - A uniform pseudo Boolean (PB)-based algorithm, applicable to both average and peak power minimization.
    - Reduce power dissipation by 47%, compared to sequential approach.



Pseudo-Boolean (PB) Problem

- *Pseudo-Boolean (PB) Constraint* is an inequality

$$C_0 p_0 + C_1 p_1 + \cdots + C_{n-1} p_{n-1} \geq C_n,$$

  where p_i is a literal and C_i is an integer coefficient for each i.
- An *objective function* is a sum of weighted literals on the same form as PB constraints.
- The *Pseudo-Boolean Constraint Problem* is to find a satisfying assignment to a set of PB-constraints that minimizes a given objective function.
- PB Problem can be solved by
  - A generic 0-1 ILP solver, e.g., mosek
  - A specialized SAT-based solver, e.g., minisat+

Test Power Modeling

- Scan energy for the test vectors, $\overrightarrow{s_1}, \cdots, \overrightarrow{s_n}$ is

$$E_{reg}(\overrightarrow{s_1}, \cdots, \overrightarrow{s_m}) = \sum_{i=1}^{m} \sum_{j=1}^{K-1} w_{ij} \cdot |s_i^j - s_i^{j+1}|,$$

where w_{ij} is the weight to characterize the loading capacitance of the scan-chain registers and the weighted transition count (WTC), which has been normalized based on the K.

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- Capture energy due to the switch of two test vectors, $\overrightarrow{s_i} \rightarrow \overrightarrow{s_{i+1}}$, is

$$E_{cap}(\overrightarrow{s_i} \rightarrow \overrightarrow{s_{i+1}}) = \sum_{g \in G} C_g \cdot |v_g(\overrightarrow{s_i}) - v_g(\overrightarrow{s_{i+1}})|$$

where C_g is the loading capacitance of gate or register g in the circuit which is calculated based on Weighted Switching Activity (WSA). $v_g(\overrightarrow{s_i})$ is the logic value at gate g under test vector $\overrightarrow{s_i}$.

Test Power Modeling

- Average test power for test vectors, $\overrightarrow{s_1}, \cdots, \overrightarrow{s_{\hat{m}}}$, is

$$P(\overrightarrow{s}, \hat{m}) = \frac{E_{reg}(\overrightarrow{s_1}, \cdots, \overrightarrow{s_{\hat{m}}}) + \sum_{i=1}^{\hat{m}-1} E_{cap}(\overrightarrow{s_i} \rightarrow \overrightarrow{s_{i+1}})}{\hat{m}}.$$

- Peak test power for test vectors, $\overrightarrow{s_1}, \cdots, \overrightarrow{s_{\hat{m}}}$, is

$$P(\overrightarrow{s}) = \max(\max_i(\sum_{j=1}^{K-1} w_{ij} \cdot |s_i^j - s_i^{j+1}|), \max_i(C_g \cdot |v_g(\overrightarrow{s_i}) - v_g(\overrightarrow{s_{i+1}})|))$$

Problem Formulation: simultaneous test pattern compaction, ordering and X-filling (COX) for test power minimization

Given a set of test patterns $\overrightarrow{t_1}, \cdots \overrightarrow{t_m}$, find an ordered set of test vectors $\overrightarrow{s_1}, \cdots \overrightarrow{s_{\hat{m}}}$ such that

- each $\overrightarrow{s_i} \in \{0,1\}^K$ (i.e., contains no don't-care terms),
- $\hat{m} \leq m$,
- fault coverage is preserved (i.e., for each $\overrightarrow{t_i}$ there is some $\overrightarrow{s_j}$ such that $\overrightarrow{s_j} \dashv \overrightarrow{t_i}$),
- the testing power dissipation objective (either overall dissipation or peak dissipation) is minimized.

PB Formulation for COX Problem

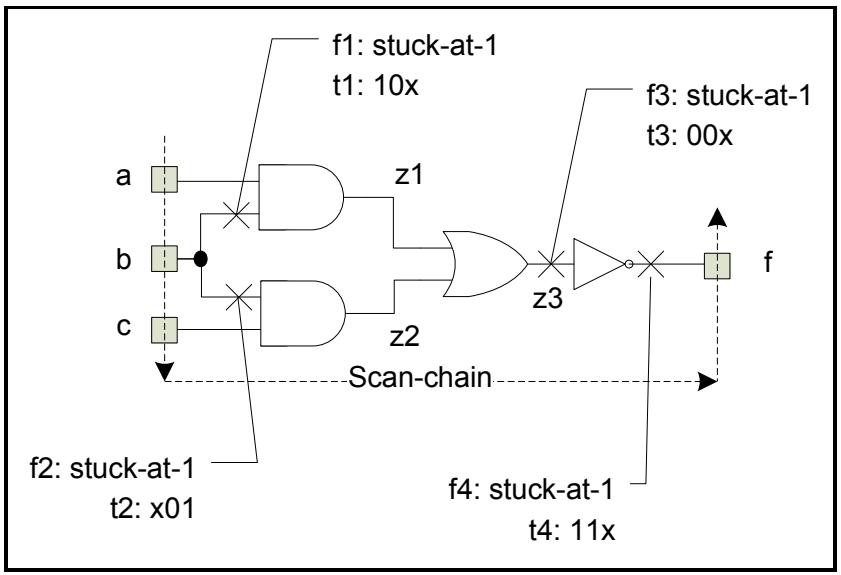
COX problem

- the testing power dissipation objective is minimized.
- fault coverage is preserved,
- test vectors contain no don't-care terms,
- $\hat{m} \leq m$,

PB-based formulation

minimize	$P(\overrightarrow{s}, \hat{m})$
subject to	
$\mathrm{CNF}_G(\overrightarrow{s_i})$	for $i = [1, m]$,
$\bigvee_{j=1}^{\hat{m}}(\overrightarrow{s_j} \dashv \overrightarrow{t_i})$	for $i = [1, m]$,
$s_i^j \in \{0, 1\}$	for $i = [1, m]$, $j = [1, K]$,

Example



- Nine 0-1 variables (literals) are needed:

$$\overrightarrow{s_1} = (s_1^1, s_1^2, s_1^3) \in \{0,1\}^3$$
$$\overrightarrow{s_2} = (s_2^1, s_2^2, s_2^3) \in \{0,1\}^3$$
$$\overrightarrow{s_3} = (s_3^1, s_3^2, s_3^3) \in \{0,1\}^3$$

- the objective function is

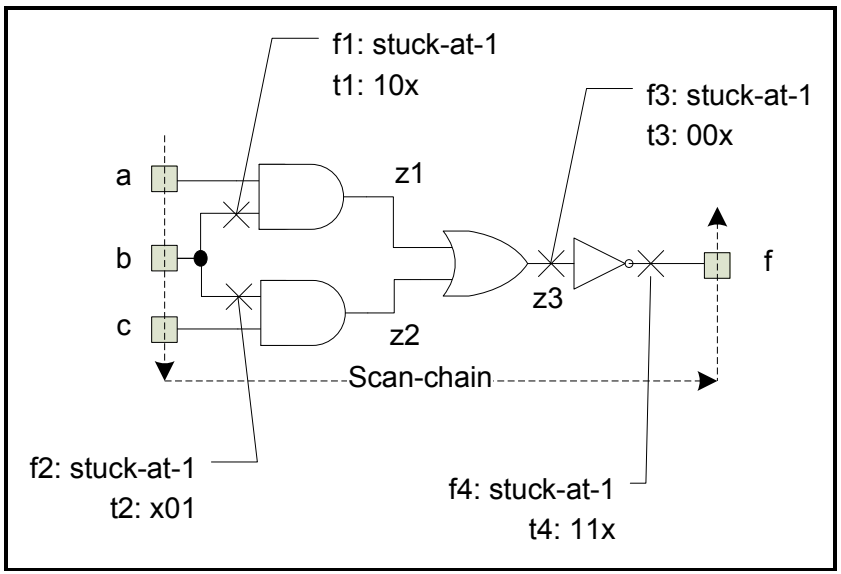
$$E_{reg} = \sum_{i=1}^{3} \sum_{j=1}^{2} |s_i^j - s_i^{j+1}|$$
$$E_{cap} = \sum_{i=1}^{2} \sum_{g \in G} C_g \cdot |v_g(\overrightarrow{s_i}) - v_g(\overrightarrow{s_{i+1}})|,$$

where $G = \{z_1, z_2, z_3, f\}$.

- $|x_1 - x_2| = x_1 \oplus x_2$ can be rewritten in CNF:

$$(\neg x_1 \vee \neg x_2 \vee y) \wedge (x_1 \vee x_2 \vee y) \wedge$$
$$(\neg x_1 \vee x_2 \vee \neg y) \wedge (x_1 \vee \neg x_2 \vee \neg y).$$

Example



The logic value constraints

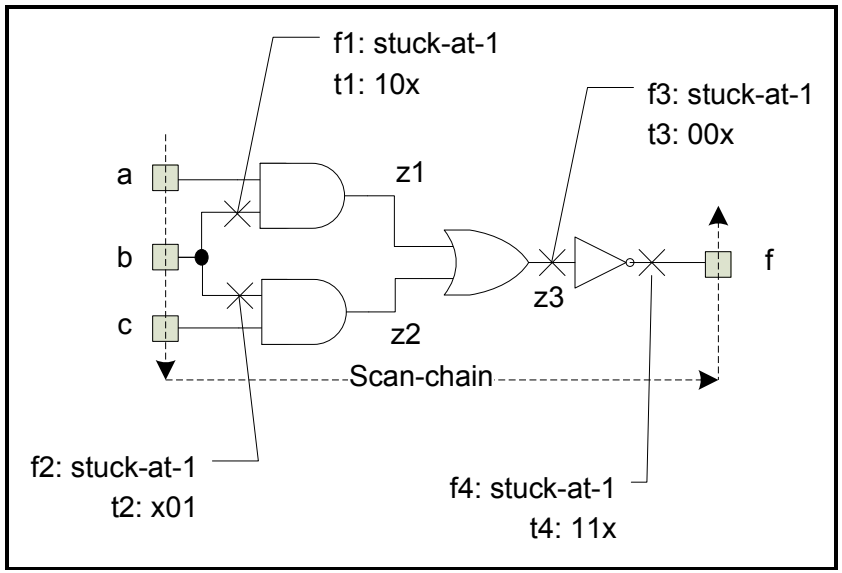
$$\mathrm{CNF}_G(\overrightarrow{s_i}),\ \text{for } i = [1, m],$$

are as follows.

$$(s_i^1 \vee \neg v_{z_1}^i) \wedge (s_i^2 \vee \neg v_{z_1}^i) \wedge (\neg s_i^1 \vee \neg s_i^2 \vee v_{z_1}^i) \wedge$$
$$(s_i^3 \vee \neg v_{z_2}^i) \wedge (s_i^2 \vee \neg v_{z_2}^i) \wedge (\neg s_i^3 \vee \neg s_i^2 \vee v_{z_2}^i) \wedge$$
$$(\neg v_{z_1}^i \vee v_{z_3}^i) \wedge (\neg v_{z_2}^i \vee v_{z_3}^i) \wedge (v_{z_1}^i \vee v_{z_2}^i \vee \neg v_{z_3}^i) \wedge$$
$$(\neg v_{z_3}^i \vee \neg v_{z_4}^i) \wedge (v_{z_3}^i \vee v_{z_4}^i)$$

where v_g^i denotes $v_g(\overrightarrow{s_i})$, and the above four constraints represents the characteristic function to compute the logic value of `AND` gates z_1 and z_2, `OR` gate z_3 and `INV` gate f, respectively, under test vector $\overrightarrow{s_i}$, for $i = 1, \cdots, 3$.

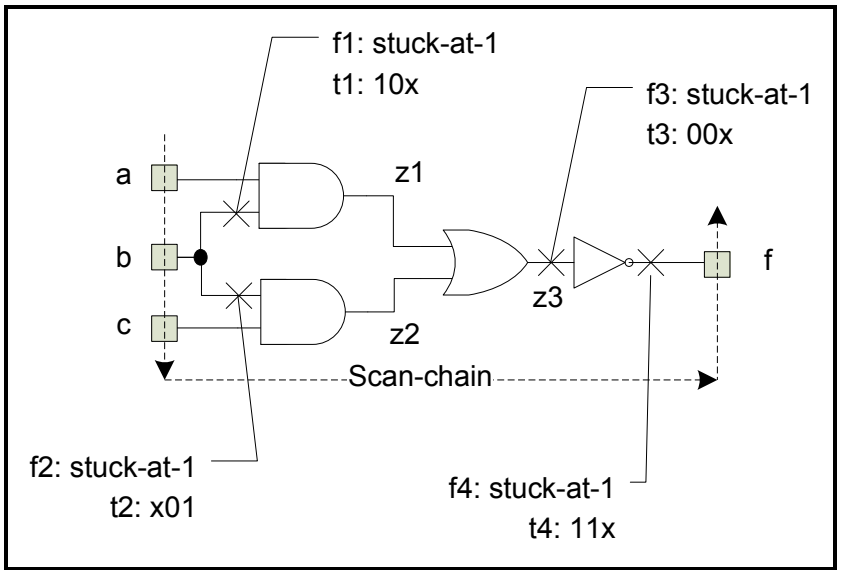
Example



To cover all faults, we have

$$((s_1^1 \wedge \neg s_1^2) \vee (s_2^1 \wedge \neg s_2^2) \vee (s_3^1 \wedge \neg s_3^2)) \wedge$$
$$((\neg s_1^2 \wedge s_1^3) \vee (\neg s_2^2 \wedge s_2^3) \vee (\neg s_3^2 \wedge s_3^3)) \wedge$$
$$((\neg s_1^1 \wedge \neg s_1^2) \vee (\neg s_2^1 \wedge \neg s_2^2) \vee (\neg s_3^1 \wedge \neg s_3^2)) \wedge$$
$$((s_1^1 \wedge s_1^2) \vee (s_2^1 \wedge s_2^2) \vee (s_3^1 \wedge s_3^2))$$

Example



After solving the above PB constraint problem, the optimal solution returned by PB solver is

$$\overrightarrow{s_1} = (0, 0, 1)$$
$$\overrightarrow{s_2} = (1, 1, 1)$$
$$\overrightarrow{s_3} = (1, 0, 0)$$

Peak Power Minimization

Original formulation

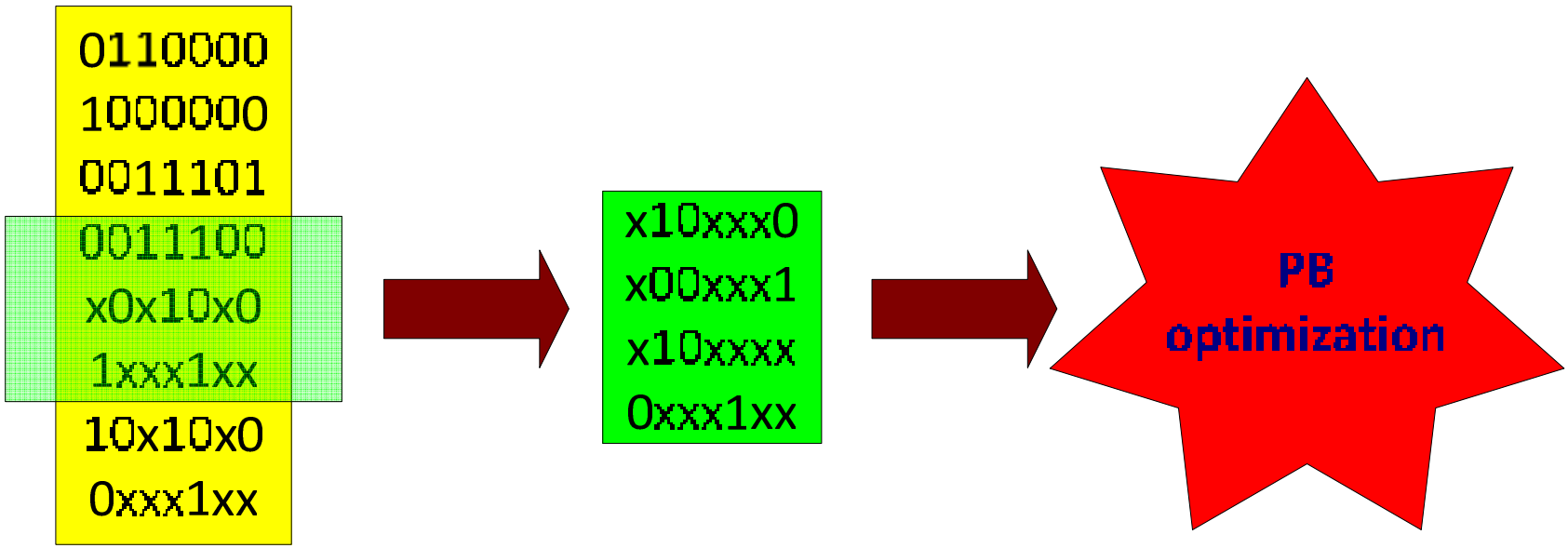
$$\begin{aligned} \text{minimize } P(\overrightarrow{s}) = \quad & \max(\max_{i,j}(w_{ij} \cdot |s_i^j - s_i^{j+1}|), \\ & \max_i(C_g \cdot |v_g(\overrightarrow{s_i}) - v_g(\overrightarrow{s_{i+1}})|)) \\ \text{subject to} \quad & \text{all constraints from average power minimization} \end{aligned}$$

PB-based formulation

$$\begin{aligned} \text{minimize} \quad & t \\ \text{subject to} \quad & \sum_{j=1}^{K-1} w_{ij} \cdot |s_i^j - s_i^{j+1}| \leq t \\ & C_g \cdot |v_g(\overrightarrow{s_i}) - v_g(\overrightarrow{s_{i+1}})| \leq t \\ & \text{all other constraints from average power minimization} \end{aligned}$$

Can be solved by the binary search of t.

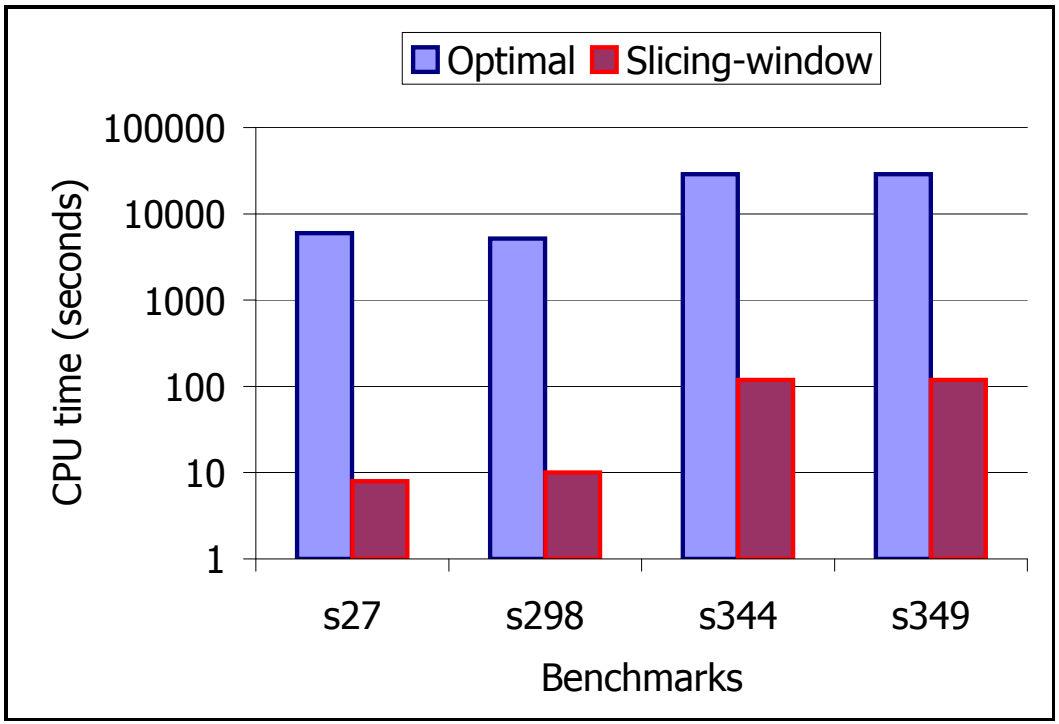
Speedup By Slicing Window



Experimental Settings

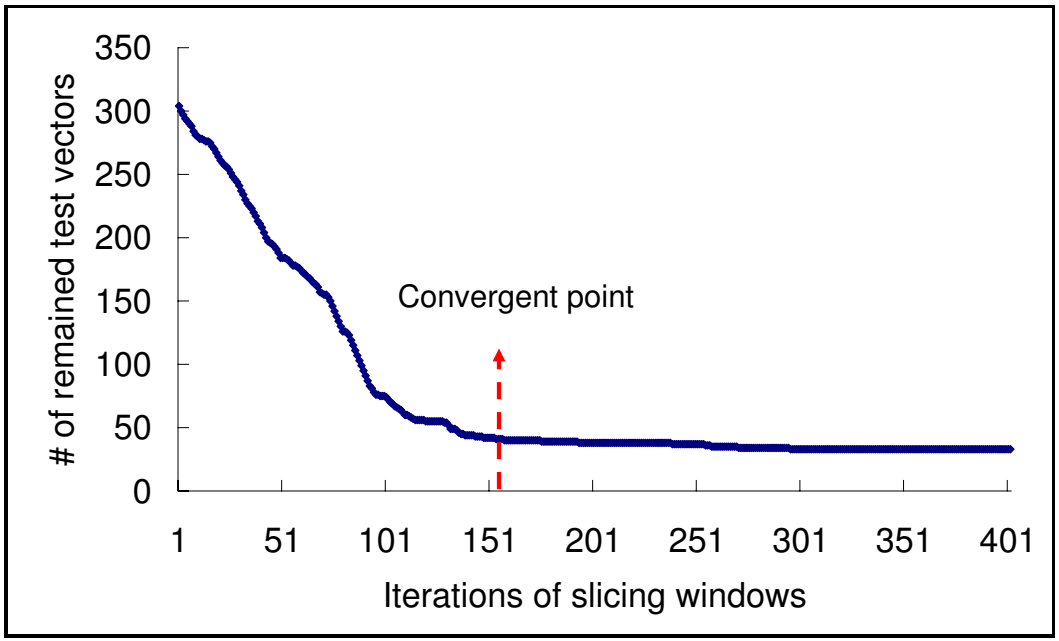
- ISCAD'89 benchmark circuits
- Test pattern generated by ATALANTA
- PB problem solved by minisat+
- Baseline sequential algorithm ("seq")
  - Compacted by ATALANTA
  - X-filled by repeated filling [Costa, IWLS'98]
  - Ordered by a TSP-based algorithm [Costa, IWLS'98]

Optimal vs. Slicing Window (SW)-Based Heuristic



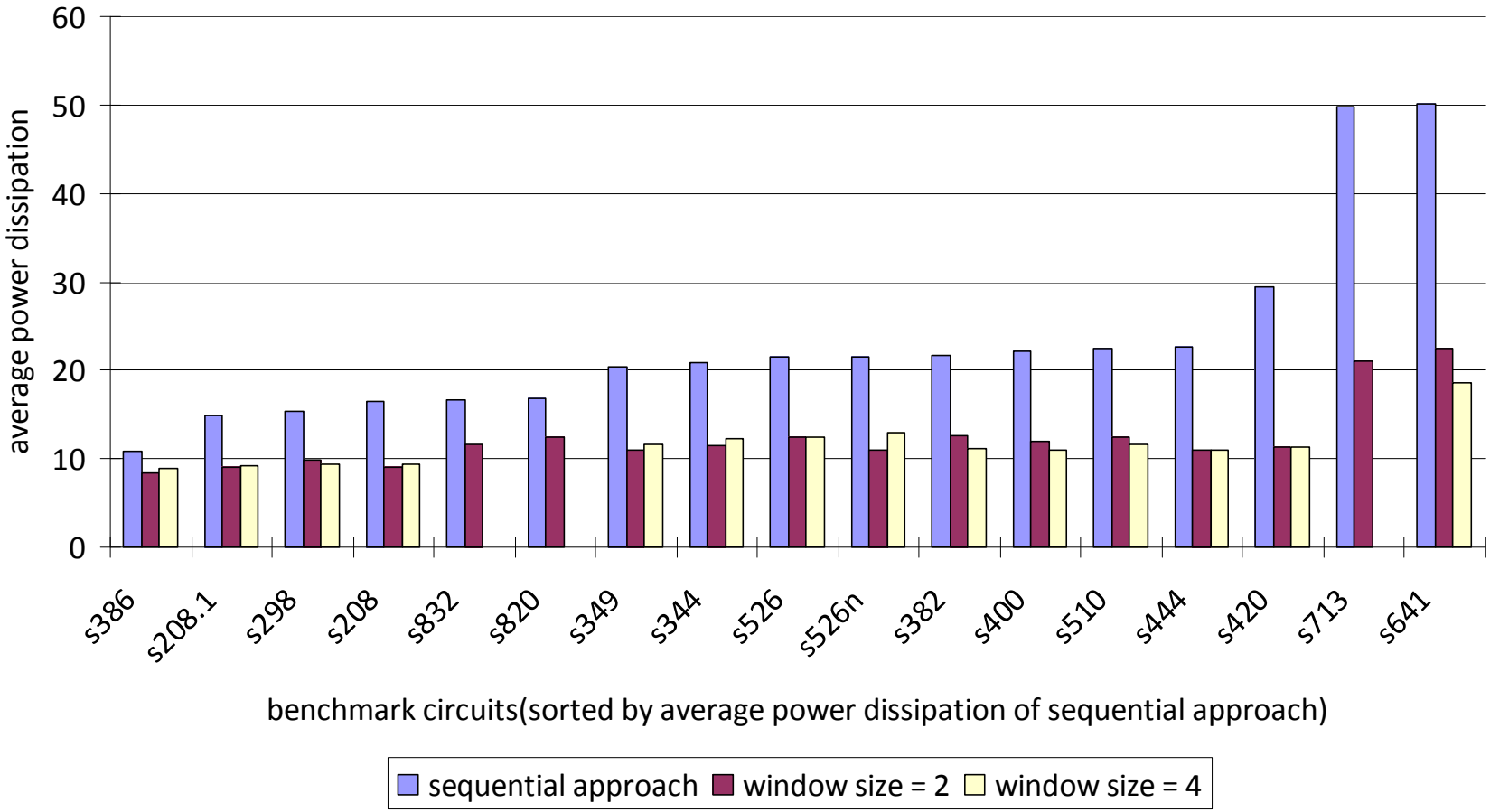
- Due to the capability of PB solver, four small circuits (s27, s298, s344, s349) are tested using 20 test patterns
- The same results are obtained by the two approaches.
- SW is three orders of magnitude faster.

Convergency Slicing Window

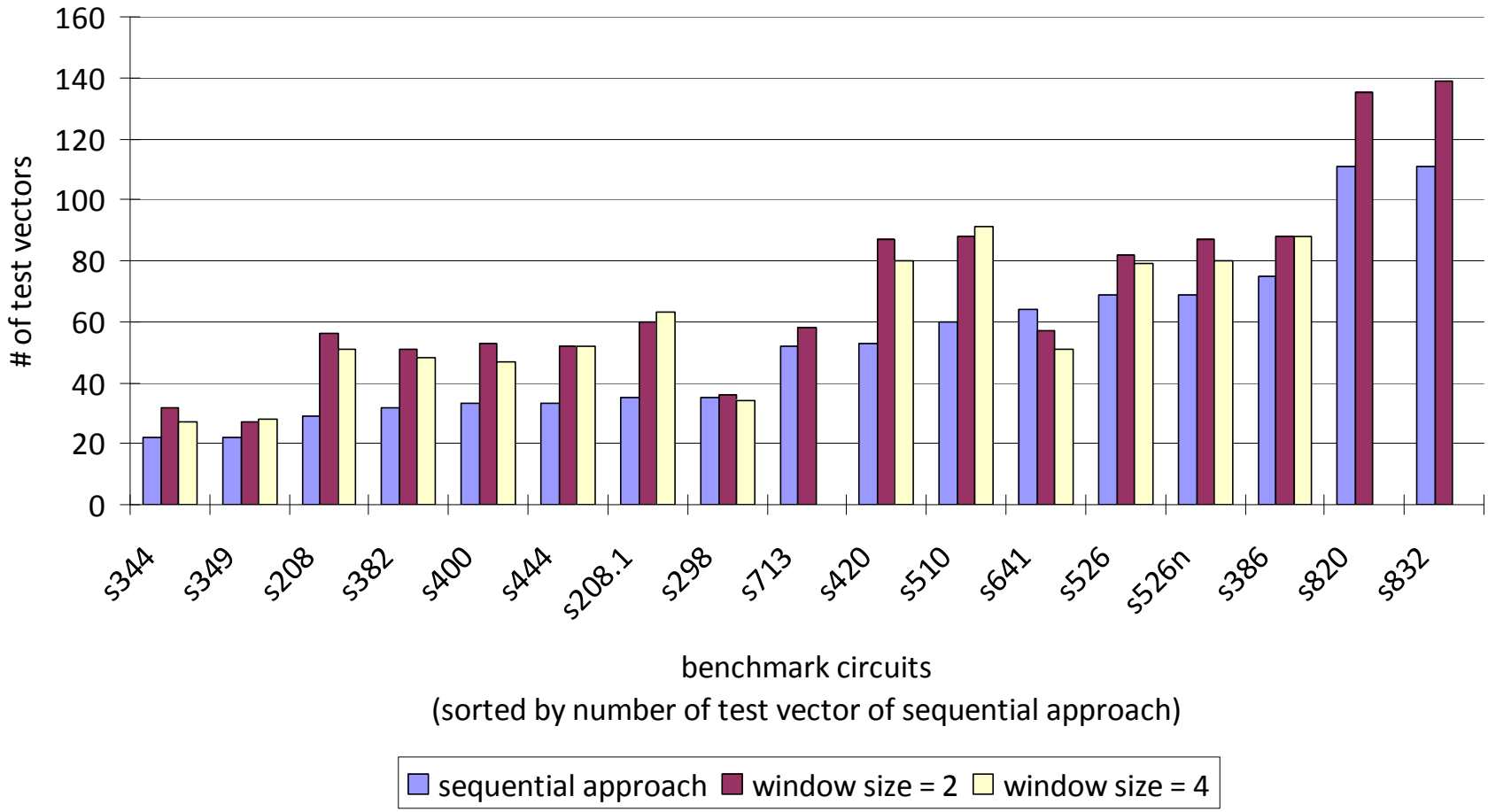


- Window size 4
- Benchmark: s298
- SW converges when 150 windows are passed, i.e. 4 iterations

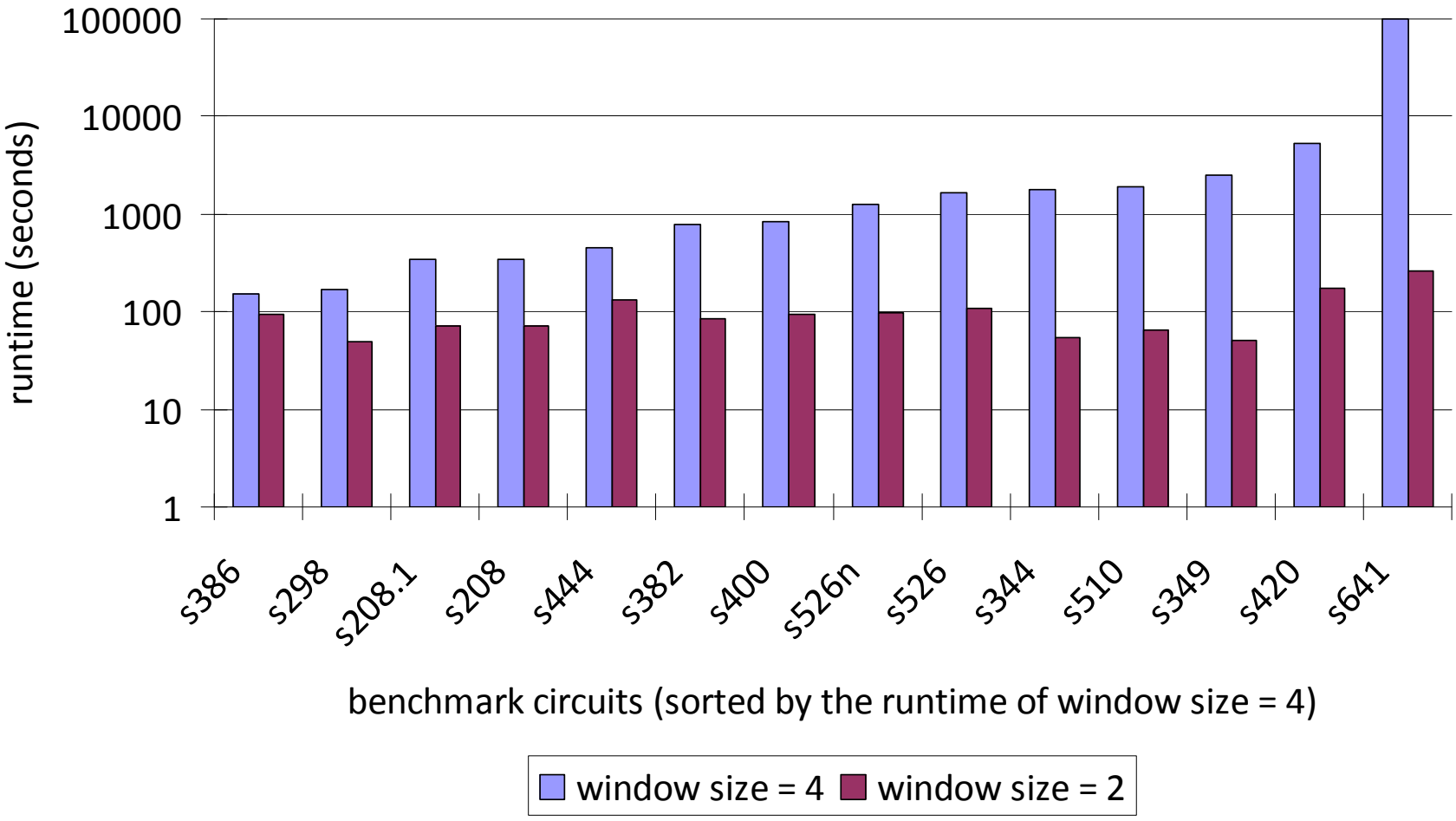
Power Dissipation Comparisons



Test Set Size Comparisons



Runtime Comparisons



Conclusions and Future Work

- A uniformed formulation for the problem of simultaneously compacting, ordering, and Xfilling to minimize power dissipation is proposed
- Our proposed approach reduces average power by 47% compared to the conventional sequential approach
- In the future, we will
  - conduct experiments on average power minimization under peak power constraint
  - futhere improve the efficiency of the proposed algorithm