Wave Digital Filter based Analog Circuit Emulation on FPGA

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***Abstract*— Unlike well accepted FPGA emulation for digital circuits, there is no winning emulation solution for analog and mixed-signal (AMS) circuits. This paper presents an analog circuit emulation based on wave digital filters (WDFs), which covers the entire flow of transforming an AMS circuit from SPICE netlist to hardware implementation in FPGA. More specifically, it presents the theoretical support of how to map linear and nonlinear circuit components to WDF. The detail implementation of each WDF component in FPGA is not elaborated due to the page limit. Experiments show that there is a virtually perfect match between FPGA emulation and HSPICE simulations on two small but representative analog circuits, indicating high accuracy of the proposed emulation, and the FPGA-based WDF emulation can process analog signal sampled at as high as 512KHz, which is adequate for a variety of biomedical sensing applications.**

I. Introduction

Analog/Mixed-Signal (AMS) components such as I/O circuits, PLLs and DLLs are key bottlenecks with growing importance in today's advanced process technologies (32nm and below). Moreover, an increasingly significant proportion of overall design bugs are now attributable to on-chip AMS components [1]. However, the design cycle of AMS circuit is prohibitively long because of iterative phase of design, simulation, fabrication, and verification.

Unlike well accepted FPGA emulation for digital circuits, AMS circuit can only be simulated before tapeout [2], [3], [4], and there is no winning solution for emulation of AMS circuits. Existing AMS emulation research includes Field Programmable Analog Arrays (FPAAs) [5], [6], [7] and Programmable ANalog Device Array (PANDA) [8]. Analog macros of FPAA include switched capacitor circuits [9], operational and transconductance amplifiers [6], and mega-modules such as ADCs, DACs, track and hold circuits [7]. Whereas, these FPAAs still do not provide sufficient versatility because of the limited type and number of primitive building blocks [8]. PANDA offers more functional versatility by providing transistor-level programmability [8].

However, in both FPAAs and PANDA, the analog building blocks and interconnections inevitably introduce undesired parasitics (and in turn, loss of accuracy) to the emulation circuit. Therefore they cannot perform accurate emulation which is necessary for AMS circuits. Both FPAAs and PANDA need special hardware supports, such as analog macros, which are not available in existing commercial products.

In this paper, we apply the theory of wave digital filter (WDF) to analog circuit emulation. The WDF theory was originally developed for designing digital filters with low sensitivity to coefficient quantization [10], [11]. Any linear analog continuous time circuit can be mapped to a sampled digital equivalent while preserving circuit topology. They employ incident and reflected wave signals rather than voltages and currents to render the realizable digital equivalent circuit. We will show that both linear components (R, L, C, etc.) and nonlinear components (e.g. transistors) in AMS circuits can be mapped to their WDF equivalent, and these WDF modules can form a WDF equivalent of the AMS circuit. Therefore, the digital implementations of WDF modules immediately lead to an accurate emulation for the original AMS circuits. We call the resulting emulation as Wave digital filter based Analog Circuit Emulation, in short, WaveACE.

To the best of our knowledge, this paper presents the first in-depth study of WDF emulation for the AMS circuit using FPGA. We develop both software and hardware platform, which obtain an optimal WDF implementation based on the original circuit netlist, and implements WDFs in FPGA to form a reconfigurable emulation hardware platform with high speed and small area. This is the primary contribution of this paper.

More specifically, while it is known how to map linear circuit components to WDFs [10], [12], we present the emulation of nonlinear transistor with linearized WDFs and a nonlinear lookup table (LUT). The implementation and optimization of these WDFs in FPGA are non-trivial, but we cannot elaborate them in this paper given the page limit. Instead, we present the performance and resource consumption of the final FPGA implementation.

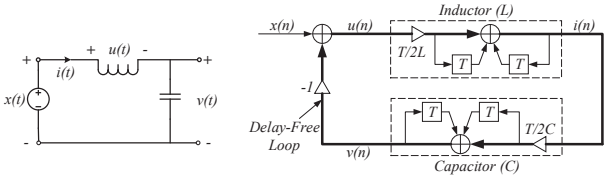
Experiments on two small but representative analog circuits show that there is a perfect match between FPGA emulation and HSPICE simulations, indicating high accuracy of the proposed emulation. The FPGA-based WDF emulation can process analog signal sampled at 512KHz, which is more than adequate for a variety of biomedical sensing applications, such as electrocardiogram (ECG) and Electroencephalogram (EEG) sensing, which typically operate at KHz level or lower [13].

The remaining of this paper is organized as follows. Preliminary knowledge of wave digital filter is covered in Section II. Emulation of linear and nonlinear circuit components are expatiated in Section III. The WaveACE framework and experiment results on a transmission line and a differential amplifier are presented in Section IV. Finally, we conclude this paper in Section V.

II. Preliminaries of WDF

A. Digital Filter Models for RLC Circuits

Conceptually, an analog circuit consisting of linear components (R, L, C, etc.) can be mapped to a digital system through component-by-component digitalization [14]. However, using Kirchoff variables (K-variables in short, including current i and voltage v) makes the resulting digital system have delay-free loops that are not realizable.



(a) Analog LC circuit (b) Digital filter representation

Fig. 1: Component-by-component digitalization of an analog LC circuit

Take the LC circuit in Figure 1(a) as example: the original analog circuit is described by a system of ordinary differential equations (ODEs) as follows,

$$u = L * di/dt \tag{1}$$

$$i = C * dv/dt \tag{2}$$

$$x = u + v \tag{3}$$

where (1) and (2) represent Ohm's Law[1] for L and C, and (3) corresponds to the constraint of Kirchoff Voltage Law (KVL).

This circuit can be digitalized component-by-component by applying trapezoidal rule [15] to the ODE for each component. ODEs for L and C are discretized to difference equations in (4) and (5) respectively,

[1]The Ohm's Law stands for the general Law that applies to R, L, and C, with $V = R_s I$, where R_s equals R, sL, and $1/sC$ for R, L, and C respectively.

while (3) is rewritten as (6).

$$i[n] = i[n-1] + T/2L * (u[n] + u[n-1]) \quad (4)$$
$$v[n] = v[n-1] + T/2C * (i[n] + i[n-1]) \quad (5)$$
$$x[n] = u[n] + v[n] \quad (6)$$

where T is the time step of digitalized system.

Difference equations (4), (5), and (6) do form a digital filter and fully represent the original analog LC circuit. However, it is not realizable due to the presence of a delay-free loop. This is apparent in Figure 1(b), the signal flow representation of these difference equations. Note that the digital modules for both L and C contain direct paths from input to output. When combined together, they form a delay-free loop of combinational components marked as a border line in Figure 1(b).

B. Wave Digital Filter

Wave digital filter [10] was proposed to eliminate the aforementioned delay-free loop. Instead of using the original K-variables, wave variables (W-variables in short) are introduced,

$$\begin{cases} a = v + R_p i \\ b = v - R_p i \end{cases} \quad \text{and} \quad \begin{cases} v = \frac{a+b}{2} \\ i = \frac{a-b}{2R_p} \end{cases} \quad (7)$$

where a and b are incident wave and reflected wave respectively, and R_p is called the port resistance. Each analog component is digitalized as a one-port WDF module, where W-variables a and b are its interface. For each component, the port resistance, R_p, is chosen such that no delay-free path exists from the input to the output.

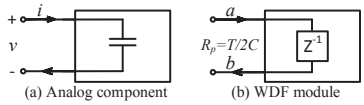


Fig. 2: WDF module for capacitor

Take the capacitor as example, substituting i and v in (5) with a and b leads to

$$\frac{a[n]+b[n]}{2} = \frac{a[n-1]+b[n-1]}{2} + \frac{T}{2C}\left(\frac{a[n]-b[n]}{2R_p} + \frac{a[n-1]-b[n-1]}{2R_p}\right) \quad (8)$$

Choosing $R_p = T/2C$ eliminates $a[n]$ from (8) and results in a simplified equation

$$b[n] = a[n-1] \quad (9)$$

In (9) the output $b[n]$ only depends on the input of the previous cycle. That is equivalent to inserting a delay module and eliminating the direct path in between WDF input $a[n]$ and the output $b[n]$. The WDF module for capacitor behaves as a register as shown in Figure 2, which stores the input $a[n]$ and outputs it at the next time step.

III. WDF-based AMS Circuit Emulation

In this section, we go through the WDF modules for several typical circuit components, and demonstrate how a circuit is emulated using WDF modules in practice. Furthermore, we introduce how a nonlinear transistor is represented using WDF module, and explain it with a simple common source amplifier circuit.

A. Emulating linear circuits

1) Mapping RLC and power sources to WDF modules: WDF modules for linear circuit components are obtained by substituting the K-variables with W-variables and properly choosing port resistance. Several frequently used WDF modules are presented in Figure 3, while a more comprehensive list of WDF modules are available in [10].

Note that, the delay-free path is removed for resistor, inductor, capacitor, and resistive source. However, the voltage source in Figure 3(d) still has a direct path from input to output, but this could be trivially addressed by the reflection-free port in the next subsection.

Furthermore, each WDF module is linked to the original analog circuit component through a bilinear transform [16], which theoretically

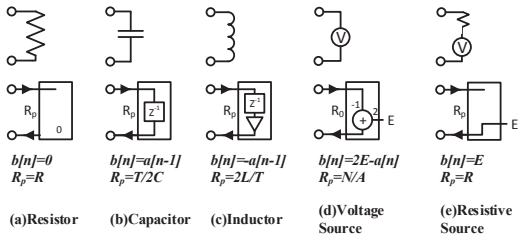


Fig. 3: WDF modules for resistor, capacitor, inductor, resistive source and voltage source

supports the component-by-component mapping. For a analog capacitor, the reflectance is defined as

$$\frac{B}{A} = \frac{V - R_p I}{V + R_p I} = \frac{1 - R_p C s}{1 + R_p C s} = \frac{1 - \frac{T}{2}s}{1 + \frac{T}{2}s} \quad (10)$$

considering Ohm's Law $sCV = I$ and choosing $R_p = T/2C$.

2) Serial and Parallel Adaptors: WDF eliminates the delay-free path in the digital models of analog components. However, they can not be directly connected together because the WDF modules may assume different port resistances. Consequently, adaptors are needed to "equalize" the port resistance.

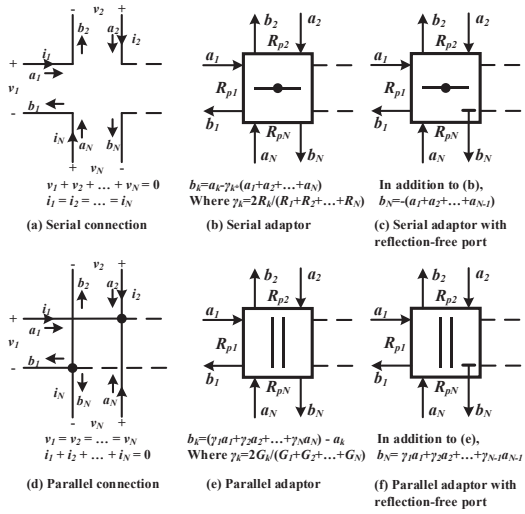


Fig. 4: Serial and parallel adaptors [10]

Another interpretation of adaptors is that they represent the KVL and KCL in the ODEs, while other WDF modules for linear components only represent Ohm's Law. The digital adaptor for serial and parallel connections are presented in Figure 4.

For example, a serial adaptor with N ports can be fully described by KCL and KVL as follows

$$v_1 + v_2 + \cdots + v_N = 0 \quad \text{and} \quad i_1 = i_2 = \cdots = i_N \quad (11)$$

Substituting the K-variables with W-variables leads to

$$b_k = a_k - \gamma_k \textstyle\sum_{n=1}^{N} a_n, \quad \forall k \in \{1, 2, \cdots, N\} \quad (12)$$

where $\gamma_k = 2R_k / \sum_{n=1}^{N} R_n$, and R_n is the port resistance of the n^{th} component serially connected to the adaptor.

The N-port serial adaptor implements these equations using multipliers and adders of appropriate resolution. So, to connect the WDF modules of N analog components in series, an N-port series adaptor is employed with the γ_k coefficients chosen according to the port resistances. Similar equations can be derived for parallel adaptors, which are included in Figure 4(d) and Figure 4(e).

With the WDF of linear circuit components and adaptors, the LC circuit in Figure 1(a) can be converted in WDF modules as shown in Figure 5. In Figure 5, the ideal voltage source is connected to the reflection-free port because it has a delay-free path. The port resistance for L and C are $2L/T$ and $T/2C$ respectively, while the equivalent port resistance of the voltage source is calculated as $2L/T + T/2C$.

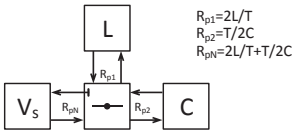
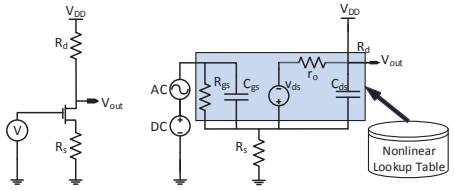


Fig. 5: WDF implementation of the LC circuit

B. Emulating Nonlinear Circuits

Different from linear components, whose I-V behavior can be depicted by Ohm's Law, the I-V behavior of a transistor is nonlinear and more complicated to describe. Most of the existing WDF theory does not deal with nonlinear circuits directly. However, some WDF extensions with special nonlinear transistor models are available [17], [18], [19]. These models are intended for software simulation of WDF and difficult to be implement in hardware such as FPGA.

In this paper, we model the transistor as a linearized equivalent circuit with offline nonlinear lookup table (LUT) that stores the equivalent circuit parameters at different nodal voltage. The LUT is characterized by the HSPICE simulation of a single transistor.



(a) Original circuit (b) linearized equivalent circuit with nonlinear LUT

Fig. 6: Common source amplifier and its its linearized equivalent

As shown in Figure 6(b), R_{gs} and C_{gs} represent the gate resistance and capacitor respectively, while C_{ds} and r_o model the parasitic capacitor and output resistance. A voltage controlled voltage source (VCVS) v_{ds} [2] is used to model the transconductance g_m. During the implementation, R_{gs}, C_{gs}, C_{ds}, g_m, and r_o are looked up from the offline LUT based on the precalculated nodal voltages at operation point, V_g, V_d, and V_s. Dynamic table lookup based on the actual nodal voltage will be implemented in the future.

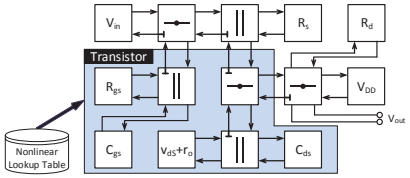


Fig. 7: WDF equivalent of the common source amplifier

Putting this transistor in a common source (CS) amplifier circuit in Figure 6(a), we can get its WDF equivalent as shown in Figure 7. In detail, the circuit can be considered as the serial connection of 3 part, 1) voltage source V_{in}, 2) modules in between gate and source, i.e. R_{gs} and C_{gs}, and 3) the remainder of the circuit. These three parts are connected to a serial adaptor on the top-middle of Figure 7. The WDF modules corresponding to the transistor are highlighted in Figure 7. The amplified voltage can be read out from the serial adapter on the right hand side of Figure 7.

Note that the same circuit may be represented by several different WDFs based on the choice and ordering of the adaptors. During the WDF based emulation, the incident wave from V_{in} has to propagate through all the adaptors until it hits the 1-port modules and reflects back. Since the wave can propagate to multiple branches simultaneously, the emulation speed is only limited by the longest path in the WDF equivalent. Therefore, the achievable emulation speed and emulator hardware requirement depend heavily on adaptor choice.

IV. Experiments

A. Framework of WaveACE

The Framework of WaveACE is illustrated in Figure 8. It consists of an ADC, an DAC, a Voltage-to-Wave (V2W), a Wave-to-Voltage (W2V), and WDF implementation of the original circuit. All the modules except ADC and DAC are implemented in Verilog and mapped to FPGA.

[2]In the implementation, v_{ds} and r_o are modeled as a single WDF module, a voltage source with internal resistance, as shown in Figure 7.

In detail, the HSPICE netlist of an AMS circuit is parsed and automatically converted into FPGA implementation of WDF modules in Verilog. During emulation, instead of using an ADC to sample the analog inputs, we store the digitalized analog signals in a ROM, then load them to the V2W module in each time step. Outputs of WDF implementation are dumped into a file and compared with HSPICE transient simulation results.

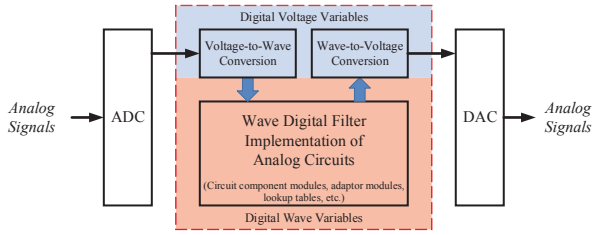


Fig. 8: WDF based Analog Circuit Emulation (WaveACE)

An AMS circuit usually consists of both linear RLC part and nonlinear part. In the following discussion, we validate the WDF based analog circuit emulation on two simple but representative analog circuits: a linear transmission line and a nonlinear 2-stage differential amplifier. The emulation accuracy is verified by comparing outputs of the WDF emulator with HSPICE simulation results of the original analog circuits.

B. Linear Transmission Line Circuit

To demonstrate WaveACE's capability of emulating linear circuit, we implement the WDF equivalent of a lumped RLGC circuit, which is a well-accepted model for transmission line based on Telegrapher's equations [20]. As shown in Figure 9, parameters of each RLGC block can be extracted using existing EM simulation tool. A 50 Ohm matched load is connected to the right hand side of the transmission line, while the power source is also configured with 50 Ohm internal resistance.

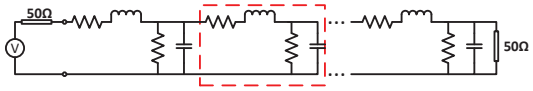


Fig. 9: A transmission line modeled as lumped RLGC circuit based on telegrapher's equations [20]

An interesting observation is that a RLGC block can be viewed as the serial connection of 4 modules if we look into the module from the left hand side. Those 4 modules are input port resistance on the left hand side, R, L, and the parallel connection of all the components on the right hand side. In the meantime, it can be considered as 4 parallel connected modules if it is observed from right hand side. Therefore, each RLGC block can be abstracted as a regular 2-port WDF modules, while the entire lumped RLGC is implemented by cascading multiple RLGC modules as illustrated in Figure 10. Note that all the 4-port adaptor in Figure 10 are implemented using 3-port adaptors in FPGA.

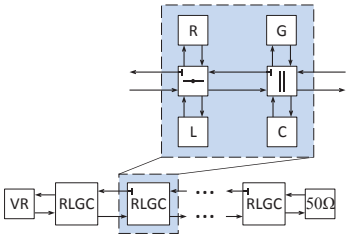


Fig. 10: WDF implementation of the lumped RLGC circuit

A set of random binary signals at the frequency of 1GHz, as shown in Figure 11, are generated and loaded as the input of the WDF module. In Figure 11, we can observe that the WaveACE results totally agree with the HSPICE simulation results.

C. Differential Amplifier Circuit

In this experiment, a two-stage differential amplifier circuit with 7 transistors is used to verify the capability of emulating nonlinear circuits. As shown in Figure 12(a), the first stage, M_3, M_4, is designed to eliminate the noise, while the second stage is used to enhance the gain. Transistors M_1 and M_2 form an active bias to ensure proper

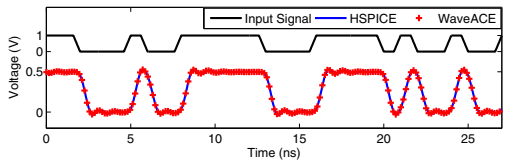


Fig. 11: Comparison between WaveACE and HSPICE transient simulation results

operation region for other transistors. In the bottom of Figure 12(a), M_5 and M_7 work as current sources.

The WDF implementation of this differential amplifier consists of 38 adaptors, including 11 serial adaptors and 27 parallel ones. It is too crowded to show all 38 adaptors here. Instead, we present a simplified WDF implementation in Figure 12(b), where each transistor is considered as a WDF modules. Detail implementation of transistor module is similar to the shaded block in Figure 7.

The WDF implementation of this differential amplifier circuit is verified with a 10MHz sinusoid signal. One of the differential input is configured as 0.9V DC voltage. The other one is a small signal with an amplitude of 1mV imposing on 0.9V bias, which is presented in Figure 13. The amplifier output swings around 0.647V with 30mV amplitude. Perfect accuracy is demonstrated because the emulation results from WDF totally overlap to the transient simulation results of HSPICE in Figure 13. We also configure the WDF implementation at several different frequency points and they again match to the HSPICE simulation results perfectly.

TABLE I: Emulation speed and resource utilization of WaveACE on differential amplifier

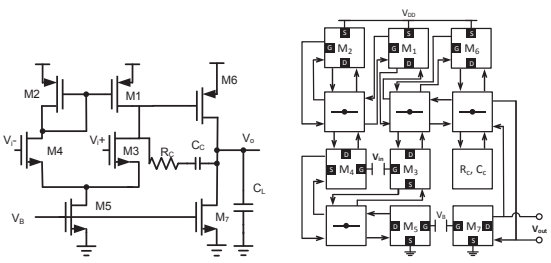
	Speed		Resource			
	clock cycles/step	Max throughput	LUT	Reg	DSP	BRAM
Sequential WaveACE	1482	135KHz	1%	0%	1%	8.5%
Optimal WaveACE	390	512KHz	1%	1%	1%	8.5%

On the other hand, as an emulation platform, we evaluate how fast WaveACE can emulate for this differential amplifier circuit. WaveACE processes input signal at fixed time step. One round of incident and reflect needs to be done in one time step (before the next input sample comes), which determines emulation speed.

We implement the WaveACE on a Xilinx Virtex 7 FPGA, XC7VX690T. The WaveACE can operate at 200MHz after FPGA implementation (while the adaptor modules can operate at 526MHz). The brute-force implementation sequentially traverses 38 adaptors on the adaptor-tree, and takes 1482 FPGA clock cycles to finish one round of incident and reflect (it takes 39 clock cycles to finish the incident and reflect of each adaptor). This poor implementation can only process analog signal sampled at 135.1KHz.

This brute-force implementation is optimized by scheduling the state machine that controlling the adaptors, which will not be discussed in this context. With the optimization, the WaveACE can process analog signal sampled at 511.8KHz, which is significantly better than the brute-force implementation.

We also find that the resource consumption does not increase notably when we get more speedup. First, the required number of DSPs and registers keep almost constant. We do not need to instantiate a large number of adaptors because they are fully pipelined. The input data to those adaptors without mutual data dependency can be streamed to the adaptor instance in adjacent cycles, instead of waiting for the



(a) Original circuit (b) WDF implementation

Fig. 12: A 2-stage differential amplifier circuit and its WDF implementation

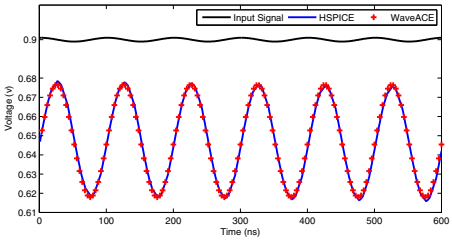


Fig. 13: Transient simulation of the differential amplifier circuit with 10MHz sinusoid input

previous incident or reflect operation to finish. In this example, we create only one instance of parallel and serial adaptor in all three WaveACE implementations. Second, those implementations use the same BRAM size for nonlinear LUTs. It consumes 125 BRAM blocks (25 for each LUT), which is less than 7% of the total number of BRAM blocks in XC7VX690T.

V. Conclusions

This paper presents the first study on an FPGA-based WDF emulation for AMS circuits. We develop both software and hardware platform, which obtains an WDF implementation based on the original circuit netlist, and implements WDFs in FPGA to form a reconfigurable emulation hardware platform. Experiments on two simple but representation circuits show perfect match between the FPGA emulation and HSPICE simulation results. And the FPGA-based WDF emulation can process analog signal sampled at about MHz level, which covers a variety of biomedical sensing applications, which typically sampled at KHz level or lower. Furthermore, good scalability can be expected on emulating larger circuit due to the balanced adaptor-tree architecture.

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