Special Session

Challenges and Opportunities for Low Power FPGAs in Nanometer Technologies

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Summary

Modern field programmable gate array (FPGAs) gains a growing importance due to large capacity, quick time to market and low non-recurring engineering cost. However, FPGA consumes more power than its ASIC (application specific integrated circuit) counterpart. Therefore, modeling and reduction of power for FPGAs has become an emerging research area.

In this session, we will first present an overview of new challenges in commercial FPGA architecture design with an emphasis on the circuit and architecture issues for power at current and upcoming process nodes. Today's 90nm FPGAs utilize techniques such as programmable shut-down of unused resources at the architectural level and multiple threshold voltages and gate-oxides at the circuit level. At 65nm and 45nm new techniques will need to target not only power mitigation but process variation in power and timing and their impact on yield and manufacturability.

Then, we will focus on power-reduction computer-aided design (CAD) techniques for standard FPGAs (with no architectural enhancements for power). We will start by discussing a typical FPGA CAD flow that is not power-aware. Then, we will study each of the four CAD steps (technology mapping, clustering, placement, and routing) and show how each CAD step can be enhanced to optimize the resulting implementation for power. For each step, we will describe both the techniques employed and present experimental results that show how well the techniques are able to optimize for power. We will first consider each stage in isolation, and then present combined results that give an indication of what sort of power savings are possible by optimizing the entire CAD flow.

Finally, we will describe new architecture research and related CAD enhancement in power control, and discuss similar and unique aspects of power reduction in FPGA compared to ASIC. We will first introduce power modeling (both simulation and measurement) and architecture evaluation for FPGA. We will then discuss a number of power reduction techniques such as region-based placement for power gating, field programmable fine-grained dual-vdd and power gating, and time slack allocation for dual-vdd assignment, all involving both architecture and CAD enhancements. We will also perform highly quantitative architecture evaluation considering some of these techniques. Moreover, we will describe device and architecture co-optimization for combined timing and leakage yield rate considering process variations.

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