Robust On-chip Signaling by Staggered and Twisted Bundle

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[1]***Abstract*-Existing shield insertion for multiple signal nets may lead to non-uniformly distributed capacitive coupling-length and inductive returned-path, which introduces large delay and delay variation by crosstalk. This paper discusses the design and test of a twisted and staggered interconnect structure to reduce both inductive and capacitive crosstalk. A transmission line model is introduced and an automatic layout synthesis is presented. Moreover, the proposed design is fabricated in the IBM 0.13um process and tested by an on-chip time-domain sampling circuit. As shown by measured results, our proposed design reduces delay by 25% and reduces delay variation by 25X when compared to designs employing coplanar shields.**

The emergence of chip multiprocessors (CMPs) is becoming the dominant hardware paradigm since the technology-scaling-based uni-processor design would lead to un-manageable power dissipation. On-chip components can be easily shared in CMPs, improving the throughput rate. However, due to the additive effect of improved utilization of components, the increased integration and sharing in a CMP exacerbate soft-errors when delivering signal and clock in the global interconnect. It is already a well-known challenge for Giga-scale integration of uni-processor design to distribute a low-skew and low-jitter (delay variation) global clock and signal in the presence of crosstalk [1-3]. Due to the highly compact integration of interconnect, the adjacent coupling capacitance of global interconnect increases. In addition, the inductance also becomes significant when the slew-rate of the switching signal becomes sharp [4-5]. The crosstalk through capacitive and inductive coupling could severely affect the timing and signal-integrity of clock or signal nets. Since each interconnect experiences a different length of capacitive-coupling or a different return-path of inductive-coupling, it shows a varying clock/signal delay under different switching patterns. As a result, high-speed digital circuits in CMPs that heavily employ the dynamic-logic family are more susceptible to crosstalk compared to circuits that employ the static-logic.

I. Robust On-Chip Signaling

Various techniques have been proposed to improve the robustness of on-chip signaling. Compared to the buffer insertion, planning shields is an effective approach with smaller implementation cost [6-8]. Since the co-planar shielding (called COS) reduces the capacitive-coupling length and provides the local return-path for the inductive-coupling, COS is widely used in current layout design to reduce the crosstalk. An inter-digitized co-planar shielding is introduced in [6] to minimize the self-inductance, and simultaneously shield insertion and net ordering are developed in [7]. In addition, an active shielding method is introduced in [8] by applying complementary signals on shields. The effectiveness of the co-planar shielding is also demonstrated by experiments [9-10]. However, the number of global signal-nets in CMPs is significantly large and hence the use of COS would significantly consume the routing resource of the signal-net. As a result, there is usually only one shield that is shared by many signal nets. This can lead to the delay variation among a group of signal nets. In this paper, the use of multiple signal nets is referred as bundle.

Using via-arrays in copper interconnect with small via resistive loss and improved reliability, another approach of shield distribution twists interconnects together with shields. This approach interleaves the polarity of magnetic flux and hence cancels the inductive coupling. The use of twisted wire is well-known in the wired transmission such as the telephone line and cable. The work in [11] first employs the twisted pair into the differential signaling to reduce crosstalk for DRAM design. Recently, the work in [12] further studies the optimal position of twist for the RC-dominant interconnect. Identical to the use of the COS shielding, where each signal net is designed with its differential net, the use of differential pair would increase the design cost for a bundle of signal nets. The work in [13] introduces a method to distribute shielding for a bundle of signal nets. With the use of both twisted and normal interconnects with shields (called TNS), this approach minimizes the inductive coupling by compensating the polarity-interleaved magnetic fluxes between the twisted group and the normal group. The work in [14] further measures the delay variation of TNS by only twisting shields. However, due to the use of normal interconnects, shields are not uniformly distributed. The capacitive-coupling is therefore still large in between the twisted and normal interconnects and among those inside the group of normal interconnects. As a result, each bit in TNS could have a different capacitive-coupling-length, and hence delays can be still largely varied for signal/clock nets.

This work introduces a twisted and staggered shielding (called TSS) structure to minimize both the inductive and capacitive coupling by uniformly distributing twisted shields. A transmission line model is developed to explain why TSS can reduce both the capacitive and inductive couplings. Furthermore, an automatic layout synthesis is presented for the design of TSS-bundle, which is validated by the SPICE simulation of the worst-case-delay (WCD) and the worst-case-noise (WCN). More importantly, a testing-chip is fabricated to verify the delay and its variations of all these structures under different switching patterns. The measured results show that compared to the COS structure, the TSS structure reduces delay by 25% and reduces delay variation by 25X. When compared to the TNS structure, the TSS

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structure also reduces delay by 7.5% and reduces delay variation by 33X.

II. Twisted Signal and Shield Pairs

Pair of Twisted and Normal Wire

As shown in Fig. 1, a twisted pair means that each signal has a shield as the local ground. Moreover, the aggressor is a normal interconnect with a shield and the victim is twisted together with another shield. Note that due to the symmetry, the victim and its shield see an equal coupling in the twisted pair.

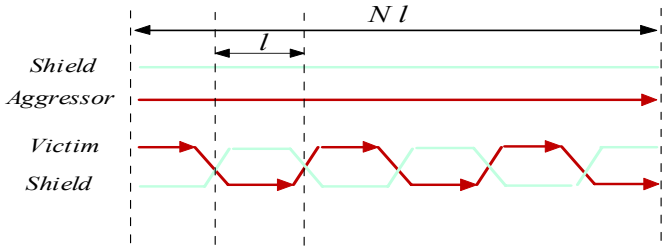

Figure 1. A typical twisted pair signaling with N(6) segments and 5- stages of twists.

The wire is divided into an N-segment with (N-1)-stage. Each segment has a unit length l. To analyze the crosstalk, the aggressor is modeled by the voltage source V_{Asrc} with the source/load impedance Z_{Asrc}/Z_{Ald}, and the victim is modeled by the source/load impedance Z_{Vsrc}/Z_{Vld}. Note that the crosstalk introduced noise at receiver contains two parts: inductive noise V_{ind} and capacitive noise V_{cap}. Below, we derive the induced crosstalk voltage in frequency domain(s).

We first determine the inductive-coupling introduced noise: V_{ind}. As shown in Fig. 2 (a) and (b), we assume that the current at *i-th* stage of the aggressor is I_{Ai}, and the mutual inductance (unit-length) is M_0 between two loops: the one loop composed by the aggressor with its local ground, and the other one composed by the victim with its local ground.

Then the superposed total $V_{induced}$ is

$$V_{induced} = (sM_0 l)(I_{A1} - I_{A2} + I_{A3} - \cdots) \quad (1)$$

where the aggressor current I_{Ai} is approximated by

$$I_{A1} \approx I_{A2} \approx I_A = V_{Asrc} / (Z_{Asrc} + Z_{Ald}) \quad . \quad (2)$$

Since the equivalent model works as a voltage-divider, the inductive noise V_{ind} observed at receiver can be obtained by

$$V_{ind} = \frac{Z_{Vld}}{(Z_{Vld} + Z_{Vsrc})} \times V_{induced} \quad .$$

Based on (1) and (2), V_{ind} becomes

$$V_{ind} = \begin{matrix} if\, N\, is\, even\, , 0 \\ else\, , \end{matrix} \frac{Z_{Vld}}{(Z_{Vld} + Z_{Vsrc})} \times (sM_0 l) I_{A,} \quad . \quad (3)$$

Therefore, when the pair is twisted into an even number of segments, the inductive crosstalk is zero. When the pair is twisted into an odd number of segments, the inductive crosstalk is as small as the coupling of one divided segment with the length (l).

Note that this finding is based on a low frequency analysis, where the current at each twisted stage is approximately the same according to (2). The exact mutual coupling needs to be calculated by the 3D field solver [15] in the high frequency range. As shown by the extraction in Section II, this observation is still approximately valid.

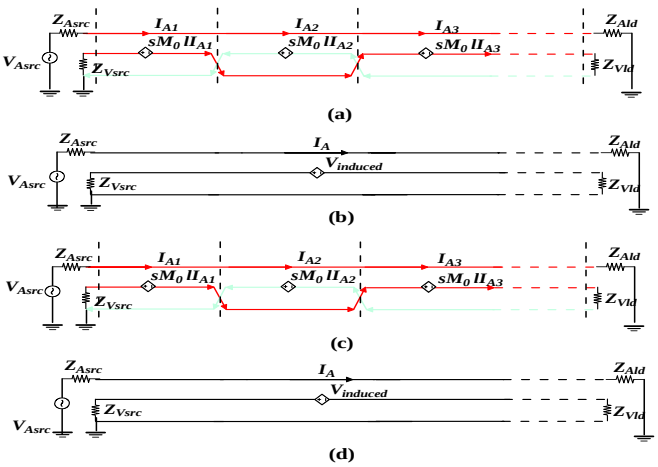

Figure 2. (a) is a detailed crosstalk model and (b) is a simplified equivalent model for inductive crosstalk; (c) is a detailed crosstalk model and (d) is a simplified equivalent model for capacitive crosstalk.

We can further determine the capacitive-coupling introduced noise: V_{cap}. As shown in Fig. 2 (c) and (d), we assume that the coupling capacitance (unit-length) is C_0 between the aggressor and victim when there is no shielding. The coupling is $\alpha\ C_0$ when there exists shielding. Note that the factor α reflects the effect of shielding between the aggressor and victim. Its value can be larger than 1.0 and depends on switching patterns of the aggressor and victim.

Then we have a superposed total $I_{induced}$ by

$$I_{induced} = (sC_0 l)(V_{A1} + \alpha V_{A2} + V_{A3} + \cdots) \quad (4)$$

with the aggressor voltage V_{Ai} at each stage as

$$V_{A1} \approx V_{A2} \approx V_A = \frac{Z_{Ald}}{(Z_{Asrc} + Z_{Ald})} V_{Asrc} \quad (5)$$

The capacitive crosstalk V_{cap} observed at the receiver becomes

$$V_{cap} = Z_{Vsrc} \times (0.5\, sC_0 Nl)(1 + \alpha) V_A \quad (6)$$

where Nl is a constant, the interconnect length. Clearly, for the twisted pair, the capacitive coupling contributes to the dominant crosstalk and there is a difference by a factor N compared to the inductive crosstalk.

Therefore, in the TNS design [13], the two signals experience the capacitive coupling (with no shield inside) in a range that is half of the interconnect length. This situation becomes even more severe when there are more signal nets sharing with one shield, i.e., the structure of twisted bundle. Therefore, the application of TSS is limited if no proper treatment is applied to reduce the capacitive-coupling.

Pair of Twisted and Staggered Wire

We find that the above situation can actually be alleviated by staggering twists as shown in Fig. 3 (b), where shields are alternatively routed between the signals.

Let the number of staggering be N_{stag}. It is easy to verify that the capacitive coupling is effectively reduced by a factor of $2N_{stag}$

$$V_{cap} = Z_{Vsrc} \times \left(0.5 sC_0 Nl\right)\left(\frac{1+\alpha}{2N_{stag}}\right) V_A \quad (7)$$

Clearly, when twisted interconnect is managed in a staggered style, the capacitive coupling-length is effectively reduced compared to the twisted and normal interconnect.

Furthermore, when staggered and twisted shields are uniformly distributed, the flux will be compensated for. As a result, the net flux approaches zero as well. In the example Fig. 4 (b) with wire length 4000um, width 1um, and spacing 2um, the loop inductance matrix extracted at 1GHz by FastHenry [15] is

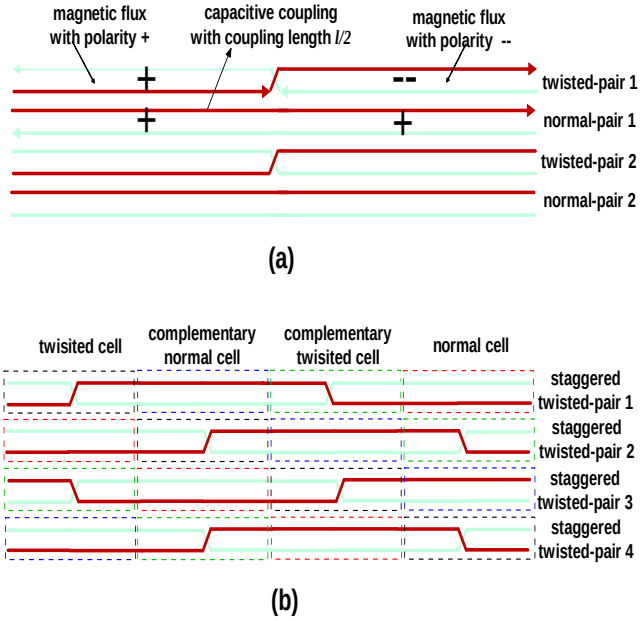

Figure 3. (a) is the twisted and normal interconnect and (b) is the twisted and staggered interconnect.

$$L_{TNS} = \begin{bmatrix} 3.501e\text{-}09 & 4.069e\text{-}14 & 5.159e\text{-}11 & 3.147e\text{-}15 \\ 4.069e\text{-}14 & 3.504e\text{-}09 & 4.069e\text{-}14 & 5.160e\text{-}11 \\ 5.159e\text{-}11 & 4.069e\text{-}14 & 3.501e\text{-}09 & 4.069e\text{-}14 \\ 3.147e\text{-}15 & 5.160e\text{-}11 & 4.069e\text{-}14 & 3.504e\text{-}09 \end{bmatrix}$$

for a twisted pair with normal wires, and the matrix is

$$L_{TSS} = \begin{bmatrix} 3.491e\text{-}09 & 5.796e\text{-}14 & 5.151e\text{-}11 & 4.640e\text{-}15 \\ 5.796e\text{-}14 & 3.491e\text{-}09 & 5.796e\text{-}14 & 5.151e\text{-}11 \\ 5.151e\text{-}11 & 5.796e\text{-}14 & 3.491e\text{-}09 & 5.796e\text{-}14 \\ 4.640e\text{-}15 & 5.151e\text{-}11 & 5.796e\text{-}14 & 3.491e\text{-}09 \end{bmatrix}$$

for a staggered and twisted pair.

Finer discretization (4x4) at each wire cross-section is employed to consider skin and proximity effects. Here, each signal-net and its nearest-neighboring shield compose of a pair, and one end of the signal-net is the port during the extraction. Clearly, the inductive coupling between adjacent groups is also reduced by orders of magnitude for the staggered and twisted pair. Therefore, the design of staggered and twisted and pair can simultaneously reduce capacitive and inductive couplings.

However, it consumes the routing resource to design one shield for each signal-net to form a twisted pair with staggering. Typically we need a shield to be shared among multiple signal nets, i.e., a bundle of interconnect.

III. Synthesis for Staggered and Twisted Bundle

To design a layout for a bundle of signal nets with twisted and staggered shields, we need a systematic synthesis methodology. The problem formulation is summarized below

TSS-Synthesis Problem: Given the number of signal nets N_{sig}, the number of signal/shield ratio N_{cell}, and the number of staggering-stages N_{stag}, the synthesis of staggered and twisted bundle is to find a routing topology with N_{gp} (N_{sig}, / N_{cell}) groups of wires. Each group has N_{stag} stages formulated by connecting a unit twisting-cell (T), a unit normal-cell (N) and their complements (T_b and N_b) alternatively. Then, adjacent groups of wires are generated by cyclically shifting unit cells.

Fig. 3 (b) shows the wire diagram with unit cells for the case of N_{sig}=6, N_{cell}=3, and N_{stag}=1. The definitions of four kinds of unit-cells (*T, N, T_b N_b*) are defined by construction as shown below.

We first discuss how to synthesize a twisting-cell. A twisting-cell consists of N_{cell} signal nets with N_{cell} segments per net. Assuming that each bit of interconnect is equally divided into n (n=N_{cell} + 1) segments, then the twisted pattern is described by a routing matrix T

$$T = \begin{bmatrix} t_{1,1} & t_{1,2} & \cdots & t_{1,n} \\ t_{2,1} & t_{2,2} & \cdots & t_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ t_{n,1} & t_{n,2} & \cdots & t_{n,n} \end{bmatrix} \quad (8)$$

where its *ith*-row is

$$T_i = \begin{bmatrix} t_{i,1} & t_{i,2} & \cdots & t_{i,n} \end{bmatrix}$$

to represent wire segments in *ith*-bit. The changes between each neighboring column represent changes of routing connections. For example, a pair ($t_{k,i}$, $t_{k,j}$) means that the *kth*-bit will change from the *ith-bit* track to the *jth*-bit track.

As shown by Fig. 3 (a), to minimize the inductive crosstalk, we need to twist both the signal and shield segments in a fashion such that the polarity of the current loop for each cell could change symmetrically. In the following, we first discuss how to generate the staggered and twisted pattern for multiple signal nets with one shield.

When n is even, the routing matrix for one unit twisting-cell is synthesized as follows similar to the approach in [13]:

Begin with an initial row T_0=[n-1 n-2 … 1];

Cyclically shift T_0 up by one segment in (n-1) times, obtain (n-1) number of permuted rows and construct a cyclic permutation matrix;

Replace the diagonal element in the cyclic permutation matrix by 0 (representing a shield), attach the diagonal element to an additional column (row) and form an $n \times n$ routing matrix T.

On the other hand, when n is odd, we can apply the same procedure by adding one more dummy wire such that the total wires $(n+1)$ in one unit twisting-cell is still even. This avoids the additional design cost as in [13] to enforce the permeability for odd number of wires.

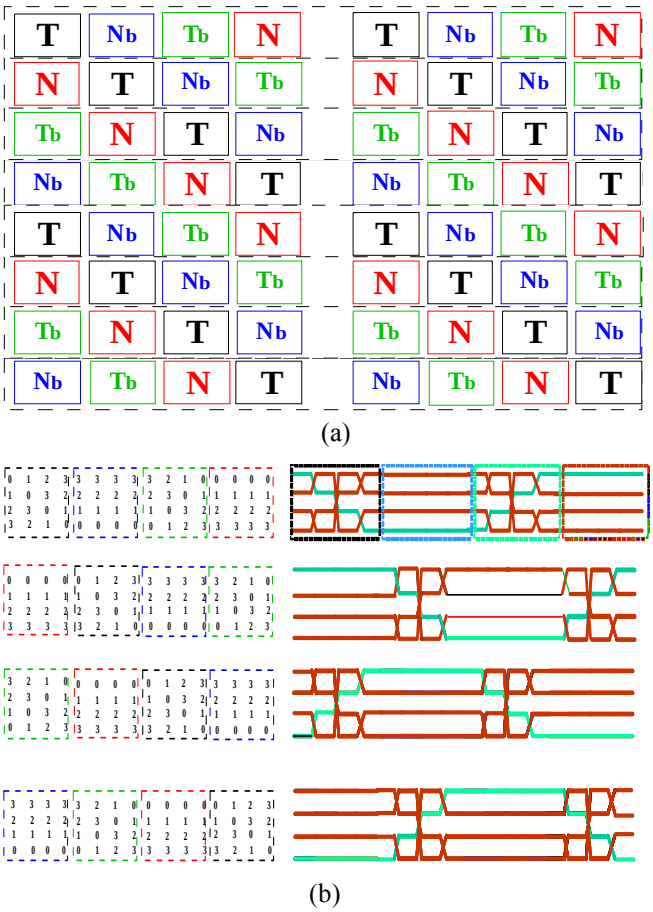

Figure 4. (a) shows how to synthesize the staggered and twisted interconnects using 4 groups of unit cells, and (b) is one example with routing matrix in the left for 3-bit signal nets + 1-bit of shielding net.

For the example in Fig. 3 (b), considering the leftmost cell in the top row, we have the following steps:

T_0 = [3 2 1];

Cyclic permutation matrix:

$$\begin{matrix} 3 & 2 & 1 \\ 1 & 2 & 3 \\ 2 & 3 & 1 \end{matrix}$$

Routing matrix T:

$$\begin{matrix} 0 & 1 & 2 & 3 \\ 1 & 0 & 3 & 2 \\ 2 & 3 & 0 & 1 \\ 3 & 2 & 1 & 0 \end{matrix}$$

Note that we can not synthesize the staggered and twisted bundle by solely using the above constructed twisting-cell. In this paper, we further derive the procedure to synthesize the other three unit-cells. The complementary matrix T_b for the twisting-cell T in (7) is obtained by reversing the order of each row in (8):

$$T_b = \begin{bmatrix} t_{1,n} & t_{1,n-1} & \cdots & t_{1,1} \\ t_{2,n} & t_{2,n-1} & \cdots & t_{2,1} \\ \vdots & \vdots & \ddots & \vdots \\ t_{n,n} & t_{n,n-1} & \cdots & t_{n,1} \end{bmatrix} . \quad (9)$$

Furthermore, we can define a normal-cell (N) and its complementary (N_b) by the following routing matrices accordingly

$$N = \begin{bmatrix} t_{1,1} & t_{1,1} & \cdots & t_{1,1} \\ t_{2,2} & t_{2,2} & \cdots & t_{2,2} \\ \vdots & \vdots & \ddots & \vdots \\ t_{n,n} & t_{n,n} & \cdots & t_{n,n} \end{bmatrix}$$

$$N_b = \begin{bmatrix} t_{n,n} & t_{n,n} & \cdots & t_{n,n} \\ t_{n-1,n-1} & t_{n-1,n-1} & \cdots & t_{n-1,n-1} \\ \vdots & \vdots & \ddots & \vdots \\ t_{1,1} & t_{1,1} & \cdots & t_{1,1} \end{bmatrix} . \quad (10)$$

With use of the above four unit-cells, we can construct the staggered and twisted pattern by interleaving the twisted-cell (T, T_b) and the normal-cell (N, N_b). The according procedure repeats the same synthesis procedure for one twisted-cell.

In details, we first construct an *initial staggered row*:

$$R^0 = [\, T \,//\, N_b \,//\, T_b \,//\, N, \ldots, T \,//\, N_b \,//\, T_b \,//\, N \,]$$

where we repeat the pattern by N_{stag} times. We then cyclically permute R^0 by one unit-cell at a time to obtain the routing matrix for each group as follows:

$$R^1 = P^1 R^0 = [\, N \,//\, T \,//\, N_b \,//\, T_b, \ldots, N \,//\, T \,//\, N_b \,//\, T_b \,]$$

$$R^2 = P^2 R^0 = [\, T_b \,//\, N \,//\, T \,//\, N_b, \ldots, T_b \,//\, N \,//\, T \,//\, N_b \,]$$

$$R^3 = P^3 R^0 = [\, N_b \,//\, T_b N \,//\, T, \ldots, N_b \,//\, T_b \,//\, N \,//\, T \,] .$$

Fig. 4 (a) shows the resulting general structure of the staggered and twisted pattern composed of those unit cells (T, T_b, N, N_b). We further illustrate this procedure in Fig. 4 (b), an example of 18 signal nets with 1-stage staggering. There are 6 groups for synthesis when the signal/shield ratio is 3:1. The routing matrix is shown in Fig. 4 (b) with dash-lines in different styles to indicate different unit cells. The initial staggering row is cyclically permuted 6 times by one cell at a time, and the resulting patterns form the overall routing matrix.

IV. Validation by Circuit Simulation

With the use of above synthesis, we can design more complicated layout for staggered and twisted bundle, and further study the impact of interconnect structure to the worst-case-delay (WCD) and worst-case-noise (WCN).

We use 180nm and 70nm in the Berkeley Predictive Model with copper interconnect. We consider three interconnect structures: the coplanar wire with shielding (COS), the twisted and normal wire with shielding (TNS), and the twisted and staggered wire with shielding (TSS). We assume that M6 is used to layout the signals and shields; the minimum wire width is 0.45um for 180nm, and is 0.2um for 70nm; the spacing is 0.5um for 180nm, and is 0.2um for 70nm. The via is chosen as 2 × 2 array of the minimum size (0.2um×um). The wire length is 4000um, and driver size is about 100X to the minimum inverter size. Note that in our design, the driver strength and interconnect resistive loss are both less than the characteristic impedance of interconnect. Therefore, the inductive effect can not be ignored. Furthermore, an exponential voltage source with 50ps rising time is used as input signals. The non-linear driver is modeled by the Berkeley BSIM3 model within a modified Spice3 [16] simulator. The capacitance is extracted by FastCap [15] with wire discretized into 100 boxes along the length. The resistance and inductance are extracted by FastHenry [15] with an additional 4x4 discretization at cross-section. A distributed RLC circuit is then used to model the signal wire.

Since it is expensive to explore every switching pattern during the design, in this paper, the WCN and WCD are measured based on [4] by keeping the victim line quiet. Note that the study in [5] shows the worst-case noise occurs when the victim line switches in the same direction of neighboring aggressor lines. Moreover, we consider the aggressor and victim having a switching window of 200ps, i.e., the earliest and latest arrival times differ by 200ps. The computational time linearly depends on the number of signal nets and the SPICE simulation time for each alignment. To reduce the simulation time for large circuits, we apply the model order reduction to generate macro-model for interconnects and stamp in the macro-model back for the time-domain analysis.

We compare the WCD/WCN of COS, TNS, and TSS using 6 signal wires with signal/shield ratio 3:1 in the 180nm technology. There are 3 shields used for COS but 2 shields for both TNS and TSS. Fig. 5 compares the WCD and WCN when each wire acts as the victim for all aforementioned three structures. According to Fig. 5 (a), we find that the variation of WCD between signal nets is smaller in TSS than those in COS and TNS. In terms of the average WCD among all 6 bits, TSS has delay 11ps smaller than the COS (51ps vs. 62ps). Moreover, the WCN is shown in Fig. 5 (b). The WCNs of TSS are also uniform among 6 signal nets. Especially for the WCN of TNS, due to the large capacitive coupling among normal wires, the WCNs of signal nets in normal group (net4, net5, net6) are much larger (averaged 15% difference) than those in twisted group (net1, net2, net3). As a result, we can see that TSS structure is optimal in terms of both delay and noise.

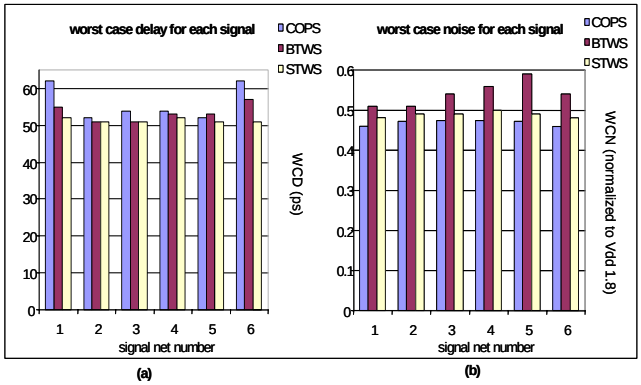

Figure 5. The WCD/WCN comparison for each signal net of COPS/TWB/STWB structures with signal/shield ratio 3:1.

V. Layout and Delay Measurement Circuit

Guided by the simulation from Section IV, we further design the layout and measurement circuit with use of IBM 130nm (8DF-DM) technology with copper interconnect, and fabricate the test chip through MOSIS. The objective of our measurement circuit is to study whether and when inductance becomes important to delay variation, and how interconnect structure affects delay and delay variation.

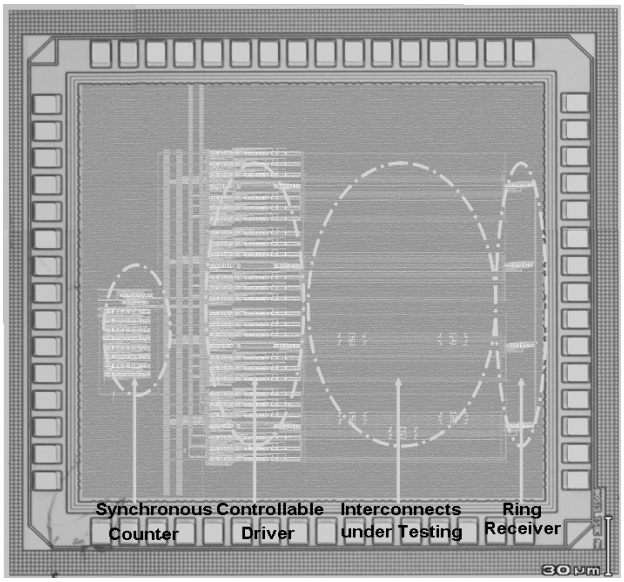

Figure 6. The overall die diagram of the layout and delay measurement circuit.

As shown by the overall die diagram in Fig. 6, our measurement circuit has four components. The first component is the device under test (DUT), i.e., 4 groups of interconnect-structures. The second component is the testing generation module including the programmable driver and delay element, and control-logic to generate different logic pattern. The third component is a ring receiver. It forms an oscillator with the programmable driver by including DUTs in its signal path. The last part is the read-out circuitry. We use a 16 bit synchronized counter to directly record the oscillation frequency of the ring oscillator. We then apply a slow sampling clock to shift out the counted result. As a result, we can infer the delay information of the DUT. As the DUT is

located in the signal paths, the overall operating frequency is achieved around 1GHz.

Layout of Interconnect Structure under Testing

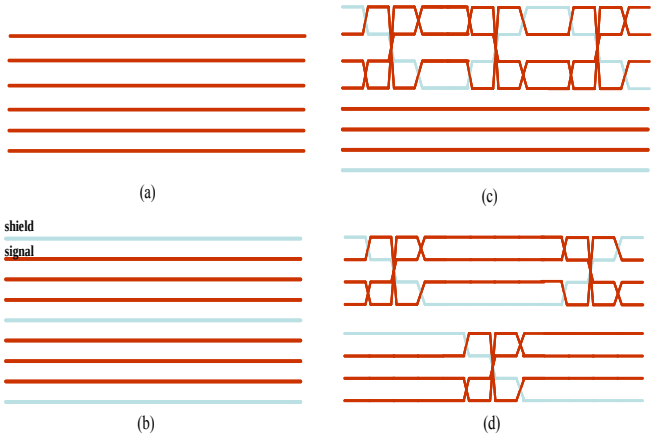

Figure 7. 4 groups of interconnect structures under testing: (a) 6-bit normal interconnects, (b) 6-bit co-planar interconnects with 2-bit shieldings, (c) 6-bit twisted and normal interconnects with 2-bit shieldings, and (d) 6-bit twisted and staggered interconnects with 2-bit shieldings.

In general, the MQ-metal (top) is used for the normal signal net with L=800um, W=4um, S=6um, M3 is used for grounded interconnect (shield), and MG (second top) is used for twisting. Considering the reliability from vias, four 2 x2 via-array are used during connection. As shown in Fig. 7, there are four groups of structures of interconnects under testing. Fig. 7 (a) is 6-bit of normal (NO) interconnects. In this case, the delay variation at each bit is determined by both the return path of inductive coupling and the capacitive coupling length. Moreover, Fig. 7 (b) is 6-bit of coplanar (CO) interconnects with 3-bit of shieldings. There are 6 bits straight signal wires and 3 bits shielding with the same wire length, width and spacing. In this design, there are two groups each with 3 straight signal wires sharing two shielding, and M3 for logic ground. Because there are multiple signals sharing only one shielding, it results in a biased inductive return path, unequal capacitive coupling length, and hence a non-uniform delay variation for the bit in the middle and in the boundary.

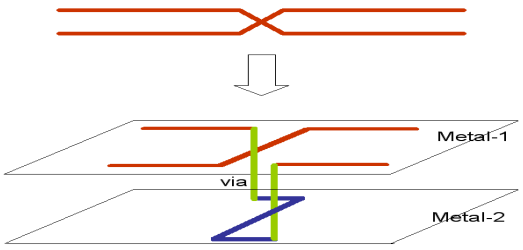

Figure 8. The layout shows how to design a typical twist with use of two layers of metals and via-array.

In addition, Fig. 7 (c) is 6-bit twisted and the normal (TN) interconnects with 2-bit of shieldings. There are 3 bits twisted signal wires, 3 bits straight signal wires and 2 bits shielding. In this case, 1 normal group has 3 straight wires and 1 shielding, and 1 twisted group has 3 twisted wires and 1 shielding, which is also twisted. In addition, MQ is used for signal and shielding wires, MQ and MG are used for twisting wires, and M3 is used for logic ground. Since twisting interweaves the polarity of flux, the twisted group cancels the mutual inductances of the normal group. However, the distribution of shields is still non-uniform in these two groups and hence the delay variations are still significant. Finally, Fig. 7 (d) is 6-bit of twisted and staggered (TS) interconnects with 2-bit of shieldings. In this design, each group is composed of six bits of interconnects. There are two twisted groups, where each group has 3 twisted signal wires and 1 shielding. The same as TN wires, MQ is used for signal and shielding wires, MQ and MG are used for twisting wires, and M3 is used for logic ground. In this design, the shielding is uniformly distributed among 6 bits to minimize both the capacitive and inductive coupling. Note that Fig. 8 further shows how to design a typical twist with use of two layers of metals and via-array.

Test-Generating Circuits

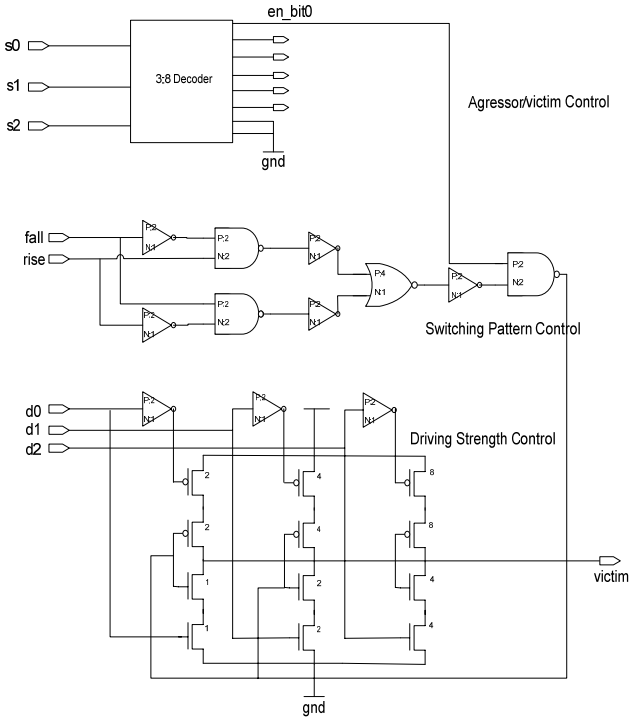

Figure 9. The schematic overview the test-generating circuit.

In this paper, there are three components to generate the test signals: the decoder to select the aggressor and the victim, the control-circuit of switching pattern, and the driver with programmable driving strength. As shown in Fig. 9, we first use the 3:8-decoder to select one bit of victim from other 5 bits of aggressors. Then, each aggressor is enabled to switch from '0->1' (rising) or '1->0' (falling) controlled by a pre-set 1:2-MUX, and the victim is disabled to stay at '0' (quiet). In addition, the driver-strength can be also changed from 1X ~ 8X by selecting 3 drivers in parallel with exponentially increased widths (NMOS W=2.56um,5.12um,10.24um) that will drive the interconnect structure under testing.

Sampling Circuits

In [4], by placing devices under testing in the signal path, a ring-oscillator is used to measure the inductance of interconnect device in frequency domain. As a result, the impedance mismatch and the parasitic from the probe can both affect the accuracy of the measurement. In this paper, similar to [5], the delay measurement is through an on-chip sampling system by including test structures in the signal path of a ring oscillator and using an on-chip counter to record the delays. However, the measured DUT in [14] is of a number of twisted shields with norm wires, a simplified design of [13].

In this paper, there are also three components to sample the delay as shown in Fig. 10. The first component is the ring-oscillator composed by the programmable driver and the receiver, connected into an odd stage of inverter chain with the selected victim in the signal path to be measured. The second component is the 16-bit synchronous counter, used to directly count the output of the ring-oscillator when enabled by an external fast-clock signal. The last component is the shift-register to serially shift out the counter outputs when enabled by another external slow-clock signal.

By setting different input switching pattern for aggressors, the delay is measured at one selected victim bit in the signal path. The delay reflecting the impact from crosstalk can be calculated

$$T_{delay} = \frac{t_{Enable}}{N_{counter}} \qquad (11)$$

Where t_{Enable} is the enable time of the fast-clock and $N_{counter}$ is the counter output shifted by the slow-clock.

Moreover, as this paper is mainly focused on the design of a bundle of signal nets, different from the delay uncertainty defined for a pair of signals [3], the delay uncertainties in this paper are defined as the mean and standard-deviation of measured delays by iterating each bit as the victim from a group of 6-bit lines.

VI. Measurement Results

In the measurement, Tektronix CSA 907A pattern generator is used to generate sampling clock 20MHz, the HP 8130A pulse generator is used to generate control for counter enabling and shifting, and the Agilent 8867 Logic Analyzer is used to measure counter output. The Enabling time for the ring oscillator is 50.5us (with period 90ms), the Reset time is 100ns (with period 90ms), and the sampling clock is 8.15MHz.

Moreover, there are 3 different switching patterns investigated, and the driver strength is selected to be 1X. For the first switching pattern, all 6 bits switch '0->1'. As a result, there is no dynamic capacitive coupling, and the impact of inductive coupling is amplified. For the second switching pattern, two adjacent bits switch in the opposite direction. In this case, the inductive current can return locally by its neighbor and hence the inductive coupling is reduced. However, the dynamic capacitive coupling is magnified due to the Miller effect. Therefore, this case is used to study the impact of capacitive coupling. As for the third case, only one bit in each group switches and all other bits are quiet. Accordingly, a combined inductive and capacitive coupling can be studied. Table 1-3 summarize the results: the counter outputs and extracted delays for three switching patterns. The mean delay and its standard deviation of 6 bits under three switching patterns are calculated for each group in Table 4.

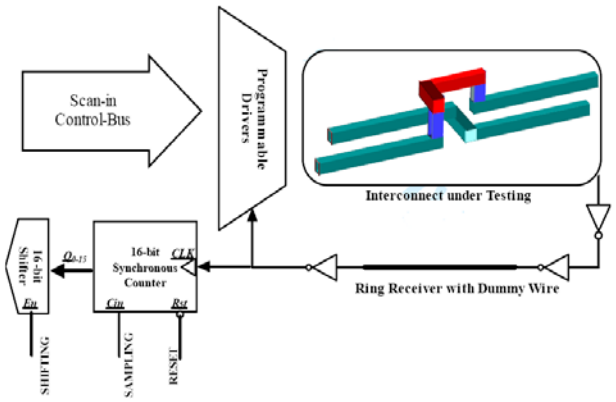

Figure 10. The schematic overview the sampling circuit.

As for switching pattern 1, as shown by Tables 1 and 4, the NO-interconnects have the largest delay variation (0.07ns) among the four groups. The capacitive coupling is minimized because all bits switch in the same direction. Since there are no local shields serving as the return paths, each bit has a different return path and hence a different loop inductance. As a result, the delay of each bit in NO-interconnects has the largest deviation. In contrast, the CO, TN and TS-interconnects provide similar (among different bits) return paths for the inductive coupling. Hence their delay variations are all similar and smaller than that in NO-interconnects. Note that TS-interconnects have the smallest mean delay (0.9ns) and delay variation (1ps).

As for switching pattern 2, as shown by Tables 2 and 4, the CO-interconnects have the largest delay variation (0.06ns) among the four groups. The capacitive coupling is maximized and each bit sees a constant inductive coupling because two adjacent bits switch in the opposite direction. In addition, since the capacitive coupling length is quite different for the bit on the boundary and the bit in the middle, the delay of each bit in CO-interconnects has the largest deviation, larger than that in NO-interconnects. In contrast, as TS-interconnects uniformly distribute the shields among 6 bits to minimize both the capacitive and inductive coupling, they have the smallest delay (0.9ns) and delay variation (3ps).

As for switching pattern 3, as shown by Tables 3 and 4, the TN-interconnect structure has 0.06ns delay variation, while NO-interconnect structure has 0.08ns delay variation. Different from the previous two switching patterns, the delay variation of each bit in this case is determined by both the return path of inductive coupling and the coupling length. Although the TN-interconnect structure provides return paths to minimize the inductive coupling, the capacitive coupling between the twisted and normal groups and inside the normal group is still significant. As a result, the delay of each bit in TN-interconnects has a large deviation (0.06ns), similar to the NO-interconnects (0.08ns). In contrast, both CO-interconnects (0.02ns) and TS-interconnects (3ps) show uniform delay variations. In addition, because TS-interconnects minimize the inductive coupling and also have smaller capacitive coupling length than CO-planar

interconnects, they show the smallest delay (0.9ns). In addition, Table 5 also studies the delays and delay variations under switching pattern 3 but with 8X driving strength. Due to the increased strength, 8X drivers have a higher tolerance of crosstalk than the driver with 1X strength and hence the delay and delay variations are smaller than those for 1X drivers.

Summarizing results of all 3 switching patterns, the TS-interconnect structure reduces delay by 25% and reduces delay variation by 25X compared to the CO-interconnect structure. In addition, the TS-interconnect structure reduces delay by 7.5% and reduces delay variation by 33X compared to the TN-interconnect structure.

VII. CONCLUSIONS

To reduce the delay uncertainty of on-chip signal delivery due to crosstalk, we have demonstrated by both simulation and on-chip measurement of twisted and staggered interconnect to reduce both the capacitive and inductive crosstalk. We first present a transmission line model for the twisted and staggered pair, and an automatic layout-synthesis procedure for the twisted and staggered bundle. We then validate the advantages of our design with the SPICE simulations by studying impacts of the interconnect structure, staggering number and the signal/shield ratio. We further fabricate and measure our design in IBM 0.13um process with an on-chip time-domain sampling circuit to measure delay and its variation under a variety of switching-patterns and driving strengths. As shown by the measurement, our proposed twisted and staggered interconnect reduces delay by 25% and reduces delay variation by 25X compared to the coplanar interconnect with shields, and reduces delay by 7.5% and delay variation by 33X compared to the twisted and normal interconnect with shields.

The staggered and twisted signaling has the fabrication challenge for the application in the multi-level non-global interconnect since it requires an extra metal level to twist the interconnects together. However, because most of global interconnects such as data buses and clocks are usually designed with the top level metals, the application of our proposed interconnect structure seems still promising for the intra-chip and inter-chip communication with a large number of signal or clock nets. This is ideal for the data communication in the design of multi-core CPUs. To fully utilize the proposed interconnect structure in the high-performance design, more detailed studies are needed. For example, it is unknown how to optimally insert buffers for this kind of interconnect. In addition, future study is needed to design a testing-chip with all interconnect structures and to test the delay variation impacted by the process.

ACKNOWLEDGEMENT This work is sponsored by SRC-1100 and NSF-0093273. The authors would like to thank Yiyu Shi and Xinyi Zhang for the work of PCB design, Wei Yao for the work of taking photo of the die, and Prof. Frank M.F. Chang for providing and setting up the measurement equipment.

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	Bit0	**Bit1**	**Bit2**	**Bit3**	**Bit4**	**Bit5**
NO	1.1067e-009s	9.2942e-010s	9.8144e-010s	9.4500e-010s	1.0103e-009s	1.1036e-009s
CO	9.3382e-010s	9.1012e-010s	8.9061e-010s	8.8264e-010s	9.1434e-010s	9.3938e-010s
TN	8.9262e-010s	9.2506e-010s	8.5490e-010s	9.2182e-010s	9.4614e-010s	9.3715e-010s
TS	8.7870e-010s	8.7773e-010s	8.7870e-010s	8.7773e-010s	8.7675e-010s	8.76E-001

Table 1. Measured counter outputs and delays of 6 bits by switching pattern

	Bit0	**Bit1**	**Bit2**	**Bit3**	**Bit4**	**Bit5**
NO	1.0577e-009s	1.1193e-009s	1.0116e-009s	1.0208e-009s	1.1129e-009s	1.0129e-009s
CO	1.1129e-009s	1.0026e-009	1.0410e-009s	1.0301e-009s	1.1098e-009s	9.7658e-010s
TN	9.2724e-010s	9.0594e-010s	9.1753e-010s	9.5762e-010s	9.2833e-010s	1.0026e-009s
TS	8.7481e-010s	8.7384e-010s	8.7968e-010s	8.7675e-010s	8.7287e-010s	8.7384e-010s

Table 2. Measured counter outputs and delays of 6 bits by switching pattern 2

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5
NO	1.0142e-009s	9.2724e-010s	8.6144e-010s	8.9161e-010s	1.0649e-009s	9.9255e-010s
CO	1.0795e-009s	1.0929e-009s	1.0634e-009s	1.0929e-009s	1.0975e-009s	1.1193e-009s
TN	8.6238e-010s	8.1432e-010s	9.2724e-010s	9.6229e-010s	9.6523e-010s	9.3826e-010s
TS	8.7287e-010s	8.6332e-010s	8.6712e-010s	8.6712e-010s	8.6903e-010s	8.6616e-010s

Table 3. Measured counter outputs and delays of 6 bits by switching pattern 3

	Switching Pattern 1		**Switching Pattern 2**		**Switching Pattern 3**	
	Mean	Std	Mean	Std	Mean	Std
NO	1.0127e-009s	7.6942e-011s	1.0559e-009	4.9629e-011	9.5866e-010	7.8045e-011
CO	9.1182e-010s	2.2601e-011s	1.0455e-009	5.5723e-011	1.0909e-009	1.8678e-011
TN	9.1295e-010s	3.3751e-011s	9.3988e-010	3.5194e-011	9.1162e-010	6.0476e-011
TS	8.7756e-010s	1.1385e-012s	8.7530e-010	2.5177e-012	8.6760e-010	3.1834e-012

Table 4. Extracted mean delays and their variations of by three switching patterns

	Bit0	**Bit1**	**Bit2**	**Bit3**	**Bit4**	**Bit5**
NO	3.2600e-009s	3.1993e-009s	3.1471e-009s	3.1718e-009s	3.2916e-009s	3.2456e-009s
CO	3.3002e-009s	3.3081e-009s	3.2907e-009s	3.3081e-009s	3.3107e-009s	3.3230e-009s
TN	3.1479e-009s	3.1059e-009s	3.1993e-009s	3.2248e-009s	3.2268e-009s	3.2075e-009s
TS	3.1566e-009	3.1487e-009s	3.1519e-009s	3.1519e-009s	3.1535e-009s	3.1511e-009s

Table 5. Measured counter outputs and delays of 6 bits by switching pattern 3 with 8X driver-strength