Modeling and Application of Multi-Port TSV Networks in 3-D IC

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***Abstract*—Through-silicon-via (TSV) enables vertical connectivity between stacked chips or interposer and is a key technology for 3-D integrated circuits (ICs). While arrays of TSVs are needed in 3-D IC, there only exists a frequency-dependent resistance, inductance, conductance and capacitance circuit model for a pair of TSVs with coupling between them. In this paper, we develop a simple yet accurate circuit model for a multiport TSV network (e.g., coupled TSV array) by decomposing the network into a number of TSV pairs and then applying circuit models for each of them. We call the new model a pair-based model for the multiport TSV network. It is first verified against a commercial electromagnetic solver for up to 20 GHz and subsequently employed for a variety of examples for signal and power integrity analysis.**

***Index Terms*—Crosstalk, 3-D integration, modeling, packaging, power delivery, resistance, inductance, conductance and capacitance (RLGC) matrices, through-silicon via (TSV).**

I. Introduction

AS THE traditional CMOS scaling pace gradually slows down, 3-D integration offers another dimension of scaling by means of stacking functional blocks vertically and providing high integration density, fast signal transmission, low power consumption, and heterogeneous integration opportunities in the More-than-Moore era [1], [2]. Through-silicon-via (TSV) has been well regarded as a key component in 3-D integration, connecting chips vertically with shortened electrical delay and providing extremely dense I/O connections. While TSV fabrication technologies have progressed [3], it is vitally important to understand TSV electrical properties accurately and efficiently for 3-D system-performance analysis and subsequent design optimization.

In order to evaluate electrical behavior, including delay, power consumption, signal integrity (SI), and power integrity for 3-D ICs, it is desirable to have a SPICE-compatible equivalent circuit model for TSV networks. One approach is to employ an accurate full-wave numerical simulator. However, this method is slow and memory intensive. Consequently, it is not suitable for large-scale analysis and design optimization. The partial element equivalent circuit (PEEC) model [4], [5] has been widely used in inductance and capacitance extraction tools for planar on-chip traces. In a typical PEEC model, the reference has to be defined at infinity for partial inductance and capacitance [5], [6]. However, when applying the PEEC model to TSV networks, the complex 3-D metal-insulator-semiconductor (MIS) structure of TSV and the lossy silicon substrate make it difficult to find the partial inductance and partial capacitance efficiently.

Instead, an extensive amount of work has been done to model a single signal-ground pair of TSVs analytically [7]–[12]. As in [11] and [12], compact resistance, inductance, conductance and capacitance (RLGC) models for a single pair of TSVs are proposed for a wide frequency range, with consideration of the MOS depletion region effect, the alternating-current conduction and eddy currents in silicon, and the skin effect in TSV metal. Though these two-port TSV pair models are already verified against electrostatic measurements and electromagnetic (EM) simulations, they are no longer valid for any pairs of the TSV in the array structure, as the other surrounding TSVs can affect the distributions of electromagnetic fields. To model multi-port TSV networks, [13] and [14] proposed empirical parasitic models for various TSV array structures by dimensional analysis and curve fitting through EM simulations. These multi-TSV models, however, are only available for a limited number of multi-TSV arrangements and, again, cannot be applied to general multi-port TSV networks.

In this paper, we introduce a comprehensive yet accurate modeling methodology to expand TSV pair models for general multi-port TSV networks based on the proposed pair-based equivalent circuit model. An example of a multi-port TSV network is shown in Fig. 1. In our proposed method, we extend the PEEC method with impedance and admittance between TSV pairs and provide a frequency-dependent SPICE-compatible RLGC equivalent circuit for a multi-port TSV network. Design studies to evaluate crosstalk and power integrity of TSV arrays are also discussed based on our proposed multi-TSV modeling techniques.

II. Preliminary on TSV Modeling

The characteristics of TSV are dependent on its geometrical parameters such as TSV radius (r_{via}), height (H), oxide layer

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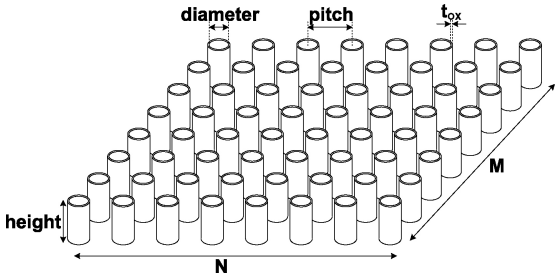

Fig. 1. Multi-port TSV network example: an $M \times N$ TSV array.

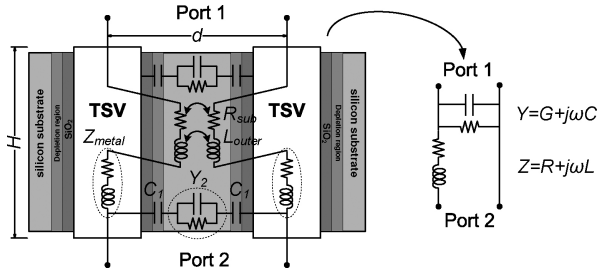

Fig. 2. Structures and dimensional variables of a single TSV pair and its RLGC equivalent circuit model [11].

thickness ($t_{\rm ox}$), center-to-center distance or pitch (d), and electrical parameters such as metal conductivity ($\sigma_{\rm metal}$), oxide permittivity ($\epsilon_{\rm ox}$), and the silicon substrate permittivity (ϵ_{Si}) and conductivity (σ_{Si}).

The conventional PEEC method, first proposed in [4] and [5], could be applied to extract the inductance and the capacitance between each conductor cylinder in TSV networks. The partial inverse capacitance matrices (P_s) and the inductance matrices (L) are defined as

$$P_{s_{ij}} = \frac{1}{A_i A_j} \int_{S_i} \int_{S_j} G_\phi(r, r') ds ds' \tag{1}$$

$$L_{ij} = \frac{1}{a_i a_j} \int_{\Omega_i} dv \int_{\Omega_j} dv' \overline{G_A}(r, r') f_i(r) f_j(r') \tag{2}$$

where A_i, A_j are the total surface areas and S_i, S_j are the surfaces for conductor i and j. Ω_i, Ω_j, a_i, and a_j are the volumes and cross section areas of conductors i and j, respectively. f_i and f_j are the current distribution functions over a_i and a_j. $G_\phi(r, r')$ and $\overline{G_A}(r, r')$ are dyadic Green's functions for electric and magnetic potentials in MIS environments. However, the derivations of dyadic Green's function in inhomogeneous medias are generally difficult problems and are often solved in spectrum domain [15]. The calculations of those Green's functions are time consuming as the numerical integration of the Sommerfeld integrals has to be performed [16].

Instead, an extensive amount of work has been done to model a single signal-ground pair of TSV analytically. In [7], [9], and [10], a parametric and frequency-dependent equivalent circuit model is developed by employing EM simulations. In [8], an MIS structure signal-ground TSV equivalent circuit model is proposed based on TSV physics and closed-form equations. In [11], an equivalent circuit model that considers the width of MIS depletion region for a single TSV pair is proposed. With various models available for a TSV pair, 1-D frequency-dependent RLGC parameters can always be extracted from a two-port network, considering one TSV as the signal and the other as a reference as shown in Fig. 2. These parameters are actually loop impedance and admittance. For example, in [11], the parallel admittance and series impedance for a single TSV pair can be expressed as

$$Z = 2Z_{\rm metal} + j\omega L_{\rm outer} + R_{\rm sub} = R + j\omega L \tag{3}$$

$$Y = [2(j\omega C_1)^{-1} + Y_2^{-1}]^{-1} = G + j\omega C \tag{4}$$

where ω is the radial frequency, and

$$C_1 = \left[\frac{1}{2\pi\epsilon_{\rm ox}} \cdot ln\left(1 + \frac{t_{\rm ox}}{r_{\rm via}}\right) + \frac{1}{2\pi\epsilon_{\rm Si}} \cdot ln\left(1 + \frac{w_{\rm dep}}{r_{\rm via} + t_{ox}}\right) \right]^{-1} \tag{5}$$

$$Y_2 = \pi(\sigma_{Si} + j\omega\epsilon_{Si}) / arccosh(\frac{d}{2} / (r_{\rm via} + t_{\rm ox} + w_{\rm dep})) \tag{6}$$

where $w_{\rm dep}$ is the silicon depletion width

$$Z_{\rm metal} = \frac{(1-j) \cdot J_0((1-j) r_{\rm via} / \delta_{\rm metal})}{\sigma_{\rm metal} \cdot 2\pi r_{\rm via} \delta_{\rm metal} \cdot J_1((1-j) r_{\rm via} / \delta_{\rm metal})} \tag{7}$$

where $\delta_{\rm metal} = \sqrt{2/\omega\mu\sigma_{\rm metal}}$ is the damping parameter for metal and J_0 and J_1 are the 0th order and 1st order Bessel functions of the first type

$$R_{\rm sub} = \frac{\omega\mu}{2} \cdot Re\left[H_0^{(2)}\left(\frac{1-j}{\delta_{Si}} (r_{via} + t_{ox} + w_{dep}) \right) - H_0^{(2)}\left(\frac{(1-j)d}{\delta_{Si}} \right) \right] \tag{8}$$

where $\delta_{Si} = \sqrt{2/\omega\mu(\sigma_{Si} + j\omega\epsilon_{Si})}$ is the damping parameter for silicon substrate. The outer inductance $L_{\rm outer}$ can be approximated by

$$L_{\rm outer} \approx \frac{\mu}{\pi} arccosh(\frac{d}{2r_{\rm via}}). \tag{9}$$

In [12], the outer series impedance $R_{\rm sub}$ and $L_{\rm outer}$ are further improved from a 2-D per-unit-length model to a first-order approximated 3-D model when the TSV height is comparable to the TSV pitch, where

$$R_{\rm sub} \approx \frac{H^4\omega^2\mu^2\sigma_{Si}}{12\pi\sqrt{r_{\rm via}^2 + \frac{169}{400}H^2}} - \frac{H^4\omega^2\mu^2\sigma_{Si}}{12\pi\sqrt{d^2 + \frac{169}{400}H^2}} \tag{10}$$

$$L_{\rm outer} \approx \frac{\mu}{\pi} \cdot \left[r_{\rm via} + H \cdot arcsinh\left(\frac{H}{r_{\rm via}}\right) - \sqrt{r_{\rm via}^2 + H^2} \right] - \frac{\mu}{\pi} \cdot \left[d + H \cdot arcsinh\left(\frac{H}{d}\right) - \sqrt{d^2 + H^2} \right]. \tag{11}$$

The TSV pair model proposed in [11] and [12] is used in the rest of the paper to model each TSV pair in the multi-port TSV network. However, as long as these impedance and admittance between a single TSV pair can be extracted through other modeling techniques, simulation, or even measurement, they can directly be applied in our techniques for modeling multi-port TSV networks.

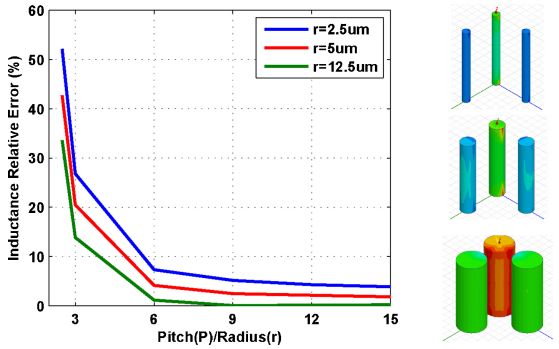

Fig. 3. Charge distribution and the inductance comparison of a 3-TSV network show the proximity effect can be neglected when TSV pitch is larger than 6× TSV radius. The equivalent inductance is calculated at 20 GHz based on our methodology and the TSV pair model in [12]. The results are compared to Ansoft Q3D [17] with various TSV radius and pitch/radius ratios.

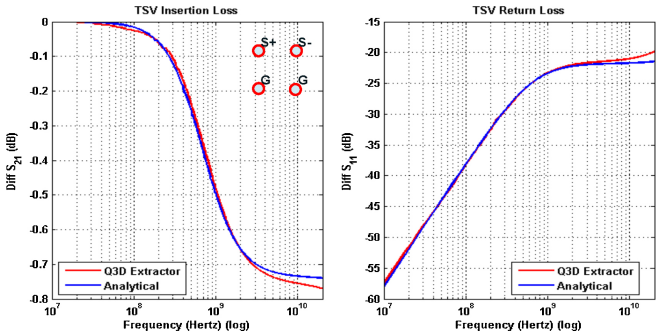

Fig. 4. 2×2 TSV differential pair differential S-parameter comparison. The TSV diameter is 25 μm and pitch is 150 μm.

III. Multi-Port TSV Network Modeling

A. Framework Overview

In this section, we propose a detailed procedure to reconstruct $S \times S$ RLGC matrices for N TSVs with S signals and $(N - S)$ ground TSVs. First, the potential matrix can be expressed as the inverse of the capacitance matrix [5] and, for a TSV pair with two individual conductors

$$P_s = \begin{bmatrix} P_{s_{11}} & P_{s_{12}} \\ P_{s_{12}} & P_{s_{11}} \end{bmatrix} = \begin{bmatrix} C_{11} + C_{12} & -C_{12} \\ -C_{12} & C_{11} + C_{12} \end{bmatrix}^{-1} \quad (12)$$

where C_{11} and C_{12} are the partial self and mutual capacitances defined when the reference is set to be at infinity. For simplicity, we assume all the TSVs in the network are identical. The pair-based capacitance C_p is defined as the capacitance between two TSVs, with one TSV as the signal and the other one as the reference, and can be expressed as

$$C_p = C_{12} + (C_{11}^{-1} + C_{11}^{-1})^{-1} = \frac{1}{2(P_{s_{11}} - P_{s_{12}})}. \quad (13)$$

In a multi-TSV network, as long as the charges uniformly distribute along the surface of the TSV conductor,[1] the self terms $P_{s_{ii}}$, $P_{s_{jj}}$ and mutual terms $P_{s_{ij}}$ of two TSVs are *solely* determined by the media and the geometry of TSV i and j themselves [5]. Thus, the partial potential matrix for a general N-TSV network can be expressed as

$$P_s = \begin{bmatrix} P_{s_{11}} & P_{s_{11}} - \frac{1}{2C_{p_{12}}} & \cdots & P_{s_{11}} - \frac{1}{2C_{p_{1N}}} \\ \vdots & \vdots & \ddots & \vdots \\ P_{s_{11}} - \frac{1}{2C_{pN1}} & P_{s_{11}} - \frac{1}{2C_{pN2}} & \cdots & P_{s_{11}} \end{bmatrix} \quad (14)$$

where $C_{p_{ij}}$ is the pair-based capacitance of a TSV pair between TSV i and j, which can be obtained using (4), and $P_{s_{11}}$ is the inverse of partial self capacitance for a single TSV. We again assume all the TSVs in the network are identical. To obtain the inverse of the conductance matrix, G^{-1}, for a general N-TSV network, the procedure is the same as the P_s matrix.

A similar procedure can also be applied to construct the inductance matrix L and resistance matrix R of an N-TSV network. Taking inductance as an example, the inductance matrix L for two TSV conductors can be expressed as

$$L = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{11} \end{bmatrix} = \begin{bmatrix} L_{11} & L_{11} - \frac{1}{2}L_p \\ L_{11} - \frac{1}{2}L_p & L_{11} \end{bmatrix} \quad (15)$$

where L_{11} is the partial self-inductance of a single TSV and L_p is the loop inductance of a TSV pair. Fundamentally, in a multi-conductor system, the self inductance of one conductor is solely decided by the conductor itself, while the mutual inductance of two conductors is solely decided by the two conductors [4], [6]. The full partial inductance matrix for a general N-TSV network can be expressed as

$$L = \begin{bmatrix} L_{11} & L_{11} - \frac{1}{2}L_{p_{12}} & \cdots & L_{11} - \frac{1}{2}L_{p_{1N}} \\ \vdots & \vdots & \ddots & \vdots \\ L_{11} - \frac{1}{2}L_{pN1} & L_{11} - \frac{1}{2}L_{pN2} & \cdots & L_{11} \end{bmatrix} \quad (16)$$

where $L_{p_{ij}}$ is the loop inductance between TSV i and j. Again, for simplicity, we assume all the self terms are the same and the loop inductance $L_{p_{ij}}$ can be obtained for each TSV pair using (3).

For typical TSV geometry, $C_{p_{ij}}$ and $L_{p_{ij}}$ can be calculated easily, for example, by using (4) and (3). However, it is difficult to analytically calculate $P_{s_{11}}$ (or $1/C_{11}$) and L_{11} for a long cylinder with inhomogeneous media. Note the reference for the full potential matrix P_s and the return path for the full inductance matrix L are set to be at infinity. In reality, however, ground TSVs are designed to be the return path and reference of the high-speed signals. In Section III-B, it can be proven that the reduced potential matrix P_{s_r} and the reduced inductance matrix L_r are independent of the values of $P_{s_{11}}$ and L_{11} if at least one of the TSVs is set as the reference of the network. Thus, we could simply choose both $P_{s_{11}}$ and L_{11} as 0 to simplify our procedure. Physically, this means that the relative potential difference between any two TSVs is independent to the selection of the reference point.

To get the reduced inductance matrix L_r and the reduced potential matrix P_{s_r} for an N-TSV network with $(N - S)$

[1]The charges in TSV are uniformly distributed as long as the center-to-center distance between TSVs is more than 6× TSV radius such that the proximity effect can be neglected. A 3-TSV network example includes one signal TSV and two ground TSV, as shown in Fig. 3. When the TSV pitch is larger than 6X TSV radius, the inductance error is saturated and the proximity effect can be neglected. When the TSV pitch is less than 6X TSV radius, the inductance error rises up dramatically due to the nonuniform current distribution on each TSV.

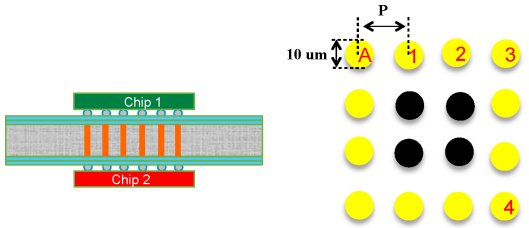

Fig. 5. TSV networks in silicon interposer for 2.5-D chip-to-chip communication.

reference TSVs, we need to connect those reference TSVs in parallel and set them as the current return path for the S signal TSVs. Take a 3-TSV network with the full inductance matrix L as an example. Since $V = j\omega L \cdot I$, then $\frac{1}{j\omega} L^{-1} \cdot V = I$, or equivalently

$$\frac{1}{j\omega} \begin{bmatrix} (L^{-1})_{11} & (L^{-1})_{12} & (L^{-1})_{13} \\ (L^{-1})_{21} & (L^{-1})_{22} & (L^{-1})_{23} \\ (L^{-1})_{31} & (L^{-1})_{32} & (L^{-1})_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}. \tag{17}$$

Assume TSV_1 is the only signal TSV and both TSV_2 and TSV_3 are reference TSVs. After connecting them in parallel and setting $V_2 = V_3$, the reduced inductance matrix L_1 should satisfy

$$\frac{1}{j\omega} L_1^{-1} \begin{bmatrix} V_1 \\ V_2 (= V_3) \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 + I_3 \end{bmatrix} \tag{18}$$

with L_1^{-1} expressed as

$$\begin{bmatrix} (L^{-1})_{11} & (L^{-1})_{12} + (L^{-1})_{13} \\ (L^{-1})_{21} + (L^{-1})_{31} & (L^{-1})_{22} + (L^{-1})_{23} + (L^{-1})_{32} + (L^{-1})_{33} \end{bmatrix} \tag{19}$$

or equivalently

$$L_1 = (A(L^{-1})A')^{-1}, \quad \text{where} \quad A = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}. \tag{20}$$

We now set these parallel-connected reference TSVs as the current return path, which means

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = j\omega L_1 \begin{bmatrix} I_1 \\ -I_1 \end{bmatrix} \tag{21}$$

and the resulting reduced impedance matrix L_r satisfies

$$(V1 - V2) = j\omega L_r \cdot I_1 \tag{22}$$

where $I_1 = -I_2 - I_3$. As a result, L_r can be expressed as

$$\begin{aligned} L_r \;=\; & (L^{-1})_{11} \\ & -((L^{-1})_{12} + (L^{-1})_{13}) - ((L^{-1})_{21} + (L^{-1})_{31}) \\ & +((L^{-1})_{22} + (L^{-1})_{23} + (L^{-1})_{32} + (L^{-1})_{33}) \end{aligned} \tag{23}$$

or equivalently

$$L_r = B(L_1)B' = B(AL^{-1}A')^{-1}B' \tag{24}$$

where

$$A = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix} \quad B = \begin{bmatrix} 1 & -1 \end{bmatrix}. \tag{25}$$

This procedure can be generalized to find the reduced impedance matrix Z_r and the reduced admittance matrix Y_r for any N-TSV networks, where S of them are signal TSVs and $(N - S)$ of them are reference TSVs, with

$$Z_r = B(AZ^{-1}A')^{-1}B' \tag{26}$$

$$Y_r = (B(AYA')^{-1}B')^{-1} \tag{27}$$

and

$$A = \left[\begin{array}{c|c} I_{(S+1)} & \begin{matrix} 0 \\ 1_{1\times(N-S-1)} \end{matrix} \end{array} \right] \quad B = \begin{bmatrix} I_S & -1_{S\times 1}. \end{bmatrix}. \tag{28}$$

Note that $S < N$ so that at least one of the TSVs is a reference. A is an $(S+1) \times N$ matrix and B is an $S \times (S+1)$ matrix. Here, we assume that the first S TSVs in the full Z and Y matrix are signal TSVs and the remaining $(N - S)$ TSVs are reference TSVs. If not, it can be rearranged to this form by multiplying Z and Y with permutation matrices. A summary of our proposed modeling methodology can be found in Algorithm 1. The TSV loop impedance and pair-based admittance Z_p and Y_p can be obtained through (3) and (4) or by other TSV pair models as well.

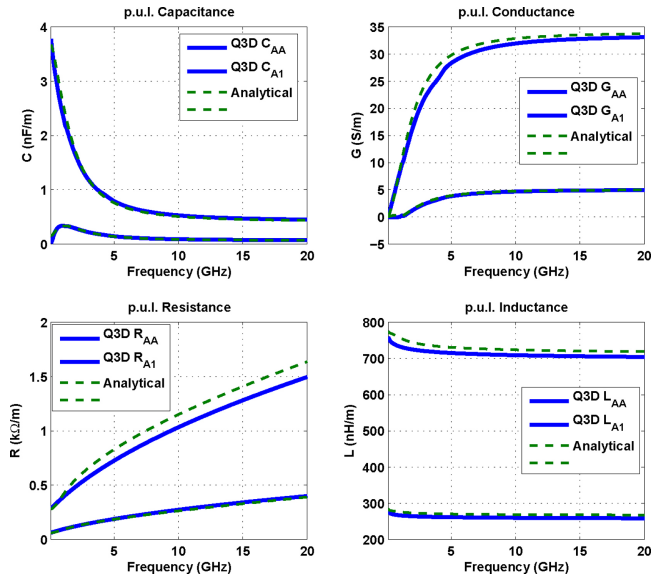

Fig. 6. 4×4 TSV array RLGC comparison for self terms of TSV_A, and mutual terms between TSV_A and TSV_1.

Algorithm 1 Pair-based equivalent circuit method for N-TSV network modeling.

for $i = 1 : N$ **do**
  for $j = 1 : N$ **do**
    if $i \neq j$ **then**
      $Z_{ij} = -\frac{1}{2} Z_p$;
      $(Y^{-1})_{ij} = \frac{-1}{2Y_p}$;
    else
      $Z_{ii} = 0$; $(Y^{-1})_{ii} = 0$;
    end if
  end for
end for
Rearrange Z and Y matrix, if necessary, for reference TSVs;
Prepare matrix A and B according to (28);
$Z_r = B(AZ^{-1}A')^{-1}B'$;
$Y_r = (B(AYA')^{-1}B')^{-1}$

B. Pair-Based Equivalent Circuit Model

In a typical PEEC model, partial inductance and capacitance of a open loop are defined as the integration of the fields to

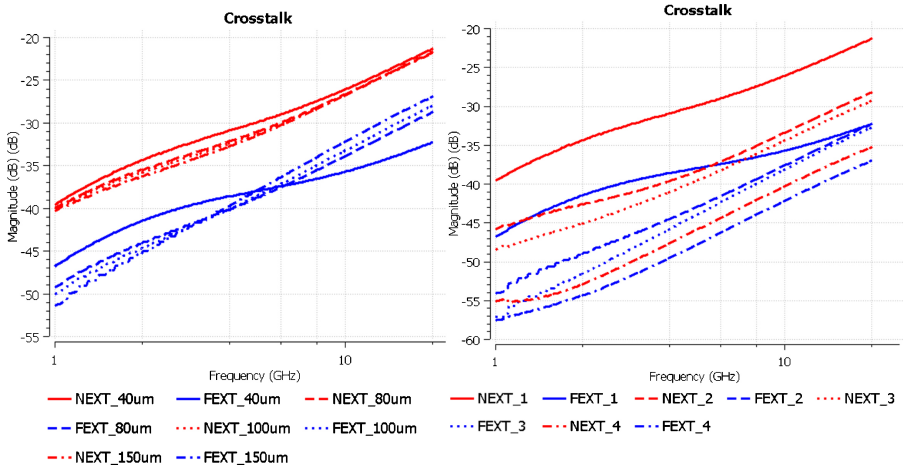

Fig. 7. S parameters of NEXT and FEXT between TSV_A and TSV_1 with different pitch sizes and between TSV_A and other TSVs with pitch 40 μm.

infinity. Computational methods with filament approximation were widely developed [4]–[6] based on the concepts of those partial elements. In some situations, however, when integral-equation based PEEC methods cannot obtain partial elements easily while the loop or pair-based elements among filaments are available through other methods, a numerical scheme as Algorithm 1 can be used to obtain circuit models for these complex structures. The reference needs to be set on at least one or more filaments in the network when applying Algorithm 1. The following derivations demonstrate that the resulting equivalent circuit model for the network is only related to the impedance and admittance between each pair of filaments. The information for the partial self-inductance and self-capacitance with reference at infinity has no effect on the resulting equivalent circuit model. Note in the modeling of a multi-port TSV network, we can simply take each TSV as one filament as long as the proximity effect can be neglected, as shown in Fig. 3.

Without loss of generality, we use impedance matrix Z as an example. For a general N-TSV system, the impedance matrix Z can be expressed as $Z = G + H$ where

$$G = \begin{bmatrix} 0 & -\frac{1}{2}Z_{p_{12}} & \cdots & -\frac{1}{2}Z_{p_{1N}} \\ -\frac{1}{2}Z_{p_{12}} & 0 & \cdots & -\frac{1}{2}Z_{p_{2N}} \\ \vdots & \vdots & \ddots & \vdots \\ -\frac{1}{2}Z_{p_{1N}} & -\frac{1}{2}Z_{p_{2N}} & \cdots & 0 \end{bmatrix} \tag{29}$$

and

$$H = \begin{bmatrix} Z_{11} & \cdots & Z_{11} \\ \vdots & \ddots & \vdots \\ Z_{NN} & \cdots & Z_{NN} \end{bmatrix} \tag{30}$$

where $Z_{p_{ij}}$ is the pair-based impedance between each TSV pair (i, j) and Z_{ii} is the partial self-impedance for TSV i. All the TSVs in the network are identical. Note that G is symmetric and H is of rank 1. We would like to show that the choice of Z_{ii} actually has no impact on the reduced impedance matrix Z_r as long as we set at least one of the TSVs as the reference.

To start with, from (26), we have

$$Z_r = B(AZ^{-1}A')^{-1}B' = B(A(G+H)^{-1}A')^{-1}B' \tag{31}$$

where A and B can be found in (28).

Since G is symmetric and H is of rank 1, by applying a Lemma in [18]

$$\begin{aligned} Z_r &= B(A(G+H)^{-1}A')^{-1}B' \\ &= B(AG^{-1}A' + \frac{-1}{1+g}AG^{-1}HG^{-1}A')^{-1}B' \\ &= B(G_1 + H_1)^{-1}B' \end{aligned} \tag{32}$$

where $g = tr(HG^{-1})$. H_1 is still of rank 1 since $rank(XY) \leq min(rank(X), rank(Y))$ for arbitrary matrices X and Y. The lemma in [18] can be applied again and we get

$$\begin{aligned} Z_r &= B(G_1^{-1} + \frac{-1}{1+g_1}G_1^{-1}H_1G_1^{-1})B' \\ &= B(AG^{-1}A')^{-1}B' + \frac{1}{(1+g)(1+g_1)} \cdot KHK' \end{aligned} \tag{33}$$

where $g_1 = tr(H_1G_1^{-1})$ and $K = B(AG^{-1}A')^{-1}AG^{-1}$.

It can be shown that

$$KHK' = 0 \tag{34}$$

such that

$$Z_r = B(AG^{-1}A')^{-1}B' \tag{35}$$

is not related to H, and so Z_r is not related to the choice of Z_{ii}. The detailed proof can be found in the Appendix.

C. Model Validation via Simulation

From the previous section, it has been shown that by applying our proposed methodology for general multi-port TSV networks, the resulting RLGC models in the reduced impedance (Z_r) and admittance (Y_r) matrices are only related to the equivalent circuit model of each TSV pair within the network. As long as the pair model for each TSV pair is accurate, the resulting multi-port TSV network model is also accurate without the knowledge of partial self elements. To even further verify our method for a multi-port TSV network, a 2×2 TSV array with two signal TSVs and two ground TSVs is first simulated for its differential insertion loss (S21 magnitude) and differential return loss (S11 magnitude) and compared to a commercial EM simulator (Ansoft Q3D [17]), as shown in Fig. 4. The TSV diameter is 25 μm and pitch

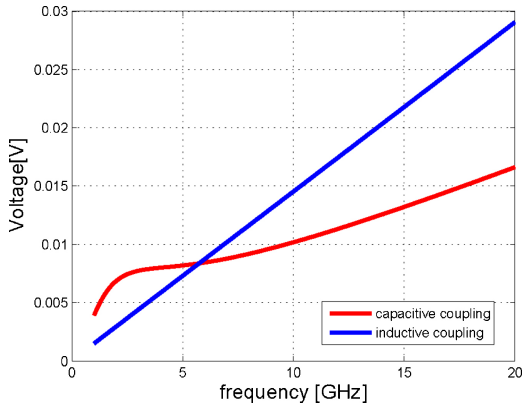

Fig. 8. Normalized crosstalk voltages between TSV_A and TSV_1. The noise voltages are separated to capacitive and inductive couplings using (38) and (39). The pitch size is 40 μm.

is 150 μm. The height of the TSV is 150 μm and the silicon dioxide thickness is 0.5 μm. The resistivity of silicon substrate is 10 Ω·cm. From Fig. 4, it can be shown that our model correlates well with the commercial EM simulator up to 20 GHz for this 2×2 TSV differential network.

Another 4×4 TSV array case with 12 signal TSVs in peripheral and 4 ground TSVs in center, as shown in Fig. 5, is also modeled using our proposed methodology. The reduced impedance and admittance matrices are compared to a commercial EM simulator (Ansoft Q3D [17]) with its extracted RLGC values, as shown in Fig. 6. The TSV diameter is 10 μm and silicon dioxide thickness is 0.5 μm. The height of the TSV is 150 μm and the pitch for this TSV array is 40 μm. The resistivity of silicon substrate is 10 Ω·cm. In Fig. 6, the self-terms (TSV_A) and the mutual terms (between TSV_A and TSV_1) of all the RLGC elements are compared between our method and the extracted results. It can be shown that again our modeling method correlates well with the commercial EM simulator for both self and mutual RLGC values up to 20 GHz.

Note that since in the experiment our methodology is based on an analytical model between each TSV pair without any meshing or other computational electromagnetic procedures, our method could achieve orders of magnitude improvement in terms of efficiency while providing similar accuracy compared to commercial EM simulation tools.

IV. Multi-Port TSV Network Characteristics in Signal and Power Integrity

A. Crosstalk Analysis for Chip-to-Chip TSV Networks in Silicon Interposer

Crosstalk in TSV networks is a critical issue in 3-D integration and may have significant impacts on timing margins and signal integrity, especially for high density TSV arrays on a lossy silicon substrate. Although the TSV arrays can be modeled as a multi-conductor transmission line, the crosstalk among the TSV arrays behaves differently than the crosstalk of transmission lines with homogeneous media.

We first review the near-end crosstalk (NEXT) and far-end crosstalk (FEXT) for electrically short transmission lines by

TABLE I

Mutual Inductance and Capacitance Between TSV_A and TSV_1 at 10 GHz With Different Pitch Sizes

Pitch	40 μm	80μm	100 μm	150 μm
Mutual Inductance (nH/m)	320	350	360	380
Mutual Capacitance (pF/m)	75	50	47	40

the following equations:

$$V_{NE} = \frac{R_{NE}}{R_{NE}+R_{FE}} j\omega L_m I_{ag} + \frac{R_{NE}R_{FE}}{R_{NE}+R_{FE}} j\omega C_m V_{ag} \quad (36)$$

$$V_{FE} = \frac{-R_{NE}}{R_{NE}+R_{FE}} j\omega L_m I_{ag} + \frac{R_{NE}R_{FE}}{R_{NE}+R_{FE}} j\omega C_m V_{ag} \quad (37)$$

where V_{NE} and V_{FE} are the near-end and far-end phasor crosstalk voltages while R_{NE} and R_{FE} are terminations at the near end and far end, respectively. L_m and C_m denote the mutual inductance and capacitance between the aggressor and the victim. V_{ag} and I_{ag} are the aggressor voltage and current, respectively. Equations (36) and (37) assume that the transmission lines are weakly coupled and lossless and the crosstalk can be separated to inductive and capacitive couplings.

TSV structures can usually be considered electrically small and weakly coupled transmission lines below 20 GHz. Thus, the near-end and far-end crosstalks in terms of the S-parameters between TSV i and j can be written as

$$S_{near} = (Z_m/Z_{ref} + Ym \cdot Z_{ref})/2 \quad (38)$$

$$S_{far} = (-Z_m/Z_{ref} + Ym \cdot Z_{ref})/2 \quad (39)$$

where Z_m and Y_m are the mutual impedance and admittance between TSV i and j in the reduced impedance and admittance matrices.

Fig. 5 shows a 4×4 TSV array structure, including 12 peripheral high-speed signal IOs and 4 center ground TSVs. Crosstalk between the aggressor (TSV labeled as A in Fig. 5) and other TSVs is evaluated using our proposed model. The aggressor has 50 Ω terminations at both source and load and all the other TSVs also have 50Ω terminations. Because the TSV array needs to be aligned with package microbumps in this 2.5-D silicon interposer integration, as shown in Fig. 5, the pitch size for each adjacent TSV pair in this array structure has to be identical. Both near-end crosstalk (NEXT) and far-end crosstalk (FEXT) between aggressors TSV_A and TSV_1 with different pitch sizes are illustrated in Fig. 7(a), while the crosstalks between TSV_A and TSV_1, TSV_2, TSV_3, and TSV_4 for a fixed pitch size of 40 μm are shown in Fig. 7(b). First, compared to the crosstalk in ordinary transmission lines with homogeneous media, the frequency responses of total crosstalk transfer functions do not maintain 20 dB/decade. This is mainly due to the transitions of slow mode to TEM mode of semi-conductive media [19], which results in a frequency-dependent mutual capacitance. At low frequencies of the slow-mode region, as shown in Fig. 8, capacitive coupling dominates while inductive coupling dominates at the TEM-mode region.

Interestingly, from Fig. 7(a), it can be observed that the crosstalk cannot be significantly reduced by increasing the

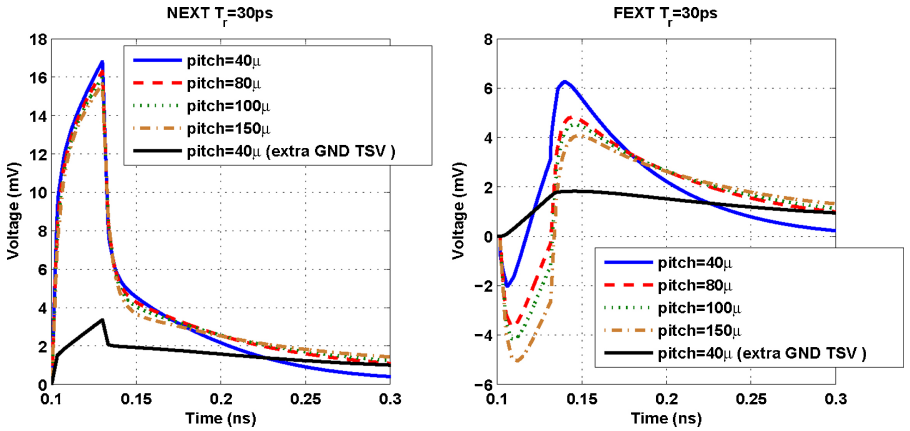

Fig. 9. Time-domain crosstalk voltage at near and far ends between TSV_A and TSV_1, with 1 V signal strength and 30 ps rise time.

pitch size, especially at the high-frequency range. This is because although capacitive coupling decreases as pitch size increases, the mutual inductance between TSV_A and TSV_1 actually increases, as shown in Table I. When increasing the pitch size, not only signal TSVs are further away from each other, ground TSVs are also further away from signal TSVs, which leads to more magnetic couplings between TSV_A and TSV_1. Decreasing TSV pitch hurts NEXT with more capacitive coupling but, on the other hand, benefits FEXT at high frequency where inductive coupling dominates, as shown in Fig. 7(a). From Fig. 7(b), for a fixed pitch size, crosstalk from both inductive and capacitive coupling affects the nearest victim most. This is similar to the crosstalk in ordinary transmission lines.

Fig. 9 shows the time-domain simulations of the crosstalk between TSV_A and TSV_1 with different pitch sizes. The signal has a 1 V voltage swing and the rise time is 30 ps, which corresponds to the knee frequency of 16.7 GHz. The TSVs are terminated at both ends by a 50 Ω resistance. From Fig. 9, for NEXT, the peak-to-peak values of the crosstalk only change slightly with different pitch sizes, as when pitch size increases, inductive coupling increases but capacitive coupling decreases. For FEXT, a deep (inductive coupling) occurs first followed by a pump (capacitive coupling). The deep increases with the pitch size while the pump decreases with the pitch size. Increasing TSV pitch size cannot reduce the crosstalk since inductive coupling is dominant at 16.7 GHz and the peak-to-peak crosstalk voltage actually increases when pitch size is increased. On the other hand, from Fig. 9, it can be shown that adding extra ground TSVs between two signal TSVs is a very effective way to reduce the crosstalk.

B. Impedance Analysis for Power/Ground TSV Array in 3-D Power Distributed Network (PDN)

In order to reduce simultaneous switching noise in a 3-D integration PDN design, the impedance properties of the power/ground (P/G) TSV array must be estimated and analyzed [14]. Fig. 10 shows a system-level PDN with three different P/G TSV array arrangements connecting one of the active die and package. TSV diameter is 10 μm and the pitch is 100 μm. The height of the TSV is 150 μm. The current

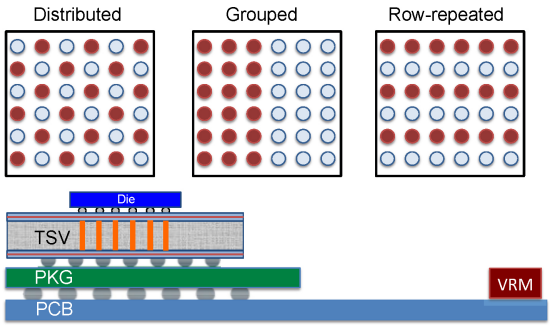

Fig. 10. Power/ground TSV array arrangements and system-level power distribution network (PDN).

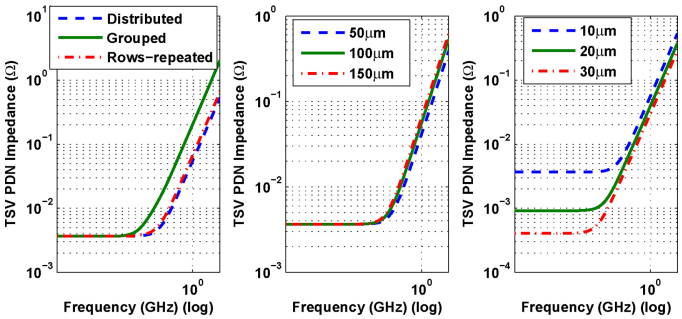

Fig. 11. P/G TSV array impedance versus: (a) different P/G TSV array arrangements, (b) different pitch sizes, and (c) different diameters.

required by the fast switching chip is delivered from the voltage regulation module, through the PCB, package, and TSV P/G networks.

Fig. 11(a) shows the impedance comparison between different array arrangements for a P/G TSV array. In the distributed P/G TSV array, for any particular TSV, all other adjacent TSVs have currents in a reverse direction, which results in reduced mutual inductance and thus smaller impedance at high frequency. The impedance at high frequency for the grouped P/G TSV array is higher than the other two cases because its longer distance between power and ground TSVs results in higher loop inductance. Similar behavior can be found if we increase the pitch in a distributed P/G TSV array, as shown in Fig. 11(b). As pitch increases, the loop inductance

$$\begin{bmatrix} y_{11} & y_{12} & \cdots & y_{1N} \\ y_{21} & y_{22} & \cdots & y_{2N} \\ \vdots & \vdots & \vdots & \vdots \\ y_{(S+1)1} & y_{(S+1)2} & \cdots & y_{(S+1)N} \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & \cdots & y_{1S} & \sum_{i=S+1}^{N} y_{1i} \\ y_{21} & y_{22} & \cdots & y_{2S} & \sum_{i=S+1}^{N} y_{2i} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ y_{(S+1)1} & y_{(S+1)2} & \cdots & y_{(S+1)S} & \sum_{i=S+1}^{N} y_{(S+1)i} \end{bmatrix} \cdot M \tag{41}$$

$$\begin{bmatrix} y_{1(S+1)} & \cdots & y_{1N} \\ y_{2(S+1)} & \cdots & y_{2N} \\ \vdots & \vdots & \vdots \\ y_{(S+1)(S+1)} & \cdots & y_{(S+1)N} \end{bmatrix} = \begin{bmatrix} y_{11} & \cdots & y_{1S} & \sum_{i=S+1}^{N} y_{1i} \\ y_{21} & \cdots & y_{2S} & \sum_{i=S+1}^{N} y_{2i} \\ \vdots & \vdots & \vdots & \vdots \\ y_{(S+1)1} & \cdots & y_{(S+1)S} & \sum_{i=S+1}^{N} y_{(S+1)i} \end{bmatrix} \begin{bmatrix} m_{1(S+1)} & \cdots & m_{1N} \\ m_{2(S+1)} & \cdots & m_{2N} \\ \vdots & \vdots & \vdots \\ m_{(S+1)(S+1)} & \cdots & m_{(S+1)N} \end{bmatrix}. \tag{42}$$

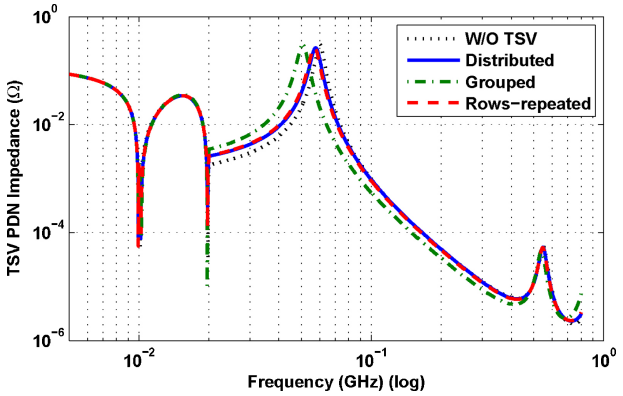

Fig. 12. 3-D PDN impedance comparison between different P/G TSV array arrangements.

increases and so does the high-frequency impedance. For frequencies less than 10 MHz, the impedance is dominated by the resistance of the P/G TSV and is not affected by the array arrangement or the pitch. By increasing the TSV diameter, the resistance of the P/G TSV is decreased and so is the low frequency TSV array impedance, as shown in Fig. 11(c).

By connecting our P/G TSV array model with the extracted package and PCB PDN models, a system-level impedance analysis for 3-D PDN can be performed between different P/G TSV array arrangements and the result is shown in Fig. 12. From the figure, the PDN impedance is still generally dominated by the large off-chip inductance and on-chip capacitance at frequencies below 10 MHz. However, with the grouped P/G TSV array, the PDN peak impedance gets shifted and the impedance between 20 MHZ and 100 MHz increases significantly due to larger inductance introduced by the grouped P/G TSV array.

V. Conclusion

In this paper, we introduced a general pair-based model for multi-port TSV networks. Frequency-dependent RLGC equivalent circuits for multi-port TSV networks can be extracted and composed based on pair-based impedance and admittance from the TSV pair models. The results of our proposed multi-port TSV network modeling were validated against commercial electromagnetic simulations up to 20 GHz. Design guidelines for TSV arrays based on crosstalk analysis and power integrity analysis were also investigated using the proposed modeling technique. The proposed pair-based equivalent circuit model can be generalized and applied to other applications as well.

Appendix

For any nonsingular $N \times N$ matrix X and rank-one $N \times N$ matrix H, it can be shown that

$$KHK' = 0 \tag{40}$$

where $K = B(AXA')^{-1}AX$. A is an $(S+1) \times N$ matrix and B is an $S \times (S+1)$ matrix, which can be found in (28).

To apply to our case, we can simply define H and G by using (30) and let $X = G^{-1}$ since G is symmetric.

Proof: Equation (40) can be proven true by showing that for any nonsingular $N \times N$ matrix X and $K = B(AXA')^{-1}AX$, the sum of each row of K equals zero such that KHK' equals zero for any $N \times N$ rank-1 matrix H.

Equivalently, we want to show $\sum_{j=1}^{N} k_{ij} = 0$ for row $i = 1, 2, \ldots, S$ in K. We first let $Y = AX$ and $M = (YA')^{-1}Y$ such that K can be expressed as

$$K = B(AXA')^{-1}AX = B \cdot (YA')^{-1}Y = B \cdot M. \tag{43}$$

Without loss of generality, we simply assume

$$Y = \begin{bmatrix} y_{11} & y_{12} & \cdots & y_{1N} \\ y_{21} & y_{22} & \cdots & y_{2N} \\ \vdots & \vdots & \vdots & \vdots \\ y_{(S+1)1} & y_{(S+1)2} & \cdots & y_{(S+1)N} \end{bmatrix} \tag{44}$$

with the following equality must be satisfied:

$$Y = (YA')M \tag{45}$$

or equivalently as shown in (41).

As a result, M can be expressed as

$$M = \begin{bmatrix} 1 & 0 & \cdots & 0 & m_{1(S+1)} & \cdots & m_{1N} \\ 0 & 1 & \cdots & 0 & m_{2(S+1)} & \cdots & m_{2N} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \cdots & 1 & m_{S(S+1)} & \cdots & m_{SN} \\ 0 & 0 & \cdots & 0 & m_{(S+1)(S+1)} & \cdots & m_{(S+1)N} \end{bmatrix}$$

where m_{ij} is defined in (42) for $i = 1, 2, \ldots, (S+1)$, $j = (S+1), \ldots, N$.

In other words

$$y_{i(S+j)} = \sum_{k=1}^{S} y_{ik} m_{k(S+j)} + m_{(S+1)(S+j)} \sum_{l=S+1}^{N} y_{il} \tag{46}$$

for $i = 1, 2, \ldots, (S+1)$ and $j = 1, 2, \ldots, (N-S)$, and we can find that the summation for each row i in (42)

$$\sum_{j=1}^{N-S} y_{i(S+j)} \tag{47}$$

$$= \sum_{j=1}^{N-S}\sum_{k=1}^{S} y_{ik} m_{k(S+j)} + \sum_{j=1}^{N-S}\sum_{k=1}^{N-S} y_{i(S+k)} m_{(S+1)(S+j)}$$

$$= \sum_{k=1}^{S} y_{ik}\Big(\sum_{j=1}^{N-S} m_{k(S+j)}\Big) + \sum_{k=1}^{N-S} y_{i(S+k)}\Big(\sum_{j=1}^{N-S} m_{(S+1)(S+j)}\Big)$$

$$= \sum_{k=1}^{S} y_{ik}\,\Sigma_k + \Sigma_{(S+1)} \sum_{k=1}^{N-S} y_{i(S+k)}. \tag{48}$$

From (48), it is clear that

$$\Sigma_k = \begin{cases} 0, & \text{if } k \le S \\ 1, & \text{if } k = S+1 \end{cases} \tag{49}$$

and the sum for any row k in M all equals 1 since

$$\sum_{j=1}^{N} m_{kj} = \begin{cases} 1 + \displaystyle\sum_{j=N-S}^{N} m_{k(S+j)} = 1 + \Sigma_k = 1, & \text{if } k \le S \\ \displaystyle\sum_{j=N-S}^{N} m_{(S+1)(S+j)} = \Sigma_{(S+1)} = 1, & \text{if } k = S+1. \end{cases} \tag{50}$$

Equivalently

$$\sum_{j=1}^{N} m_{ij} = \sum_{j=1}^{N} m_{kj} \quad \text{for} \quad i, k = 1, 2, \ldots, S+1 \tag{51}$$

for any $(S+1) \times N$ matrix Y and $M = (YA')^{-1}Y$.

Since $B = \begin{bmatrix} I_S & -1_{S\times 1} \end{bmatrix}$ and $K = BM$, it can easily be shown that the sum of each row in K equals to zero

$$\sum_{j=1}^{N} k_{ij} = 0 \quad \text{for} \quad i = 1, 2, \ldots, S \tag{52}$$

and KHK' equals zero for any $N \times N$ rank-one matrix H, which proves (40). ■

REFERENCES

[1] K. Banerjee, S. Souri, P. Kapur, and K. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.

[2] K. Bernstein, P. Andry, J. Cann, P. Emma, D. Greenberg, W. Haensch, M. Ignatowski, S. Koester, J. Magerlein, R. Puri, and A. Young, "Interconnects in the third dimension: Design challenges for 3-D ICs," in *Proc. 44th ACM/IEEE Des. Autom. Conf.*, pp. 562–567, Jun. 2007.

[3] K. Powell, S. Burgess, T. Wilby, R. Hyndman, and J. Callahan, "3-D IC process integration challenges and solutions," in *Proc. Int. Interconnect Technol. Conf.*, 2008, pp. 40–42.

[4] A. E. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM J. Res. Develop.*, vol. 16, no. 5, pp. 470–481, 1972.

[5] A. Ruehli and P. Brennan, "Efficient capacitance calculations for three-dimensional multiconductor systems," *Microwave Theory Tech.*, vol. 21, no. 2, pp. 76–82, 1973.

[6] L. He, N. Chang, S. Lin, and O. Nakagawa, "An efficient inductance modeling for on-chip interconnects," in *Proc. IEEE Custom Integr. Circuits*, pp. 457–460, May 1999.

[7] J. S. Pak, C. Ryu, and J. Kim, "Electrical characterization of trough silicon via (TSV) depending on structural and material parameters based on 3-D full wave simulation," in *Proc. Int. Conf. EMAP*, 2007, pp. 1–6.

[8] J. S. Pak, J. Cho, J. Kim, J. Lee, H. Lee, K. Park, and J. Kim, "Slow wave and dielectric quasi-TEM modes of metal-insulator-semiconductor (MIS) structure through silicon via (TSV) in signal propagation and power delivery in 3-D chip package," in *Proc. 60th ECTC*, 2010, pp. 667–672.

[9] L. Cadix, A. Farcy, C. Bermond, C. Fuchs, P. Leduc, M. Rousseau, M. Assous, A. Valentian, J. Roullard, E. Eid, N. Sillon, B. Flechet, and P. Ancey, "Modelling of through silicon via RF performance and impact on signal transmission in 3D- integrated circuits," in *Proc. 3-D Syst. Integr.*, 2009, pp. 1–7.

[10] Z. Xu and J.-Q. Lu, "Through-strata-via (TSV) parasitics and wideband modeling for three-dimensional integration/packaging," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1278–1280, Sep. 2011.

[11] C. Xu, H. Li, R. Suaya, and K. Banerjee, "Compact AC modeling and performance analysis of through-silicon vias in 3-D ICs," *Electron Devices*, vol. 57, no. 12, pp. 3405–3417, 2010.

[12] C. Xu, V. Kourkoulos, R. Suaya, and K. Banerjee, "A fully analytical model for the series impedance of through-silicon vias with consideration of substrate effects and coupling with horizontal interconnects," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3529–3540, Oct. 2011.

[13] K. Salah, H. Ragai, Y. Ismail, and A. E. Rouby, "Equivalent lumped element models for various n-port through silicon vias networks," in *Proc. 16th ASP-DAC*, 2011, pp. 176–183.

[14] J. S. Pak, J. Kim, J. Cho, K. Kim, T. Song, S. Ahn, J. Lee, H. Lee, K. Park, and J. Kim, "PDN impedance modeling and analysis of 3-D TSV IC by using proposed P/G TSV array model based on separated P/G TSV and chip-PDN models," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, no. 2, pp. 208–219, Feb. 2011.

[15] W. Chew, *Waves and Fields in Inhomogenous Media*. New York: Wiley-IEEE Press, 1999.

[16] Y. Chow, J. Yang, D. Fang, and G. E. Howard, "A closed-form spatial Green's function for the thick microstrip substrate," *IEEE Trans. Microw. Theory Tech.*, vol. 39, no. 3, pp. 588–592, Mar. 1991 .

[17] ANSYS, Inc. (NASDAQ:ANSS) [Online]. Available: http://www.ansys.com/

[18] K. S. Miller, "On the inverse of the sum of matrices," *Math. Mag.*, vol. 54, no. 2, pp. 67–72, 1981.

[19] H. Hasegawa, M. Furukawa, H. Yanai, "Properties of microstrip line on Si-SiO2 system," *Microw. Theory Tech.*, vol. 19, no. 11, pp. 869–881, 1971.

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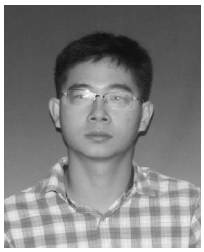

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