# Chip and Package Power Supply Noise Analysis for SoC Design

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<table>
<thead>
<tr>
<th>Year</th>
<th>Gate Length (nm)</th>
<th>Chip Frequency (GHz)</th>
<th>Maximum Power (Watt)</th>
<th>Supply Voltage (Volt)</th>
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<tr>
<td>2001</td>
<td>65</td>
<td>1.7</td>
<td>130</td>
<td>1.1</td>
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<td>2002</td>
<td>53</td>
<td>2.3</td>
<td>140</td>
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<td>2003</td>
<td>45</td>
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<td>2004</td>
<td>37</td>
<td>4.0</td>
<td>160</td>
<td>1.0</td>
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<td>2005</td>
<td>32</td>
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<td>170</td>
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<td>2006</td>
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<td>5.6</td>
<td>180</td>
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<td>2007</td>
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<td>6.7</td>
<td>190</td>
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<td>2010</td>
<td>18</td>
<td>11.5</td>
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<td>2016</td>
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International Technology Roadmap for Semiconductors
Power Supply Noise $\Delta V = IR + L \frac{\Delta I}{\Delta t}$

### Power Supply Noise Issues

- How much is total Vdd drop?
- How much is on-chip IR drop?
- How much is off-chip L $dl/dt$ drop?
- What is the on-chip Vdd distribution?
- Where are the hot spots?
- Which design parameters can be changed to minimize the noise?
- Do we need on-chip decoupling capacitors?
- How much decoupling capacitance is needed?
- Where should the decoupling capacitors be placed?
Package Impedance Frequency Response

No Decap
Off-Chip Decap
On-Chip Decap

0.0 0.2 0.4 0.6 0.8 1.0
0.0
1.0
2.0
Ohm
GHz

1.64V
1.66V
1.68V
1.70V
1.72V

On-Chip Decoupling Capacitor Analysis

Without On-Chip Decap
(1.640V - 1.700V)

With On-Chip Decap
(1.680V - 1.726V)
Power Supply Distribution Model

Off-Chip

On-Chip

Package Model Partition

IBM

Circular Pattern
Package Model Cross Section

Chip Model Partition
On-Chip Power Bus Structure

Equivalent Switching Circuit
On-Chip Decoupling Capacitors

- Built-in decoupling capacitors
  - N-well capacitor
  - Non-switching circuit capacitor
- Added decoupling capacitors
  - Thin-oxide capacitor
  - Trench capacitor

Integrated Model and Design Flow

- Package Model
- On-Chip Power Bus
- Chip Floorplan
- Switching Circuit Model
- Decap Placement

Hierarchical Power Supply Distribution Model

Full-Chip Power Supply Noise Analysis

- Noise Map
- Power Supply Waveform
- Frequency Response

Performance Target

No

Yes
Dual-Chip Power Supply Noise Analysis

1.66V
1.73V
1.80V
1.87V
1.94V

Clock Gating and Its Effect on Transient Power Supply Noise

- A Potential Show Stopper
Transient Noise Analysis

Clock Gating

- C1 off
- Test
- C1 off
- C1 on
- Function
- Max
- C1 off

Power Ramp-Up

- 1/2 C2(A) on
- C2(A) on
- C1(A) on
- C2(B) on
- C1(B) on

Power Ramp-Down

- C1(B) off
- 1/2 C2(B) off
- C2(B) off
- 1/2 C2(A) off
- C1(A) off
- C2(A) off

Hold-to-Maxave Transient Vdd

 transient noise analysis and power ramp-up/down graphs.
Bulk-CMOS and SOI Noise Analysis

With N-Well (Bulk)
(1.718V - 1.767V)

Without N-Well (SOI)
(1.680V - 1.726V)

C4 Current and Electromigration Analysis

100mA
75mA
50mA
25mA
0mA
On-Chip Temperature Gradient Analysis

- Based on thermal fluid dynamics model.
- Use on-chip power distribution as boundary condition.
- 3°C for a 25W chip with uniform power distribution.
- 12°C for a 25W chip with nonuniform power distribution.

Power Supply Noise Analysis Summary

- Build chip and package power distribution model.
- Simulate switching activities and calculate thermal power.
- Control steady-state noise under 10% of nominal Vdd.
- Model circuit transitions from idle power to peak power and evaluate their noise impact.
- Analyze transient noise due to clock gating, power ramp-up, and switching near resonant frequency.
- Optimize on-chip decoupling capacitor placement to minimize power supply noise.
- Balance thin-oxide and thick-oxide decap usage to reduce tunneling current, leakage power, and burn-in cost.