Topological Routing to Maximize Routability for Package Substrate

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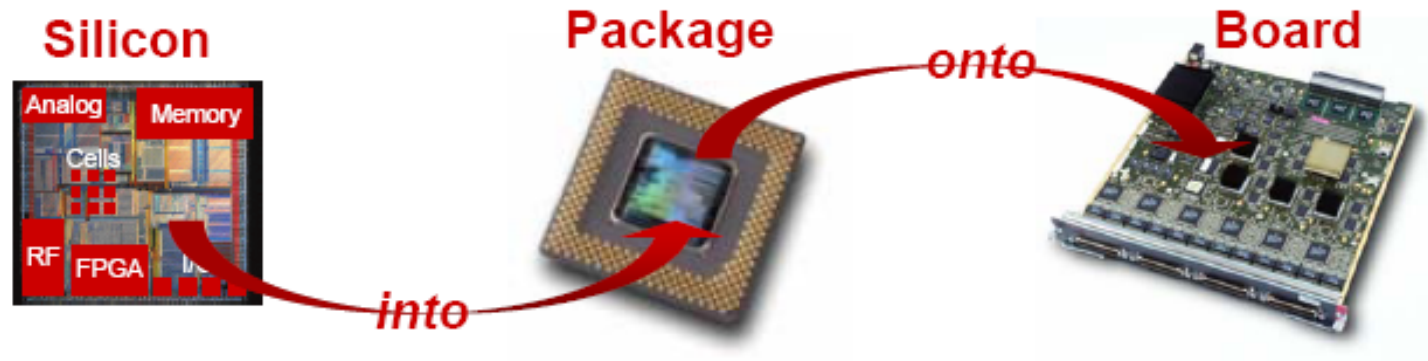Tom Tong Jing, Lei He, Tianpei Zhang,

Robby Dutta, Xian-Long Hong

Outline

- Background

- Existing work

- Problem formulation

- Algorithm

- Experimental results

- Conclusion

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- **Background**

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Package (2)

- **Package substrate**
  - ⊙ PGA (pin grid array)
  - ⊙ BGA (ball grid array)

- **Two techniques to mount the die to the substrate**
  - ⊙ wire bonding, WB
  - ⊙ flip chip, FC

Substrate Routing (1)

- Packaging in BGA with wire-bonding technique
  - chip is put into the cavity of substrate
  - chip I/Os are connected to bonding pads around the cavity
  - substrate routing connects bonding pads with balls

- Packaging in BGA with flip-chip technique
  - re-distribution layer, RDL, routing connects chip I/Os to bump array
  - escape routing breaks bumps out to substrate routing layer
  - break points lay on the escape boundary
  - substrate routing connects break points to balls

Substrate Routing (2)

- Substrate routing usually has two steps: topological routing and detailed routing

- [W. W. Dai, DAC, 1991] discussed detailed routing

- This paper studies topological routing

- Substrate routing is preferred to be planar, even though multiple routing layers are available

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Existing work

- [S. S. Chen, ASPDAC, 1999] [Y. Kubo, ISPD, 2005] [C. C. Tsai, IEEE Trans, 1998]
    - assumed that start-points are located side to side with respect to balls.
    - are NOT flexible enough for SiP and even some one-die packages

- [M. F. Yu, ASPDAC, 1995] [M. F. Yu, ICCAD, 1996]
    - use the minimum-cost maximum flow algorithm to solve interchangeable pin routing problem
    - however, specifying ball assignment is preferred by designers to consider constraints of PCB

- [Y. Kubo, et al, ISPD'05]
    - considered the staggered via assignment in substrate routing,
    - and well solved the two-layer substrate routing problem

Our Major Contributions

- Our algorithm honors flexible locations for start-points, instead of the existing 1.5-dimensional routing

- Our substrate router solves the specified-pin-assignment substrate routing problem

- It considers the staggered via assignment for multiple-layer substrate routing
  - ⊙ end-zone model is proposed

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Staggered via and end-zone

- When dropping signal vias
  - close to the positions above assigned destination ball
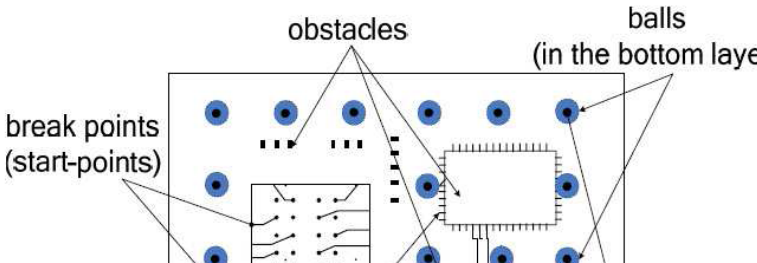 - vias need to be staggered
  - required offsets between staggered
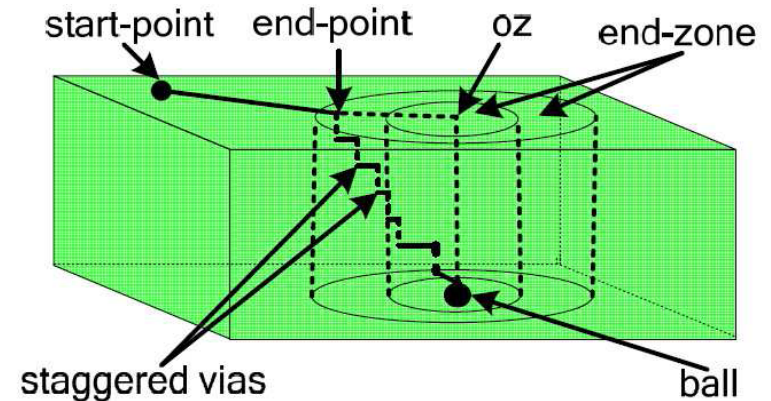
- End-zone includes two cycles with center aligned with the ball

- Radii   , and
  - where   and   are the minimal and maximal staggered via pitch i $d_1 = \sum_i md_i$ ex i $d_2 = \sum_i pd_i$

md_i pd_i

Problem formulation

- **Given**
  - start-points,
  - assigned balls (in the bottom layer),
  - netlist (dened by ball assignment),
  - and obstacles (including the escape area for escape routing, the pre-routed connections, vias, and other obstacles in the layer),

- **Find**
  - a topological routing solution connecting each start-point to any point in the end-zone for the assigned ball

- **Such that**
  - routed nets are planar
  - satisfy the capacity constraints,
  - and have minimal length
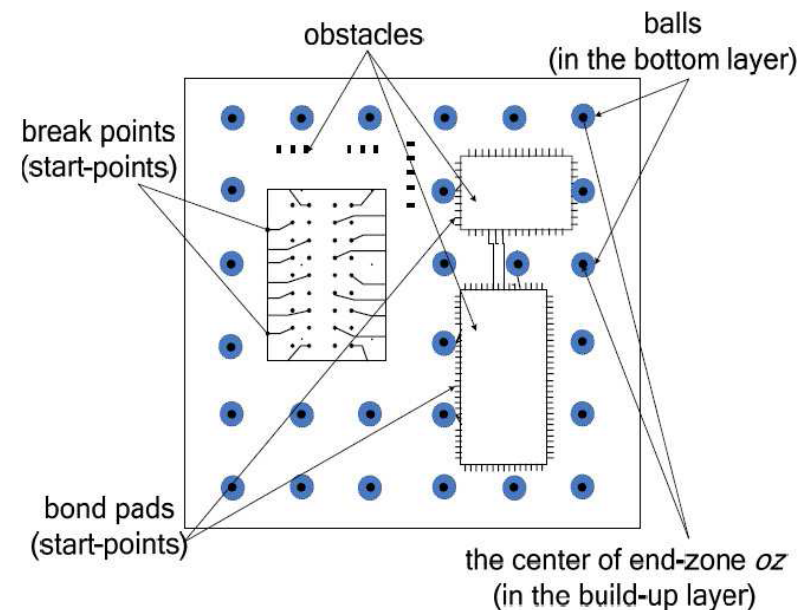
Data Structure

- The substrate routing plane (SF is triangle- meshed by constrair Delaunay triangulation (CDT)
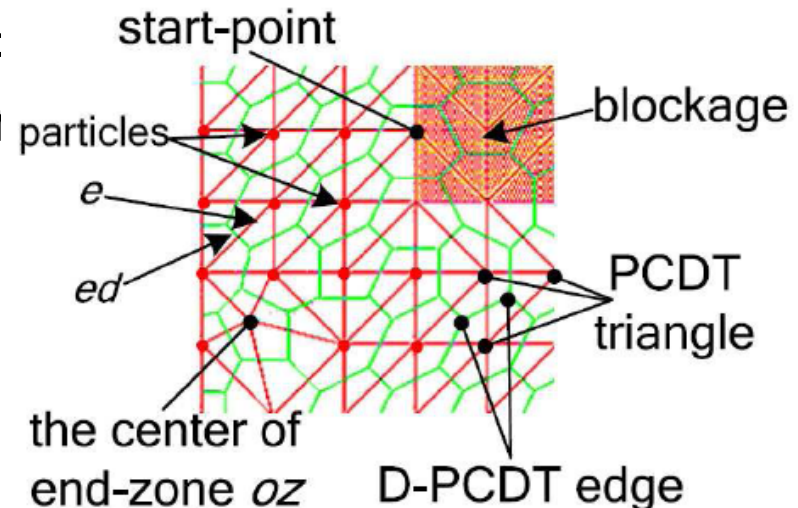
- Uniformly spreading points are added for particle-insertion-based CDT

- Capacity

$$C_{ed} = l_e$$

- Congestion

$$\eta_{ed} = \frac{\sum_i (w_i + s_i)}{C_{ed}}$$

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Framework

- Iterative scheme is derived from [R. Nair, TCAD, 1987]
  - Only one net is ripped up at a time
  - Every net is ripped up and rerouted on every iteration

- During iterative scheme
  - net path search by algorithm *DS**
  - reorder nets for wire length reduction, based on strategies
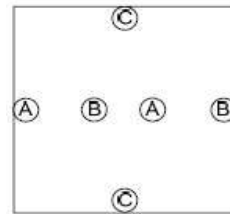   - whole reordering, and
    - partial reordering

Net path search algorithm *DS**

- Net path search algorithm *DS**
  - ◉ based on the heap implementation of Dijstra
  - ◉ honors estimation cost
  - ◉ honors *dynamic pushing*
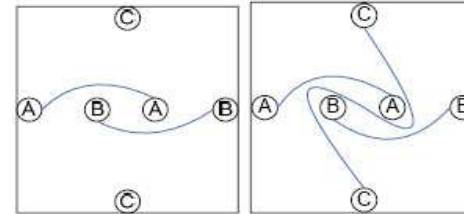 - ◉ honors *flexible via-staggering* in a end-zone

Dynamic pushing methodology

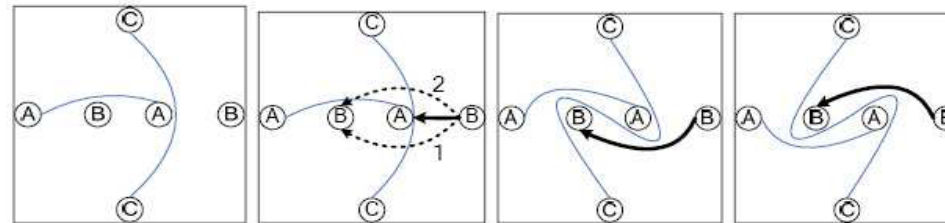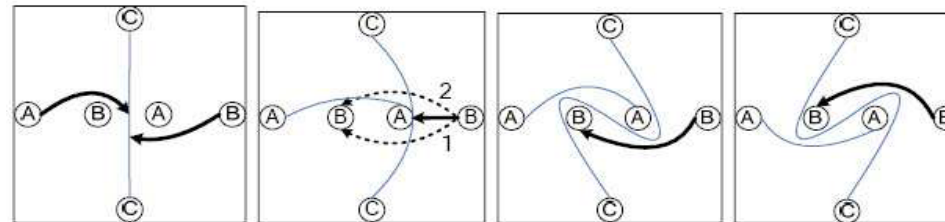● Dynamic pushing helps tackle the net ordering problem
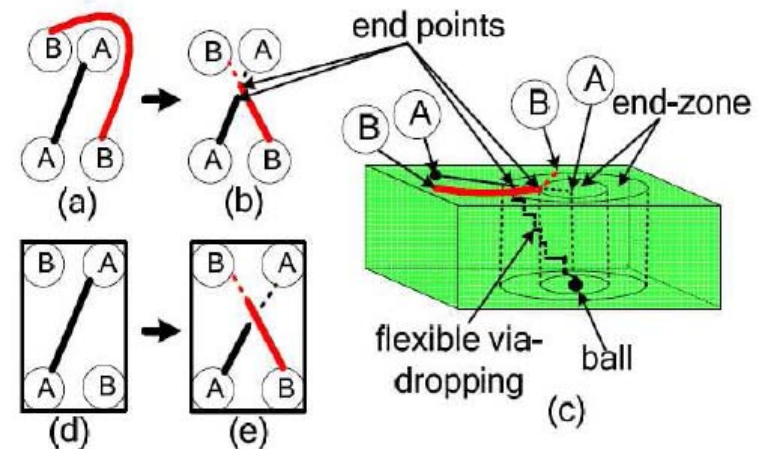
(A, B)-C

A-C-B或B-C-A

C-(A, B)

Flexible via-staggering

- Flexible via-staggering

  ⊙ reducing wire length

  ⊙ improve success ratio

- Define the cost for stopping at end-zone
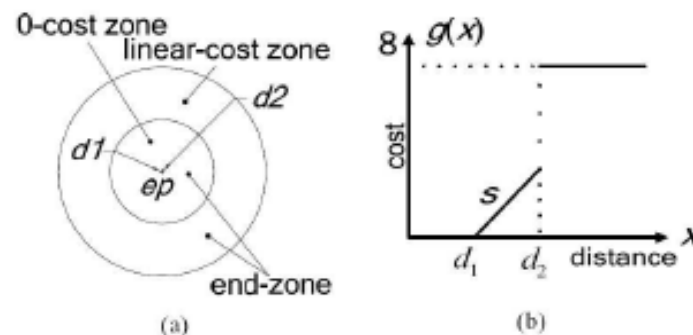
Reorder nets for wire length reduction

- Reordering algorithm
  - ⊙ routing nets frequently results in bent wires caused by pushing,
  - ⊙ bent wires usually involve unnecessary detours and increase total wire length
  - ⊙ solve this problem by designing a good order for rerouting
  - ⊙ whole reordering strategy
  - ⊙ partial reordering strategy

Whole/Partial reordering
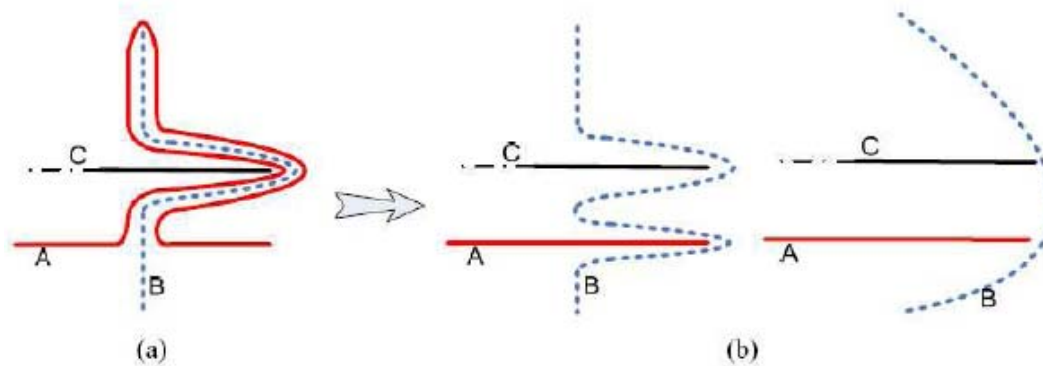

- Whole reordering--larger net length ratio first
- Net length ratio $\quad \delta = l/u$
  - is the net length acquired from the latest routing iteration
  - is the distance from start-point to end-point *oz*
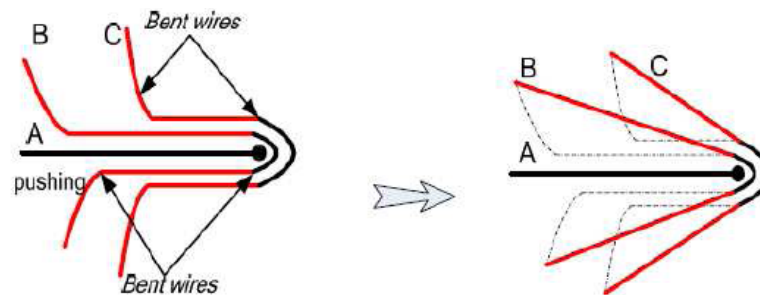
- Partial reordering--according to pushing order C-B-A

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Experimental results

Table 1: TEST CASES AND EXPERIMENTAL RESULTS
(*: Package size and Die (s) size are given by width × length (μm) in rectangle.)

Name of circuit	Package type	Package size*	Die(s) size*	Number of nets	# of failed nets BKM	# of failed nets new	Runtime(s) BKM	Runtime(s) new	Average WL (μm) BKM	Average WL (μm) new
case 1	2-2-2	35000 × 35000	14000 × 15000	474	52	16	2.06	11.33	9.10E+03	8.49E+03
case 2	2-2-2	30000 × 30000	9000 × 10500	543	10	0	1.90	5.34	8.24E+03	7.99E+03
case 3	3-1-3	40000 × 40000	9300 × 9300	800	306	49	13.81	16.86	1.65E+03	1.37E+03
case 4	3-2-3	35000 × 35000	12000 × 12000	506	82	6	6.90	8.46	2.29E+04	1.78E+04
case 5	3-2-3	40000 × 40000	20000 × 22000	891	98	45	2.60	13.65	5.93E+03	5.27E+03
case 6	4-2-4	40000 × 40000	20000 × 23000	990	198	51	9.95	26.62	9.10E+03	7.93E+03
case 7	4-2-4	45000 × 45000	20000 × 19000	1009	100	14	5.91	26.14	2.31E+04	1.89E+04
case 8	1-0-1	12000 × 12000	3900 × 6700 4400 × 5700 3200 × 4400	349	60	22	15.24	1.51	1.83E+03	1.73E+03
case 9	2-2-2	37500 × 37500	11000 × 10000 4700 × 3800 4600 × 5500	538	30	9	95.17	110.93	9.78E+03	9.38E+03
total	—	—	—	6100	936	212	—	—	—	—
average	—	—	—	—	—	—	—	—	1.02E+04	8.76E+03 (-13.9%)

- Comparing with a best know method (BKM) in an industrial design tool, our routing algorithm
  - leaves 212 failed, a 4.5-times unrouted net number reduction
  - reduces the average wire length by 13.9%

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Conclusion

- Considering high density packaging, we have developed a planar topological router.

- Compared with one current industrial router, Our algorithm
  - ⊙ does not limit start-point locations
  - ⊙ allows the routing to finish in a zone or at fixed locations
  - ⊙ honors the ball assignment specified for start-points.

- A 4.5x unrouted net number reduction and practically more design time reduction
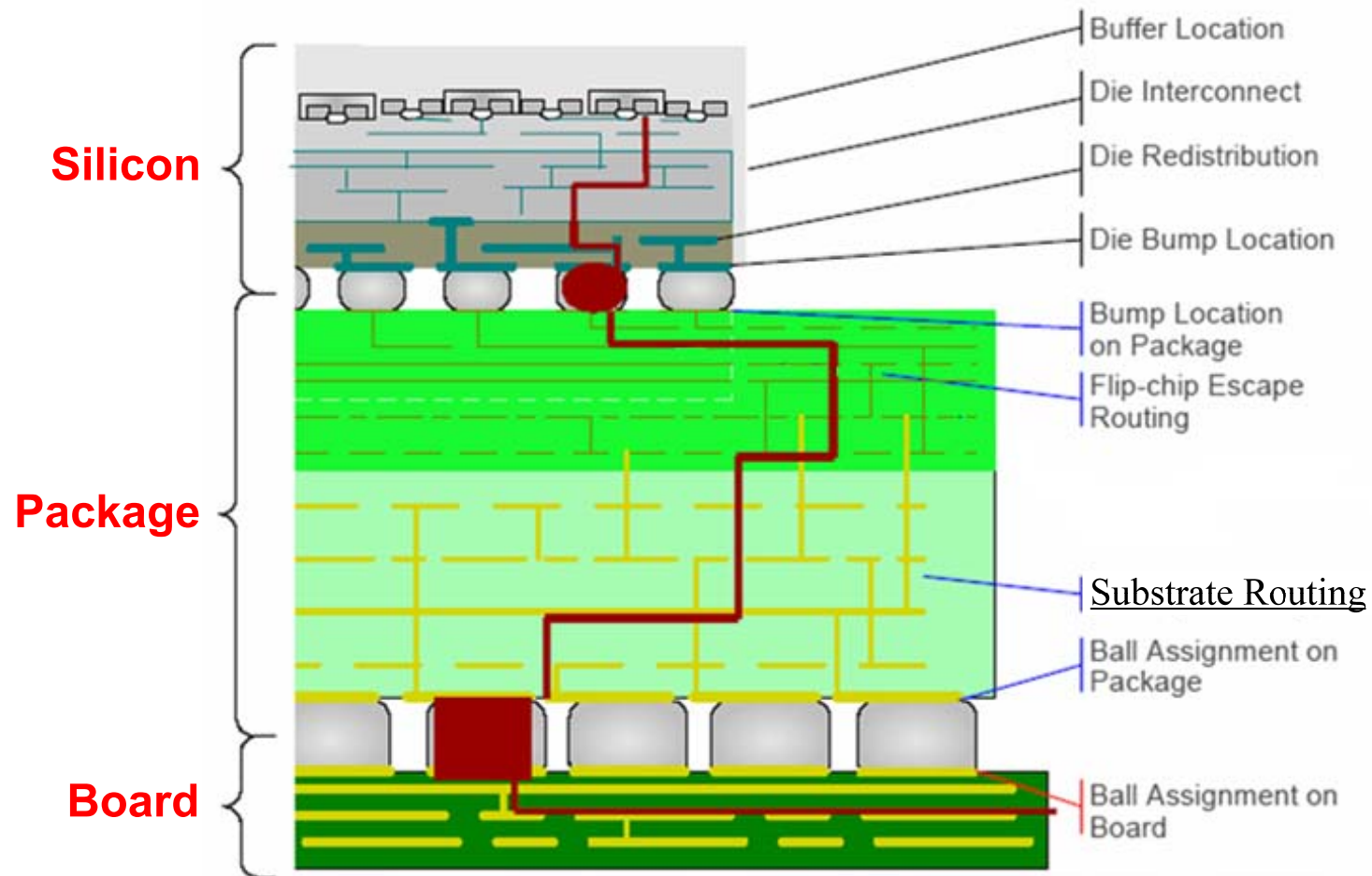
Thank You
Q&A

PGA and BGA

● Comparing with PGA substrate, BGA substrate has the advantages of

- ⊙ higher integrity,
- ⊙ higher reliability,
- ⊙ lower coupling,
- ⊙ cheaper cost, and
- ⊙ lower thermal-resistance
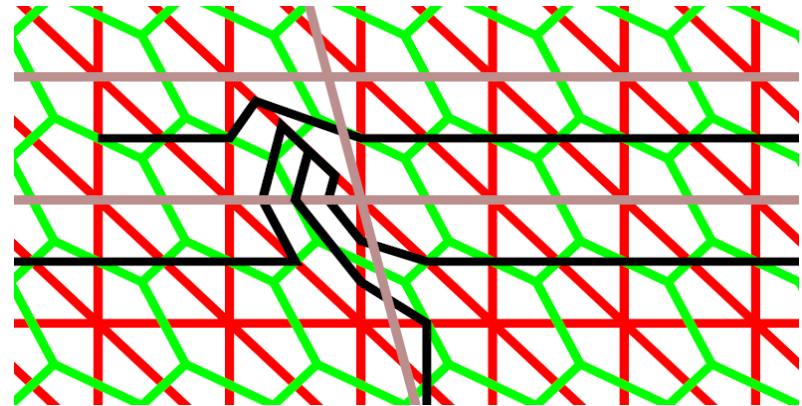
An example of flip-chip BGA

(Cadence)

Cost function

Initial

$$w = w_0 + s_0$$

$$rc = p_0 \times w$$

$$ec = \begin{cases} (h_0 - d_2) \times w + (d_2 - d_1) \times \min(s, w), & h_0 > d_2 \\ (h_0 - d_1) \times \min(s, w), & d_1 \leq h_0 \leq d_2 \end{cases} \qquad (8)$$

Recursive equations

$$w* = w + 2 \sum_i (w_i + s_i) \qquad (5)$$

$$rc* = rc + \triangle p \times w* \qquad (6)$$

$$ec^* = \begin{cases} (h - d_2) \times w^* + (d_2 - d_1) \times \min(s, w^*), & h > d_2 \\ (h - d_1) \times \min(s, w^*), & d_1 \leq h \leq d_2 \end{cases} \qquad (9)$$