

Simultaneous Shield Insertion and Net Ordering under Explicit RLC Noise Constraint *

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Abstract

For multiple coupled RLC nets, we formulate the min-area simultaneous shield insertion and net ordering (SINO/NB- v) problem to satisfy the given noise bound. We develop an efficient and conservative model to compute the peak noise, and apply the noise model to a simulated-annealing (SA) based algorithm for the SINO/NB- v problem. Extensive and accurate experiments show that the SA-based algorithm is efficient, and always achieves solutions satisfying the given noise bound. It uses up to 71% and 30% fewer shields when compared to a greedy based shield insertion algorithm and a separated shield insertion and net ordering algorithm, respectively. To the best of our knowledge, it is the first work that presents an in-depth study on the min-area SINO problem for multiple RLC nets under an explicit noise constraint.

1. INTRODUCTION

It becomes increasingly evident that on-chip inductance, especially mutual inductance, should be considered for high-performance interconnect design. There has been some preliminary work using RLC interconnect models, including routing topology generation [1], wire sizing [2], and buffer insertion [3]. However, all of these assume a single RLC net without considering mutual inductance. One very recent work [4] studies simultaneous shield insertion and net ordering (SINO), minimizing the area under a given noise bound due to the “long-range” coupling of mutual inductance. A *shield* is a wire connected to P/G structures. The current is assumed to return from the nearest shield, therefore, the mutual inductance beyond a shield becomes negligible. The same assumption is also used later in a twisted-bundle layout scheme [5] to minimize inductive coupling.

However, the current does not return from the nearest

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shield in all cases. Let a *block* denote the set of wires between two adjacent shields. The current often returns from quiet wires within a block if there are plenty of quiet wires in the current block. On the other hand, substantial current often returns from shields or quiet wires outside the block when multiple wires in the block switch simultaneously. While minimizing area for a noise bound is the most practical design objective and is considered in [4] (but not [5]), the inductive coupling coefficient rather than noise voltage is used as the noise bound.

In this paper, we first develop an efficient and conservative model to compute the peak noise voltage, using the partial inductance model without assuming any current return path. Applying the new noise model, we formulate and solve a new SINO problem (herein referred to as the SINO/NB- v problem) to find a min-area SINO solution satisfying a given noise constraint in terms of the noise voltage. The rest of this paper is organized as follows: Section 2 reviews the related work and formulates the new SINO problem. Section 3 presents the new noise model, and Section 4 introduces algorithms to solve the SINO/NB- v problem. Section 5 describes the tool implementation and analyzes experimental results. Section 6 concludes the paper, with discussion of future work. A full version of this paper is given as [6]. The full version, together with the recent progress, is available at <http://eda.ece.wisc.edu>.

2. PROBLEM FORMULATIONS

In this work, we consider interconnect structures the same as those presented in [4], i.e. parallel coplanar interconnect structures. For more detail about the characteristics and assumptions in studying these structures, please refer to [6]. We exploit the concept of net sensitivity where two nets s_1 and s_2 are considered sensitive to each other if a switching signal on s_1 will cause s_2 to malfunction (due to extraordinary crosstalk or delay variation) or vice-versa. We use the following “strict” definition for an aggressor: s-wire s_i is an aggressor for s-wire s_j if and only if the two wires are sensitive to each other. For a SINO string $s_1 s_2 g s_3 s_4$, if s_1 and s_3 are sensitive to victim s_4 , but s_2 is not sensitive to victim s_4 , the given SINO string can be also represented as *aggav*, meaning that for noise computation, s_1 and s_3 are aggressors for the victim and s_2 as well as the shield are quiet wires for the victim.

The SINO problem has been studied in [4]. A K_{eff} model is developed for the inductive coupling coefficient, which is used as the figure of merit for inductive coupling. According to the K_{eff} model, an s-wire is inductive noise free if

it does not share a block with any aggressor. Further, s_i is capacitive noise free if it is not directly adjacent to any aggressor. A placement P (equivalently, a SINO solution, or a SINO string) is noise bounded if, and only if, all nets s_i within P are capacitive noise free and inductive noise is less than a given threshold value ($K_{threshold}$). We refer to this formulation as the SINO/NB- k problem in this work.

To overcome the limitations of the SINO/NB- k formulation as discussed in Section 1, we formulate the following new SINO/NB- v problem:

FORMULATION 1. Optimal SINO/NB- v problem: For a set of signal nets, find a solution P with the minimum area by simultaneous shield insertion and net re-ordering such that the peak noise of any wire s_i in P satisfies the given explicit noise constraint for wire s_i .

In this problem formulation, the *peak noise* is the maximum noise that can be induced in the victim over all signal patterns for its aggressors. An efficient model for the peak noise is of paramount importance to solving the SINO/NB- v problem. We will present such a noise model in Section 3. Further, our noise model, SINO algorithms and implementations in this paper are able to consider different geometries, driver/receiver strengths, and noise bounds for different nets. For simplicity of presentation, we assume that the coplanar interconnect structure is uniform in terms of wire width and spacing, driver/receiver strength, and we find a SINO solution where the peak noise among all nets satisfies a given noise voltage bound.

3. RLC NOISE MODELING

We now discuss the circuit model for coplanar interconnect structures. We also present the noise computation to obtain the peak noise in the victim induced by the worst-case signal pattern for all aggressors. Extensive experiments in [6] show the noise model is conservative compared to SPICE simulation with a distributed RLC circuit model.

A. Circuit Model

For each victim under study, we map the wide interconnect structure into a number of three-segment RLC circuits. We use a four-bit bus in Figure 1 to illustrate our idea, assuming that s_1 is the victim. First, if either the first-order neighbor s_2 or the second-order neighbor s_3 is an aggressor, a three-segment RLC circuit is constructed for s_3 , the victim s_1 , and its first-order neighbor s_2 , using a single segment for each wire. The circuit contains R_i , L_i , and C_i ($i = 1, 2$, and 3), where R_i is the sum of the resistance of w_i and its driver, L_i is the self inductance of the net, and C_i is the sum of the ground capacitance of w_i and its loading capacitance. In addition, the circuit has coupling inductances L_{12} , L_{13} , and L_{23} , as well as coupling capacitances C_{12} and C_{23} .

Then, if s_4 is an aggressor, another three-segment RLC circuit is constructed for s_4 , the victim s_1 , and its first-order neighbor s_2 , again using a single segment for each wire. Similar to the circuit for s_1 , s_2 and s_3 , the new circuit contains R_i , L_i , and C_i ($i = 1, 2$, and 4), as well as coupling inductances L_{12} , L_{14} , and L_{24} . However, it has only one coupling capacitance C_{12} . Therefore, we consider coupling inductance between any two wires, but consider coupling capacitance only between adjacent wires. The inductance and capacitance are computed based on [7, 8]. Another

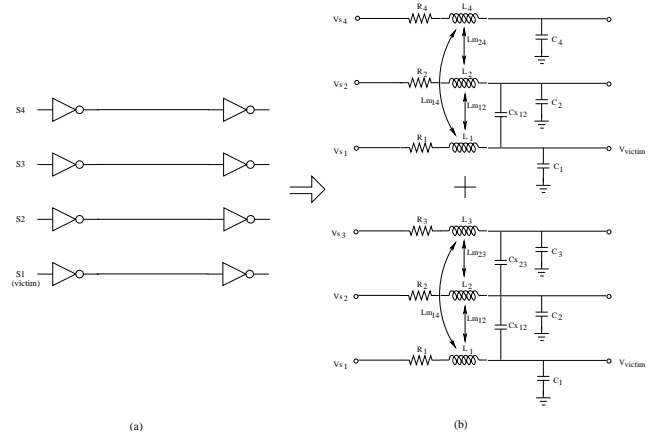


Figure 1: A four-bit bus is modeled by two three-segment RLC circuits, where s_1 is the victim, and s_2 , s_3 , and s_4 are potential aggressors.

three-segment circuit is constructed for another aggressor s_i beyond s_4 , considering wires s_1 , s_2 and s_i .

B. Noise for three-segment circuit

Given s_1 , s_2 , and s_3 are the wires in the three-segment RLC circuit, the quiet victim s_1 has noise voltage

$$V_{victim} = H_2 \cdot V_{s2} + H_3 \cdot V_{s3} \quad (1)$$

where V_{s2} and V_{s3} are the input to s_2 and s_3 , respectively, and H_2 and H_3 are their transfer functions in the s-domain. Both H_2 and H_3 have the following form

$$H_{2 \text{ or } 3} = \frac{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4}{b_0 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4 + b_5 s^5 + b_6 s^6} \quad (2)$$

We use a five-pole model to first solve H_2 and H_3 and then obtain a solution to Eqn. (1) using the superposition rule. We always assume the worst-case signal pattern—either *vqa* or *vaa* for the three wires. *vqa* means that victim is quiet, s_2 is quiet or is a shield, and s_3 is a switching aggressor. *vaa* means that victim is quiet, and both s_2 and s_3 are aggressors with same-direction switching. The coefficients and solution of Eqn. (1) can be found in [6].

C. Overall noise with inductance screening

We compute the overall noise for a victim in a bus structure as the sum of noise over all three-segment RLC circuits corresponding to all aggressors for the victim. We use the following inductance screening rule to decide the scope of *effective* aggressors: Let K_s be the screening constant, $W_a(a_i)$ is the accumulative wire width for aggressors between the victim and aggressor a_i (including a_i), and $W_q(a_i)$ is the accumulative wire width for quiet wires or shields between the victim and aggressor a_i (excluding the quiet victim). If $W_a(a_i) \cdot K_s \leq W_q(a_i)$, aggressor a_i does not contribute to the inductive noise induced in the victim. Our peak noise model *always* considers aggressors in the current block, i.e., we only use the screening rule for aggressors outside the current block. Our screening rule is victim-oriented, and is a variant to the aggressor-oriented screening rule in [9].

Our screening rule can be illustrated by the following SINO string:

$$a_1qa_2a_3a_4qva_5qa_6$$

where a_1, \dots, a_6 are aggressors, v is the victim, and q 's are either quiet wires or shields. We assume that all wires have the same width w . When the screening constant $K_s = 0.5$, for aggressor a_4 , $W_a(a_4) = w$, $W_q(a_4) = w$, therefore $0.5W_a(a_4) < W_q(a_4)$ and a_4 is not an effective aggressor; for aggressor a_2 , $W_a(a_2) = 3w$, $W_q(a_2) = w$, therefore $0.5W_a(a_2) > W_q(a_2)$ and a_2 is an effective aggressor.

4. PROPERTIES AND ALGORITHMS

We have proved in [6] that

THEOREM 1. *The optimal SINO/NB- v problem is NP-hard.*

Therefore, we focus on heuristic methods to obtain high-quality solutions with reasonable computation time. We extend three of the approximate algorithms originally developed in [4] for solving the SINO/NB- k problem: greedy-based shield insertion (SI) algorithm, net ordering for minimizing Cx noise followed by SI (NO+SI) algorithm, and simulated-annealing based SINO (SINO) algorithm. However, these SINO/NB- v algorithms are more complicated than those SINO/NB- k algorithms using the K_{eff} model. First, our peak noise model may consider aggressors beyond the current block whereas the K_{eff} model considers aggressors only within the current block. Second, the victim may be placed directly adjacent to an aggressor in the SINO/NB- v formulation but not in the SINO/NB- k formulation. In this paper, we only describe essential algorithm differences between SINO/NB- v w.r.t. SINO/NB- k algorithms, with complete detail on the SINO/NB- v algorithms in [6].

A. Greedy Based Shield Insertion Algorithm

The essence of the greedy-based shield insertion (SI) algorithm is the following: Run through the given placement P , at first ignoring the inductance screening rule presented in Section 3. At each location in the placement, calculate the maximum value of N_i that would exist in the current block if we allowed net s_i to become a member. If N_i is greater than N_{thresh} , then create a new block. In a second pass over the interconnect structure, we consider inductance screening. If any N_{thresh} violations are detected, we insert shields to eliminate them.

The solution given by the SI algorithm depends on the initial placement. If sufficient capacitive coupling exists, obviously, the number of shield wires can be reduced by first running existing net ordering algorithms to re-order nets so that no sensitive nets are adjacent to each other and subsequently invoking the SI algorithm. This leads to the NO+SI algorithm.

B. Simulated Annealing Based SINO Algorithm

The simulated annealing algorithm used in this work is essentially the same as the algorithm presented in [4]. The figure of merit used to guide SINO/SA is a weighted sum of placement size, number of N_{thresh} violations, and the *Noise Violation Figure* (roughly equivalent to the Inductance Violation Figure in [4] but also considers inductance screening.) A simple multiplicative constant of the current

Parameter	Values
Vdd, Clock	1.05V, 3GHz
N_{thresh}	0.15V, 0.20V, 0.25V
Rise time	33 ps (10% of 3GHz clock)
Length	1400 μm , 2000 μm
Sensitivity rates	30%, 60%
R_{drive}, C_{load}	150 Ω , 60fF
Screening constant K_s	0.33

Table 1: Interconnect parameters for 0.07 μm technology and experiment settings.

temperature determines the annealing schedule with all relevant parameters (initial temperature, final temperature, annealing schedule, and figure of merit component weights) determined experimentally to minimize the overall number of shields inserted without N_{thresh} violations.

The solution space perturbations allowed to generate a new placement P' from placement P (possible with equal probability) are: (i) Combine two random blocks in P (remove a shield), (ii) Swap two random s-wires in P , (iii) Move a single random s-wire to a new and random location, (iv) Insert a shield at a random location in P .

C. Algorithm Speedup

Because the complexity of the explicit noise computation model used in this work is substantially greater than the K_{eff} model in [4], we use a few methods to speed up our algorithms: (i) We exploit the symmetry of the uniform coplanar structure to perform table-based lookups of noise values computed previously in other iterations in the algorithm(s), (ii) We exploit the highly efficient K_{eff} model at high temperatures in SINO/SA- v when accuracy is not paramount, and switch at a given temperature to the explicit noise model. Greater detail about these two techniques, as well as validation of the accuracy of (ii) vs. using the explicit noise model exclusively (as we do in all results presented here) is available in [6].

5. EXPERIMENTAL RESULTS AND DISCUSSIONS

We have tested our algorithms with many different geometries and experimental parameters for the coplanar interconnect structure assumed in this work with the parameters shown in Table 1. We generate twenty different sensitivity matrices and initial placements for each design combination, and present the averages over these runs for 32 signal nets in Tables 2 and 3. We did not tune the screening constant K_s and our SA-based SINO algorithm for different examples.

The peak noise value is the maximum noise among all wires in a SINO solution considering the worst-case signal patterns. To compute the peak noise, we generate a detailed RLC circuit model for each solution generated by our algorithms. We use an RLC-segment for each 100 μm -long wire segment with a mutual inductance between any two such wire segments, and simulate with SPICE. The partial inductance model is used to achieve high accuracy. We report the maximum and average peak noise for twenty randomly sampled nets for each design combination.

Table 3 presents maximum and average peak noise values obtained by our accurate verification. One can easily

noise bound	length = 1400 μ m			length = 2000 μ m		
	SI	NO+SI	SINO	SI	NO+SI	SINO
spacing = 0.8 μ m, sensitivity rate = 30%						
0.15V	0.0535/0.0460	0.0899/0.0627	0.1022/0.0758	0.0511/0.0452	0.0917/0.0658	0.1003/0.0740
0.20V	0.0594/0.0506	0.0899/0.0627	0.1194/0.0761	0.0699/0.0497	0.1095/0.0738	0.1112/0.0755
0.25V	0.0713/0.0544	0.1175/0.0769	0.1242/0.1013	0.0683/0.0502	0.1126/0.0941	0.1268/0.1005
spacing = 0.8 μ m, sensitivity rate = 60%						
0.15V	0.0549/0.0485	0.1087/0.0926	0.1073/0.0799	0.0504/0.0311	0.1084/0.0991	0.0967/0.0805
0.20V	0.0639/0.0522	0.1261/0.1007	0.1156/0.0873	0.0475/0.0371	0.1300/0.1099	0.1132/0.0854
0.25V	0.0698/0.0577	0.1249/0.1085	0.1250/0.1104	0.0578/0.0404	0.1283/0.1126	0.1254/0.0915

Table 3: SPICE-computed maximum and average peak noise for interconnect synthesis solutions given by different algorithms. In each cell of the table, the first value is the maximum peak noise and the second value is the average peak noise (in V).

noise bound	length = 1400 μ m			length = 2000 μ m		
	SI	NO+SI	SINO	SI	NO+SI	SINO
spacing = 0.8 μ m, sensitivity rate = 30%						
0.15V	12.70	6.10	4.85	15.25	7.00	5.40
0.20V	11.85	5.35	4.40	14.90	6.15	5.05
0.25V	11.20	4.85	3.95	14.60	6.00	4.20
spacing = 0.8 μ m, sensitivity rate = 60%						
0.15V	22.00	8.95	7.60	25.55	10.80	7.85
0.20V	20.55	8.00	6.55	23.95	10.60	7.45
0.25V	20.10	6.80	6.20	23.70	9.75	7.40

Table 2: Number of shields needed by algorithms SI, NO+SI, and SINO.

see that the peak noise for all 720 test cases presented in this paper satisfies the given noise bound, and there is a smooth tradeoff between the resulting average number of shields and average peak noise. This validates our peak noise model, the SINO/NB- v problem formulation, and the toolset implementation.

As all solutions meet the given noise bounds, the algorithm quality is measured by the number of shields needed for the given noise bound. Table 2 presents numbers of shields used by different algorithms. As we anticipate, SI is always worse than NO+SI and SINO, and SINO is always best. The length greatly affects the evaluation of algorithm quality. For the shorter length (1400 μ m), SINO uses up to 20% and 69% fewer shields when compared to NO+SI and SI, respectively. For the longer length (2000 μ m), the improvement is up to 30% and 71%, respectively. We also observe that the number of shields required for all algorithms at 2000 μ m ranges from 3% to 30% more (across all algorithms), as one would expect because of greater coupling between longer structures which requires more shielding to negate it. However, for NO+SI the maximal increase in shielding resources is 43%, but for SINO it is only 19% (furthermore, this general relationship holds for all entries in Table 2), indicating that SINO is more capable of handling changing geometries efficiently.

6. CONCLUSIONS AND FUTURE WORK

For a number of coupled RLC nets, we have formulated the min-area simultaneous shield insertion and net ordering (in short, SINO/NB- v) problem to satisfy the given bound

on noise voltage. We have developed an efficient model to compute the peak noise among coupled RLC nets, and have applied the noise model to a simulated-annealing (SA) based algorithm for the SINO/NB- v problem. Accurate verification shows that the SA-based algorithm always achieves a SINO solution satisfying the given noise bound, and uses up to 71% and 30% fewer shields when compared to a greedy based shield insertion algorithm and a separated shield insertion and net ordering algorithm. As shown in [6], our SA-based algorithm is efficient to optimize a 32-bit bus in approximately 10 seconds.

The simplest interconnect structure, parallel bus structure, is assumed in this work. We are working on the SINO/NB- v problem for the multi-layer routing model with regular P/G networks, and intend to further incorporate the SINO/NB- v formulation into the global routing problem.

7. REFERENCES

- [1] J. Cong and C.-K. Koh, "Interconnect layout optimization under higher-order RLC model," in ICCAD, 1997.
- [2] T. Xue, E. S. Kuh, and Q. Yu, "A sensitivity-based wiresizing approach to interconnect optimization of lossy transmission line topologies," in *Proc. IEEE Multi-Chip Module Conf.*, pp. 117–121, 1996.
- [3] Y. I. Ismail and E. G. Friedman, "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits," in DAC 1999.
- [4] L. He and K. M. Lepak, "Simultaneous shielding insertion and net ordering for capacitive and inductive coupling minimization," in ISPD, 2000.
- [5] G. Zhong, H. Wang, C.-K. Koh, and K. Roy, "A twisted bundle layout structure for minimizing inductive coupling noise," in ICCAD, 2000.
- [6] K. M. Lepak, I. Luwandi, and L. He, "Simultaneous shield insertion and net ordering under explicit noise constraint," Tech. Rep. ECE-00-006, University of Wisconsin, 2000.
- [7] L. He, N. Chang, S. Lin, and O. S. Nakagawa, "An efficient inductance modeling for on-chip interconnects," in IEEE CICC, pp. 457–460, 1999.
- [8] J. Cong, L. He, A. B. Kahng, D. Noice, N. Shirali, and S. H.-C. Yen, "Analysis and justification of a simple, practical 2 1/2-d capacitance extraction methodology," in DAC, 1997.
- [9] S. Lin, N. Chang, and O. S. Nakagawa, "Quick on-chip self- and mutual-inductance screen," in *International Symposium on Quality of Electronic Design*, 2000.