Integrity-driven Power and Signal Network Codesign [*]

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Abstract

Conventional physical design flow separates the design of power network and signal network. Such a separated approach results in slow design convergence for wire-limited deep sub-micron designs. In this paper, we present a novel design methodology that simultaneously considers global signal routing and power network design under integrity constraints. The key part to this approach is a simple yet accurate power net estimation formula that decides the minimum number of power nets needed to satisfy both power and signal integrity constraints prior to detailed layout. The proposed design methodology is a one-pass solution to the co-design of power and signal networks in the sense that no iteration between them is required in order to meet design closure. Experiment results using large industrial benchmarks show that compared to the state-of-the-art alternative design approach, the proposed method can reduce the power network area by 19.4% on average under the same signal and power integrity constraints with better routing quality, but use less runtime.

1 Introduction

Power distribution network and signal network are two major resource consumers for wire-limited deep sub-micron (DSM) designs. In a conventional physical design flow, they are designed separately. The power network is designed first to respect the power integrity, and then signal network is routed under the remaining routing resource budgets. The separated design flow has the following two drawbacks: (1) the power network tends to over-design to have power network area more than necessary to satisfy power integrity constraints because of the lack of knowledge about the following signal routing; (2) the remaining resource budgets

after power network design may be too restrictive for a routing algorithm to find a feasible signal routing solution. Iterations between signal routing and power network design are seldom avoidable and design closure suffers.

To make things even worse, as VLSI technology advances, signal integrity becomes more and more critical due to the higher operating frequency and closer proximity between metals. Two major facts that contribute to signal integrity problems are the increasing capacitive coupling and inductive coupling. In addition to sizing, spacing, and buffering, shielding has been proven to be effective to improve signal integrity because it can not only reduces the capacitive coupling between signal nets, but also provides a closer current return paths for signals. Shields are usually inserted into the layout after signal routing, hence they contend for the same scant routing resources left for signal routing. The overhead due to shielding makes it even harder for the routing algorithm to find a one-pass routing solution successfully. Note that in the final layout, shields indeed form part of the power network. Therefore, it makes sense for us to consider shielding when we design the power network and that the area overhead due to shielding should be accounted into power network's resource budgets. However, as the accurate shielding information is only known after detailed signal routing, it is impossible to consider shielding during the power network design stage in the conventional separated design flow. Therefore, an integrated resource management and co-design of both power network and signal routing are in great demand.

There are very limited previous works on this subject. The reason is that both signal routing and power network design are computationally intensive, and combining them results in a problem with even higher complexity. To the best of our knowledge, there are only two works in literature that have addressed such a similar problem [17, 15]. The authors in [17] added a feedback loop between the power network design and signal routing to resolve the resource contention problem. Because of the iterative nature of feedback, design convergence is very slow and only results on small benchmarks were reported[1]. Moreover, shielding was

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[1]In [17], the highest net number for one benchmark is 1294, and as

not considered yet in [17]. The authors in [15] addressed the problem in three steps: signal routing, power network routing, and then signal routing. Because their first routing stage was not aware of the following power routing, iterations may still be possible. Nevertheless, [15] did provide a new perspective to the conventional physical design flow, and such a three-step solution has been successfully applied to real industrial practices.

In this work, we propose a one-pass solution to the co-design of power network and signal routing under integrity constraints . The major motivation for this work is our awareness that the design convergence problem can only be solved by a correct-by-construction methodology rather than a trial-and-error approach. Moreover, to handle the high complexity of co-design, we have to employ high abstract level power integrity and signal integrity models for the purpose of computation efficiency. The rest of the paper is organized as follows: we discuss the preliminary and design constraints in Section 2 and our problem formulation in Section 3. We present the power net estimation formula in Section 4, algorithm details in Section 5, and experiment results in Section 6. We conclude this paper with discussion of our future work in Section 7.

2 Preliminary and Design Constraints

Both power and signal integrity constraints are closely related to timing and noise problems [22, 10]. However, timing and noise constraints are generally defined in electrical domain and are difficult to be directly used in physical layout. One way to bridge the gap between electrical constraints and physical layout is to convert these electrical constraints into physical layout "wiring rules" [5, 11]. In the following, a power pitch model is proposed to address the power integrity constraints, while the signal integrity constraints are converted to signal net shielding requirements. In Section 2.2, we will discuss the routing model used in this work.

2.1 Power Pitch and Signal Shielding Constraints

The goal of power network design is to satisfy the power integrity constrains with minimum routing area. IR-drop and Ldi/dt noise are two of the major factors contributing to power integrity problems. A power network is usually designed as a mesh to provide a low impedance current return path for signals. *Power pitch* is the separation between two adjacent power lines in a mesh structure. To ensure power integrity in the mesh structure, it is preferable to have a small power pitch. Because the smaller the power pitch, the smaller the power network's effective resistance and inductance, hence the smaller the IR-drop and

Ldi/dt noise. However, the smaller power pitch also implies more routing area for power network design. Therefore, a maximum power pitch should be carefully chosen such that the low impedance current return paths are still maintained at the full-chip level but with reasonable routing area. How to choose such a maximum power pitch constraints has been addressed in [16, 23, 14]. Therefore, a power network can be designed with a maximum power pitch constraint ($\overline{PGP}$) such that as long as its power pitch is less than $\overline{PGP}$, the resulting power network is guaranteed to satisfy the required IR-drop, Ldi/dt and electro-migration constraints. Such a power pitch model has been used successfully in real designs by [15]. Because of its simplicity and high abstraction, we employ the power pitch model in this paper. The benefit of using power pitch model is two-fold: avoiding the expensive numerical-based power network analysis [2, 10] and making it possible to check the power integrity constraints on-the-fly during signal routing.

Crosstalk reduction via shielding has been studied in [21, 20, 24]. Shielding requirements for signal nets are generated by a timing/noise optimization engine according to signal nets' sensitivity and criticality. How to generate shield requirements for signal nets has been described in [3] and has been employed by [15] for modern micro-processor designs. Similar to [15], we assume the shielding requirements for nets are part of the input. We call signal nets that require two adjacent shields as *s2-nets*, nets that require one adjacent shields as *s1-nets*, and nets that require no adjacent shields as *s0-nets*. s2-nets and s1-nets are also called *critical nets* in the following.

2.2 Routing Model

We tessellate the routing area into rectangular partitions as *routing tiles*, and all cells along with their connection pins are placed at the center of routing tiles. Single-source-multi-sink (SSMS) nets are considered. Fig. 1(a) shows a circuit after layout, where a routing of a one-source-three-sink net is also illustrated.
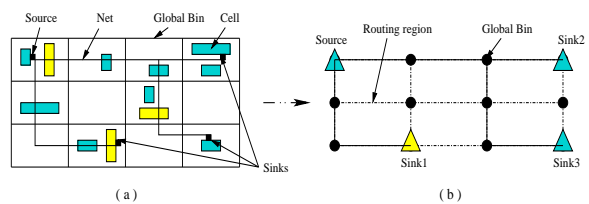

Figure 1. (a) Layout. (b) The corresponding routing graph.

The circuit layout can be formally modeled by an undirected graph $G(V, E)$, as shown in Fig. 1(b), where each

vertex $v \in V$ represents a routing tile, and each edge $e \in E$ represents the routing area between two adjacent tiles. To model the limited routing resources, we associate each edge in $G(V, E)$ with a *capacity*, which is defined as the maximum number of tracks available for routing. The capacity is decided by the geometry of the design and the technology used. In multilayer designs, an edge may consist of more than one layer. We assume that each layer is composed of equally spaced tracks and each track can be used by only one net segment. Therefore, we can accommodate multi-layer designs by increasing the capacity of each edge. An edge in the routing graph is also called a *routing region*. A *track assignment solution* in a routing region is the sequence of track numbers for all signal nets and power nets in that region. Similar to [24], an *extended global routing solution* not only decides the regions that every signal net is routed through, i.e., the set of edges to connect all nodes (global bins) that contain pins for the net, but also determines the track assignment solutions for all regions.

Because shields are part of the power network, we do not distinguish shields and power nets specifically in this paper. Assuming uniform wire sizing for all power nets and uniform length for all finest routing tiles, we can model the total power network area in terms of the total number of power nets (or shields) in the final layout:

$$PG_{area} = \sum_{\forall t} S_t \qquad (1)$$

where S_t is the number of power nets used in R_t. For a given routing region R_t, its routing density is defined as $Den_t = (G_t + S_t)/C_t$, where C_t is the routing capacity, G_t and S_t are the number of signal nets and power nets in R_t, respectively. When $Den_t > 1$, overflow occurs in R_t; otherwise, there is no overflow. Same as in [7, 17], we measure the overall routing congestion by the maximum density over all routing regions, i.e., $maxDen = max_{\forall t \in E} Den_t$.

3 Problem Formulation

As we discussed in Section 1, shields are effective to improve signal integrity but introduces routing area overhead. As the clock frequency continues to increase, the proportion of nets that require shielding is also growing. This trend implies that more and more routing area will be used solely for shielding purpose. In order to achieve design closure for both power network design and signal network design, we not only need to minimize the power network area, but also accurately allocate routing resources for shielding purpose. This is only made possible by a unified approach to the co-design of power and signal networks simultaneously. We formulate the co-design of power and signal network problem as follows:

Formulation 1 (GSPR Problem) *Given the power pitch constraint ($\overline{PGP}$), a placement solution, a net list, and the shielding requirements for all signal nets, the GSPR[2] problem synthesizes a power network and an extended global routing solution, such that the power network has a power pitch less than $\overline{PGP}$, the extended global routing solution satisfies the required shielding constraints for all nets, and the total power network area as defined in (1) is minimized.*

The GSPR problem has very high complexity. In order to solve it, we propose a novel design methodology in this paper. Instead of synthesizing the power network first as a conventional physical design flow does, we now synthesize a global routing solution first with power net estimation and minimization considering both the power pitch and signal shielding constraints. After global routing, we then synthesize a power network to satisfy the power pitch constraint, and at the same time decide track assignment solutions for all signal nets to satisfy their shielding requirements. The key of this approach is a simple yet accurate power net estimation formula that decides the minimum number of power nets needed to satisfy both power pitch and signal shielding constraints without knowing the exact power network design. We develop the power net estimation formula in Section 4, and discuss the algorithmic details in Section 5.

4 Power Net Estimation

A *valid* track assignment solution in R_t is a track assignment solution that satisfies both power pitch and signal shielding constraints. To find valid track assignment solutions for all net segments in all routing regions, we may need to insert many power nets. The exact number of power nets is only known after we have fixed the track assignment solution in each region. But at that time, it is often too late to correct a "bad" routing solution in case we could not find a feasible routing solution within the routing resource budgets. Therefore, in the following we develop a closed formula to estimate the minimum number of power nets in R_t without knowing its exact track assignment solution.

Lemma 1 *Given a routing region R_t with capacity C_t, in order to satisfy the power pitch constraint $\overline{PGP}$, the minimum number of power nets needed in R_t is given by $p_t = \lceil C_t / \overline{PGP} \rceil$.*

Therefore, knowing the power pitch constraint is equivalent to knowing p_t such that the resulting power pitch in R_t is less than $\overline{PGP}$.

Lemma 2 *Given a routing region R_t with m_2 number of s2-nets, m_1 number of s1-nets, and m_0 number of s0-nets,*

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[2]GSPR stands for Global Signal and Power co-Routing.

in order to satisfy the signal shielding requirements, the minimum number of power nets S_t^{si} is given as follows:

$$S_t^{si} = (\lceil \frac{m_1}{2} \rceil - b_2) + (m_2 + 1) \cdot b_2 \qquad (2)$$

where b_2 is a 0-1 function defined for m_2 such that $b_2 = 1$ when $m_2 > 0$, otherwise, $b_2 = 0$.

Proof: The minimum number of power nets in R_t is obtained when every power net is contributing two-side shielding effects for either s1-nets or s2-nets, i.e., there are either s1-nets or s2-nets on the two sides of every power net, while the signal shielding requirements are still satisfied. In this case, we cannot reduce any power net without violating the shielding constraints, therefore, the obtained number of power nets is minimum. Such a solution can be obtained by (1) alternating all m_2 s2-nets with power nets, and putting two s1-nets adjacent to the two outermost power nets; (2) sharing one power net between every remaining s1-net pair. As all s0-nets do not need any shields, the total power net number is the sum of the above two procedures: i.e., $(m_2 + 1) + \lceil (m_1 - 2)/2 \rceil = m_2 + \lceil m1/2 \rceil$. To accommodate the special cases when there is no s1-net or s2-net, we could obtain the more general equation as shown in (2). □

Lemma 1 and 2 give the minimum number of power nets to satisfy the power pitch constraint and signal shielding constraints, respectively. In order to satisfy both constraints, we have the following Theorem:

Theorem 1 *For a routing region R_t with two edge power nets, given the routed nets and their shielding requirements for signal integrity, and the minimum number of power nets for power integrity as $(p_t - 1)$[3], then among all valid track assignment solutions, the tight upper bound on minimum number of power nets is given as follows:*

$$S_t = \begin{cases} (\lceil \frac{m_1}{2} \rceil - b_2) + (m_2 + 1) \cdot b_2, & m_1 \geq 2 \cdot (p_t + b_2) \\ p_t + m_2 + 1, & b_2 = 1, m_1 \geq 2 \cdot p_t \\ p_t + m_2, & b_2 = 1, m_1 < 2 \cdot p_t \\ \lceil \frac{m_1}{2} \rceil, & b_2 = 0, m_1 \geq 2 \cdot p_t \\ p_t, & b_2 = 0, m_1 < 2 \cdot p_t \end{cases}$$

Proof:

We prove the theorem by construction for each case. And it is obvious that Lemma 1 and 2 give two easy lower bounds on the number of power nets for any valid track assignment solution in R_t. The maximum of the two, i.e., $\max(p_t, S_t^{si})$, results in a tighter lower bound. If a valid track assignment solution can achieve this tighter low bound, then it must also have the minimum number of power nets.

For case 1 where the number of s1-nets is great than two times the sum of p_t and b_2, i.e., $m_1 \geq 2 \cdot (p_t + b_2)$, the tighter lower bound is given by $\max(p_t, S_t^{si}) = S_t^{si}$. By construction, a valid track assignment solution for case 1 can be obtained as follows: (1) uniformly layout $(p_t - 1)$ power nets in R_t to satisfy the power pitch constraint; (2) put as many as $2 \cdot (p_t - 1)$ s1-nets adjacent to the already layout $(p_t - 1)$ power nets; (3) alternate all m_2 s2-nets with power nets, put two s1-nets adjacent to the two outermost power nets, and then assign the whole block into R_t; (4) put two s1-nets adjacent to the two edge power nets of R_t; (5) share one power net between every remaining s1-net pair, and assign them to any available tracks; (6) assign all s0-nets into the remaining available tracks arbitrarily. One example obtained by the above procedures is shown in Fig. 2, where solid squares are power nets and others are signal nets, and the numbers above signal nets are their shielding requirements. Therefore, the total power net number S_t for case 1 is the summation of power nets used in the above six procedures. After some mathematical manipulation and simplification, it is given as $S_t = (\lceil \frac{m_1}{2} \rceil - b_2) + (m_2 + 1) \cdot b_2$. Because S_t equals to the tighter low bound on power net number as S_t^{si}, the so-obtained track assignment solution is optimal with the minimum number of power nets. In case the power pitch is less than the size of the block obtained from step (3), we can treat the pre-layouted $(p_t - 1)$ power nets in step (1) as part of the whole block, and those s1-nets from step (2) can be treated the same way as in step (5). This may reduce the number of power nets further, hence the formula gives a tight upper bound on minimum number of power nets. Other cases can be proved similarly. □

5 GSPR Algorithm

The overall GSPR algorithm is illustrated in Fig. 3. The algorithm is composed of two major parts: (1) power integrity aware multilevel signal routing; (2) power network synthesis and track assignment to satisfy both power and signal integrity constraints. The essence of our GSPR algorithm is to pre-allocate routing resources for power network design during the signal routing stage, while finalize the power network design after signal routing. Below we discuss each part in detail.

5.1 Power Integrity Aware Signal Routing

Routing techniques have been studied in [6] for congestion minimization, in [12, 7] for performance optimization, and in [9, 18] for crosstalk minimization. However, all of these algorithms run directly on a flat routing models, and may suffer the scalability problems for large designs. Moreover, all of these have not consider power integrity yet. In the following, we present a novel multilevel power integrity

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[3]The two edge power nets are counted as one in S_t because of the sharing between adjacent routing regions.

P   1   0   1   P   1   1   P   1   1   P   1   0   1   P   2   P   2   P   1   1   P

Figure 2. A valid track assignment solution with a minimum number of power nets ($p_t = 2$).

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//Power integrity aware multilevel signal routing
Construct routing Graph;
Decompose SSMS nets into two-pin nets;
For each level at the coarsening stage
   For each local critical net N_i
     Pattern routing N_i;
     If not possible, mark it as failed;
For each level at the uncoarsening stage
   For each un-routed/failed net N_i
     Global maze routing N_i;
     Refine routed nets if necessary;
Rip-up and reroute;
//Power network synthesis and track assignment
Global power network synthesis;
For each routing region
   Synthesis local power network;
   Track assignment for power and signal nets;
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Figure 3. The GSPR algorithm overview.

aware signal routing algorithm by utilizing the estimation formula developed in Theorem 1. A typical multilevel routing framework consists of two parts: *coarsening* and *uncoarsening*. In the coarsening process, fine routing tiles are recursively merged into coarser tiles. At each coarsening stage, the routing resources for tiles defined in the current level are estimated from the previous coarsening level. The coarsening process stops when the number of tiles in the coarsest level is less than a certain threshold. The number of levels used in our multilevel framework is dynamically decided according to the benchmark size. The uncoarsening process is in the reverse direction of the coarsening process. The uncoarsening process not only determines tile-to-tile solutions for those un-routed nets left from the coarsening process, but also refines the routed routing solutions if necessary. Due to space limitation, we refer readers to [4, 13] for more detailed discussion about multilevel routing techniques.

According to Fig. 3, we first build the routing graph and decompose SSMS nets into a set of two-pin nets via the minimum spanning tree (MST) algorithm, with each edge of the MST corresponding to a two-pin net. We then start our power integrity aware multilevel routing algorithms from coarsening the finest tile of level 0. At each coarsening level, only critical nets belonging to the current level are routed. Pattern routing [8] is employed in coarsening stage for speed consideration. To choose a pattern among all L-shaped and Z-shaped patterns, we define the

following cost function for each path P_e:

$$cost(P_e) \;=\; \sum_{\forall t \in P_e} \alpha_t \cdot (G_t + S_t - C_t) \qquad (3)$$

where G_t is the number of nets, S_t is the number of power nets, and C_t is R_t's capacity. A dynamic amplification factor (α_t) is used to dynamically adjust the cost function so that we penalize more for a path that tends to cause overflow [6]. The path cost is the sum of edge costs along the route. A path is *overflow* if any edge in P_e has overflow. We choose a pattern that minimizes the cost function (3) without overflow. If we cannot find such a pattern during coarsening, we mark it as *failed net* and it will be refined during the uncoarsening stage. When we compute the cost function (3), we apply the power net estimation equation from Theorem 1 for each routing region. By doing this, we reserve an appropriate number of tracks for power nets during routing, and take into consideration the shielding requirements for both signal shielding and power pitch constraints. Because of this, our routing algorithm is power integrity aware.

The uncoarsening stage refines each local failed nets and all other un-routed nets starting from the coarsest level. For better routability, the routed nets from coarsening procedures can also be modified if such a modification results in less cost. In our current implementation, maze routing algorithm is employed to route local nets belonging to the current level during uncoarsening. The same cost function as in (3) is employed, and we confine the maze search scope within the tile defined by the current level and do not allow overflow.

If after uncoarsening, there are still un-routed nets, rip-up and reroute will be used to find a minimum cost route. Maze routing with the searching space defined in the whole chip is used and we allow overflow at this stage.

5.2 Power Network Synthesis and Track Assignment

The power network synthesis is a hierarchical two-step procedure. We first synthesize a global power network such that there are two power nets along the two edges of every routing region. By synthesizing the global power network this way, we decouple the whole chip power network design problem into a series of independent local power network synthesis problems; and more importantly, we satisfy the pre-condition of Theorem 1, which is used in the cost function for our power integrity aware signal routing. We

then synthesize the local power network and track assignment within each routing region simultaneously. As track assignment is performed within each routing region, and the number of power nets used is no more than what we have reserved, no iteration is required. The optimal local power network and track assignment solution in each routing region is decided by Theorem 1. The algorithmic implementation of this step is the same as the constructive proof procedures of Theorem 1.

6 Experiment Results

The proposed co-design of power network and signal network has been implemented in C++ on Linux. Ten large industrial benchmarks from the ISPD'98/IBM benchmark suite [1] are employed to show the applicability of our algorithm to real designs. The benchmarks are placed by DRAGON [19]. In our current implementation, two preferred routing directions are assumed for all regions, one for horizontal wires and the other for vertical wires. Because there is no shielding information about nets in the original benchmark, we assume that 10% nets are s2-nets and 10% nets are s1-nets for all benchmarks. We assume the required power pitch ($\overline{PGP}$) for all benchmarks is 10 according to a typical industrial design. The characteristics of the benchmarks are shown in Table 1.

Ckts	Net #	Pin #	Grid
IBM01	13056	44266	64×64
IBM02	19291	78171	80×64
IBM03	26104	75710	80×64
IBM04	31328	89591	96×64
IBM05	29647	124438	128×64
IBM06	34935	124399	128×64
IBM07	46885	244369	192×64
IBM08	49228	198180	192×64
IBM09	59454	187872	256×64
IBM10	72760	269000	256×64

Table 1. Benchmark settings .

For comparison purpose, we have also implemented a three-step algorithm (similar to [15]) as follows: route the critical signal nets along with their required shields, synthesize a power network considering shield sharing, and then route the non-critical nets. The track assignment solution in step one is decided in a greedy fashion and explicit power nets are inserted whenever the power-pitch constraint is violated in step two. Because our GSPR algorithm can optimize the shield sharing in each region while the three-step algorithm can not, the latter is expected to consume more power nets than the former. Moreover, because of more shields, step three might obtain a routing solution with many detours. Routing detours is equivalent to more routing bends or longer routing lengths. A bend in a routing path indicates that a via may be introduced during detailed

routing. Vias not only cause congestion for detailed routing, but also deteriorate signal integrity. Therefore, in a routing solution, the smaller the bend number, the better. The same argument holds for the routing length.

We compare the experiment results between our GSPR algorithm and the three-step algorithm in Table 2. Columns 5 and 10 of Table 2 are the final power network area (PG_{area}) given by (1). According to the results, we observe that under the same power and signal integrity constraints, the GSPR algorithm consumes less power network area for all benchmarks than the three-step algorithm. Take benchmark *IBM03* for an example, the three-step algorithm needs 66381 power nets, while the GSPR algorithm only needs 51450 power nets, and the relative saving is 22.5%. On average, GSPR can reduce power net area by 19.4% when compared to the three-step algorithm. This observation is expected, and it convincingly shows us that the GSPR algorithm can utilize the limited routing resource more economically than the three-step algorithm.

We further compare the signal routing quality in terms of the maximum density ($maxDen$), total number of bends ($Bend$), and total number of segments (Seg) (or equivalently, normalized routing length) in Table 2. According to columns 2 and 7 of Table 2, all benchmarks have $maxDen \leq 1$, therefore both algorithms can complete routing without causing overflow. However, when compared to the three-step algorithm, the GSPR algorithm always achieves less number of bends and smaller routing length. The reduction of number of bends and routing length on average are 6.7% and 1.7%, respectively. This observation shows that because of the earlier power net estimation and reservation, the GSPR algorithm can not only reduce the final power net area, but also improve the final routing quality.

We also compare the runtime in seconds in column 6 and 11 of Table 2. According to the runtime results, the GSPR algorithm uses less runtime than the three-step algorithm, and the overall speedup is about 2x.

7 Conclusion and Discussion

We have presented a novel design methodology to the co-design of power and signal networks under integrity constraints. Experiment results using large industrial benchmarks have shown that compared to the best alternative design methodology [15], the proposed method can reduce the power network area by 19.4% on average with better routing quality but use less runtime.

To handle the high complexity resulted from combining the power and signal network designs, we employed the high abstract yet effective power integrity model (power pitch model) and signal integrity model (shielding requirements for nets) [16, 15]. However, we recognize that these

1	2	3	4	5	6	7	8	9	10	11
Test Ckts	Three-step Algorithm					GSPR Algorithm				
	$maxDen$	$Bend\#$	$Seg\#$	PG_{area}	Time	$maxDen$	$Bend\#$	$Seg\#$	PG_{area}	Time
IBM01	0.83	28478	63955	33563	63.2	1.00	26227 (-7.9%)	62255 (-2.7%)	22921 (-31.7%)	37.5
IBM02	0.82	94227	177657	67911	127.1	0.87	87999 (-6.6%)	173693 (-2.2%)	54476 (-19.8%)	73.8
IBM03	0.82	81148	153735	66381	120.1	0.84	75329 (-7.2%)	150995 (-1.8%)	51450 (-22.5%)	68.6
IBM04	0.82	79337	171601	79856	114.6	0.80	72241 (-8.9%)	168387 (-1.9%)	61315 (-23.2%)	66.4
IBM05	0.83	409305	653752	191661	451.6	0.82	381037 (-6.9%)	646994 (-1.0%)	167198 (-12.8%)	246.7
IBM06	0.82	174652	295150	112642	177.1	0.88	163990 (-6.1%)	289980 (-1.8%)	92965 (-17.5%)	102.8
IBM07	0.86	216602	385113	147832	173.2	0.92	202349 (-6.6%)	378045 (-1.8%)	116095 (-21.5%)	102.9
IBM08	0.90	229288	427669	154048	207.9	0.94	214366 (-6.5%)	421483 (-1.4%)	122825 (-20.3%)	123.3
IBM09	0.82	257902	437863	190499	197.3	0.92	241648 (-6.3%)	427519 (-2.4%)	147738 (-22.4%)	115.8
IBM10	0.79	326648	607843	240002	255.7	0.81	305568 (-6.5%)	597621 (-1.7%)	198729 (-17.2%)	150.6
Avg							-6.7%	-1.7%	-19.4%	

Table 2. Experiment results, where numbers in parentheses are reductions of the GSPR algorithm over the three-step algorithm in percentage.

models are too conservative for real designs. For example, to reduce crosstalk, it is not necessary to shield critical nets from the source to the sinks. In the future, we will develop similar high abstract level but more accurate models for both power integrity and signal integrity, and apply them to our multilevel routing framework.

References

[1] C. Alpert. The ISPD98 circuit benchmark suite. In *ISPD*, 1998.

[2] S. Boyd, L. Vandenberghe, A. E. Gamal, and S. Yun. Design of robust global power and ground networks. In *ISPD*, April 2001.

[3] B. Chappell, X. Wang, P. Patra, P. Saxena, J. Vendrell, S. Gupta, S. Varadarajan, W. Gomes, S. Hussain, H. Krishnamurthy, M. Venkateshmurthy, and S. Jain. A system-level solution to domino synthesis with 2 GHz application. In *Proc. IEEE Int. Conf. on Computer Design*, pages 164–171, Sept. 2002.

[4] J. Cong, J. Fang, and Y. Zhang. Multilevel approach to full-chip gridless routing. In *ICCAD*, pages 396–403, 2001.

[5] P. Franzon, S. Simovich, S. Mehrotra, and M. Steer. Macromodels for generating signal integrity and timing management advice for package design. In *Proceedings of Electronic Components and Technology Conference*, pages 523–529, June 1993.

[6] R. Hadsell and P. Madden. Improved global routing through congestion estimation. In *DAC*, 2003.

[7] J. Hu and S. S. Sapatnekar. A timing-constrained algorithm for simultaneous global routing of multiple nets. In *Proc. Int. Conf. on Computer Aided Design*, pages 99–103, 2000.

[8] R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh. Predictable routing. In *ICCAD*, 2000.

[9] R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh. An exact algorithm for coupling-free routing. In *ISPD*, 2001.

[10] J. N. Kozhaya, S. R. Nassif, and F. N. Najm. A multigrid-like technique for power grid analysis. October 2002.

[11] J. Lee, E. Shragowitz, and D. Poli. Bounds on net lengths for high-speed pcbs. In *Proc. Design Automation Conf*, pages 73–76, Nov. 1993.

[12] J. Lillis, C. K. Cheng, T. T. Y. Lin, and C. Y. Ho. New performance driven routing techniques with explicit area/delay tradeoff and simultaneous wire sizing. In *Proc. Design Automation Conf*, pages 395–400, June 1996.

[13] S.-P. Lin and Y.-W. Chang. A novel framework for multilevel routing considering routability and performance. In *ICCAD*, pages 44–50, 2002.

[14] A. Mezhiba and E. Friedman. Inductive properties of high-performance power distribution grids. 10:762–776, Dec. 2002.

[15] P. Saxena and S. Gupta. On integrating power and signal routing for shield count minimization in congested regions. *TCAD*, April 2003.

[16] A. Sinha and S. Chowdhury. Mesh-structured on-chip power/ground: design for minimum inductance and characterization for fast r, l extraction. In *Proc. IEEE Int. Conf. on Custom Integrated Circuits*, pages 461–465, 1999.

[17] H. Su, J. Hu, S. Sapatnekar, and S. Nassif. Congestion-driven codesin of power and signal networks. In *Proc. Design Automation Conf*, pages 64–69, 2002.

[18] H.-P. Tseng, L. Scheffer, and C. Sechen. Timing- and crosstalk-driven area routing. April 2001.

[19] M. Wang, X. Yang, and M. Sarrafzadeh. DRAGON2000: Standard-cell placement tool for large industry circuits. In *ICCAD*, pages 260–263, 2000.

[20] J. Xiong and L. He. Full-chip routing optimization with RLC crosstalk budgeting. In *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, volume 23, pages 1036–1049, March 2004.

[21] T. Xue and E. S. Kuh. Post global routing crosstalk synthesis. *TCAD*, pages 1418–1430, Dec. 1997.

[22] Q. Zhang and M. Nakhla. Signal integrity analysis and optimization of VLSI interconnects using neural network models. In *Proc. IEEE Int. Symp. on Circuits and Systems*, pages 459–462, 1994.

[23] L.-R. Zheng and H. Tenhunen. Effective power and ground distribution scheme for deep submicron high speed VLSI circuits. In *Proc. IEEE Int. Symp. on Circuits and Systems*, volume 1, pages 537–540, may 1999.

[24] H. Zhou and D. F. Wong. Global routing with crosstalk constraints. *TCAD*, pages 1683–1688, November 1999.