Compact Macro-modeling for On-chip RF Passive Components

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Abstract— **For the efficient full-chip circuit simulation and device performance optimization in the RF system-on-a-chip (SoC) design, we propose a novel methodology to generate the compact macro-model for on-chip passive components considering parasitics. Our approach is based on the recently proposed Vector Potential Equivalent Circuit (VPEC) model for the passive sparsification of the inductance matrix, a hierarchical s-domain circuit reduction to generate a reduced driving-point impedance function, and the Brune's one-port network synthesis to realize the impedance function by a low-order RLCM ladder circuit as the compact macro-model. We improved the VPEC model generation via a window-based extraction and achieved extraction speedup by 100x times. We also proposed an efficient scaling scheme during hierarchical model reduction to improve numerical stability of the reduction process. Several industry examples are presented, including transmission lines and spiral inductors. The synthesized lower-order macro-model is accurate up to 10GHz with 1000x times simulation speedup.**

Keywords: **Hierarchical Circuit Reduction, VPEC Model, On-chip RF Passive Modeling**

I. Introduction

As RFIC technology advances with increased operating frequency and decreased feature size, the on-chip passive components like interconnects and spiral inductors become increasingly significant as the active device. It is due to the fact that parasitics of passive components will de-tune RF circuits with the sub-optimized performance [1]. To accurately model the passive component in the high frequency range, a detailed distributed RLCM model, Partial Element Equivalent Circuit (PEEC) [2] is generated by the sufficient discretization and segmentation. It results in a complicated RLCM network with densely coupled inductances. A multiple-ladder RL network to model the skin and proximity effect will further increase the model order [3]. It challenges the circuit level simulation in two aspects: (i) a dense mutual inductively coupled network kills the sparsity and hence slows the simulation time; (ii) a much higher order of circuit matrix lacks the insight of the primary system response. Therefore, we need reduce the complexity of the resulting PEEC model.

In this paper, we proposed a new reduction and realization flow for any distributed high-order RLCM circuits. We first pre-sparsify the dense mutual magnetic couplings by the VPEC (Vector potential Equivalent Circuit) model [4], [5] with the preserved passivity, where we have developed a window-based VPEC model extraction to avoid the expensive full-inversion as in [5]. With the sparsified VPEC model for the RLCM circuit, we further apply the general hierarchical circuit reduction technique (H-reduction for short in the sequel) [6] to generate the driving-point impedance function. To reduce the order of the impedance function and further improve its numerical stability, we have proposed an efficient data scaling scheme during the H-reduction. Finally, a direct circuit synthesis based on the Brune's procedure [7], [8] is applied to realize the driving-point impedance function, and it results in a low-order RLCM ladder circuit as the macro-model.

The remaining part of this paper is organized as follows. In Section II, we discuss the window-based VPEC model sparsification for the dense inductance matrix. In Section III, we review the H-reduction and present a dynamical scaling technique to generate the numerical stable and reduced driving-point impedance function. In Section IV, we present the macro-model realization based on the Brune's one-port network synthesis. In Section V, we present the experimental results for several industry examples, including interconnects and spiral inductors. Finally, we conclude the paper with discussions in Section VI.

II. Inductance Sparsification by Windowed VPEC

Because the inductance is the long-range effect, it kills the sparsity of the circuit matrix. We utilizes the newly developed VPEC model [4], [5] to sparsify the mutual magnetic coupling. Since the direct truncation of the inductance matrix results loss of passivity [9], the VPEC model replaces the coupled inductance network by effective resistance network plus controlled sources, such that the resulted circuit matrix is strictly diagonal dominant, and hence enables the direct truncation-based sparsification without loss of passivity [5]. By pre-removing the dense mutual inductive couplings, we

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obtain a less dense RLCM network and hence can further efficiently apply the H-reduction. Furthermore, because VPEC based sparsification preserves passivity, the sparsified VPEC model is positive real and can be further realized as the passive RLCM circuit.

However, the truncation-based sparsification needs the full inductance matrix (L) inversion ($O(N^3)$), it becomes impractical for both extraction time and memory allocation for the large sized system. Moreover, the directly truncated matrix may be not accurate enough to represent the original full matrix. As shown in [10] that all entries of the L inverse matrix can be approximately reconstructed just from entries of the sub-matrices in L corresponding to the coupling window of the active aggressor. Based on this windowing technique, we develop an efficient VPEC model extraction and sparsification with a reduced computation complexity ($O(Nb^3)$), where b is the size of the window. We illustrate this algorithm as follows.

A. Windowing Extraction

We specify one aggressor m and all victims within a specified window of band b, and then construct a sub-matrix L^m that:

$$L^m_{ij} = \begin{cases} L_{ij} & \text{if (i, j) inside the window;} \\ 0 & \text{if (i, j) outside the window.} \end{cases}$$

We then solve K-element vector $\mathbf{k}^m$ by: $L^m\mathbf{k}^m = \mathbf{i}^m$, where $\mathbf{i}^m$ is the unit current vector of mth aggressor: $\mathbf{i}^m_n = \delta_{mn}$. Finlay, we iterate above procedures for all conductors in turn as active aggressor.

B. Symmetric Positive Define Matrix Construction

We first merge all $\mathbf{k}^m$ vectors into one complete, sparse matrix K' that approximates the inversion of full inductance matrix. To further construct a symmetric positive definite (s.p.d) matrix K', the entry of K' is chosen by:

$$K'_{mn} = K'_{nm} = max(\mathbf{k}^m_n, \mathbf{k}^n_m) \tag{1}$$

C. SPICE Compatible Simulation

We then construct the VPEC model with the sparse approximated K' matrix. The resultant windowed VPEC model can be directly simulated in SPICE. Note that without employing VPEC model, additional efforts have to be paid for K-element based simulation. For example, one option is to make the second inversion [10] of K' matrix to generate a new inductance matrix. However, we find the new inductance matrix may become dense again.

Because this process is only related to the operation of the sub-matrix, the complexity of full inversion is reduced from $O(N^3)$ to $O(Nb^3)$ when b is small. In the experiment, we observed 100x times extraction speedup by using window-based VPEC model when compared to the truncation-based VPEC model.

III. Hierarchical Circuit Reduction with Dynamic Scaling

With pre-sparsified VPEC model for the RLCM circuit, we can efficiently perform the hierarchical circuit reduction. The general s-domain H-reduction can be viewed as a generalized block-level Gaussian elimination algorithm based on MNA formulation [6]. Unlike the existing circuit reduction algorithms [11]–[13], where voltage nodes are eliminated or current branches are merged one at a time. Hierarchical reduction method reduces multiple nodes at a time. Furthermore, this method allows the more general MNA formulation, and performs the reduction on the circuit matrices directly. As a result, it allows the reduction of any SPICE compatible model even with controlled sources, such as the VPEC model.

We first review the H-reduction as follows. Assume the $\mathbf{A}^{II}$ is the sub-matrix to be reduced in matrix $\mathbf{A}$:

$$\begin{bmatrix} \mathbf{A}^{II} & \mathbf{A}^{IB} & 0 \\ \mathbf{A}^{BI} & \mathbf{A}^{BB} & \mathbf{A}^{BR} \\ 0 & \mathbf{A}^{RB} & \mathbf{A}^{RR} \end{bmatrix} \begin{bmatrix} \mathbf{x}^I \\ \mathbf{x}^B \\ \mathbf{x}^R \end{bmatrix} = \begin{bmatrix} \mathbf{b}^I \\ \mathbf{b}^B \\ \mathbf{b}^R \end{bmatrix}. \tag{2}$$

After $\mathbf{A}^{II}$ is reduced, $\mathbf{A}^{BB}$ will become $\mathbf{A}^{BB} - \mathbf{A}^{BI}(\mathbf{A}^{II})^{-1}\mathbf{A}^{IB}$. It was shown in [14], the new element at (u, v) in the modified $\mathbf{A}^{BB}$ will become

$$a^{BB*}_{u,v} = \frac{det(\mathbf{A}^{II}_{(u,v)})}{det(\mathbf{A}^{II})}, \tag{3}$$

where $det(\mathbf{A}^{II}_{(u,v)})$ is the determinant that consists of matrix A^{II} plus row u and column v of the flatten matrix of the whole circuit. Some new admittances in the reduced matrix become rational functions of s after the reduction.

It was shown in [6], the reduction will give the exact s-polynomial (which can be truncated) of the determinant of the original flatten circuit matrix. However, to finally obtain a reduced and realizable output model, it requires the resulted impedance/admittance rational function to be numerically stable. Without scaling, the reduction process will be very sensitive to the numerical magnitudes of the admittances in the given circuit and is not numerical stable for general circuit reduction. In this paper, we propose an efficient dynamic scaling scheme during the H-reduction.

The idea of dynamic scaling is to scale the non-zero coefficient of the smallest order of s in the denominator of $a^{BB*}_{u,v}$ to 1. For instance, for polynomial $\frac{10+2s+0.4s^2}{20+4s+0.8s^2}$, the scaled polynomial is $\frac{0.5+0.1s+0.02s^2}{1+0.2s+0.04s^2}$. A polynomial with the non-zero coefficient of the smallest order of s scaled to 1 is called normalized. For a rational function, normalization means its denominator is normalized. To further guarantee the passivity of the scaled rational function, we finally apply the passivity enforcement via quadratic programming based constrained least squares fitting [15].

There are two significant benefits for such dynamic scaling scheme. First based on Eq.(3), if both coefficients of s^0 in numerator and denominator are not zero (this is the typical case), the magnitude difference between same-order coefficients of the numerator and the denominator polynomial is just the magnitude of the admittance of one device. Since the denominator is normalized, the numerator coefficients magnitude is bounded by the magnitude of the admittance of

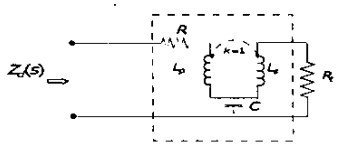

Fig. 1. Brune's driving point synthesis by multiple stage of RLCM ladders (Brune's cycle).

one device. Secondly, the normalization is a self-closure for the polynomial multiplication and division. If polynomial p_1 and p_2 are normalized, so do $p_1 * p_2$ and p_1/p_2 or p_2/p_1. As a result, the addition and multiplication of two normalized rational functions are also normalized. Note that we use Y-DDD (determinant decision digram) technique to efficiently obtain the admittance functions [6], and in DDD graphs only the addition and multiplication of rational functions are required [16]. Therefore, if all the rational admittances of a reduced matrix are normalized, the resulting rational function of the determinant of the reduced matrix is also normalized. Consequently, we find this method can significantly improve the numerical stability during the H-reduction.

IV. Model Realization by Brune's Synthesis

To obtain a low-order compact RLCM model for RF passive components, we further devise a driving-point synthesis procedure extended from circuit admittance realization theory. The driving point synthesis for RLCM circuits was studied earlier by Brune in his significant paper [17], where he pointed out that any positive real (PR) driving-point impedance $Z(s)$ can be realized by a passive multiple-stage RLCM ladder network (see Fig. 1). The Brune's synthesis needs realization of an equivalent coupled inductor to enforce passivity. Bott-Duffin's method [18], on the other hand, avoids the use of the coupled inductor, but a stiff price is paid in the extra number of RLC components and hence is not suitable to be applied for the simple RLCM macro-model realization. Note that implementation of this synthesis procedure primarily depends on the numerical stability of the rational function to be synthesized. In this paper, with the enhanced scaling theory during the H-reduction, we are able to practically implement this procedure for macro-model realization. The synthesized macro-model is a one-port model that can be used for the impedance matching for LNA or central frequency tuning for VCO [19]. However, for the synthesis of the general transfer function, the synthesis two-port or multi-port network needs be applied.

To obtain the simplest form for Brune's synthesis, it needs first to remove all possible pole/zero of $Z(s)$ from $j\omega$-axis to obtain a impedance function with *minimum phase*. This is done by Foster's preamble [7]:(i) removing a zero results a series resonant LC element in parallel with the remainder impedance; and (ii) removing a pole results a parallel resonant LC element in series with the remainder impedance. All these operations preserve the PR property. We then obtain a remainder impedance $Z_0(s)$ for further minimum resistance removing. This minimum impedance can be obtained by searching the minimum of $Re\{Z_0(s)\}$ under a wide range of frequency from dc. Assume its minimum is X_0 at frequency ω_0, and then the RLC elements in one Brune's cycle can be realized [7] by following equations:

$$\begin{aligned} L_1 &= \frac{X_0(\omega_0)}{\omega_0} \\ L_2 &= \frac{X_0'(\omega_0) - L_1}{2} \\ L_3 &= -\frac{L_1 L_2}{L_1 + L_2} \\ C &= \frac{1}{\omega_0^2 L_2} \\ L_p &= L_1 + L_2 \\ L_s &= L_2 + L_3 \\ M &= L_2 \end{aligned} \tag{4}$$

During each cycle, we check the PR property of the remainder impedance $Z_f(s)$ ($Re\{Z_f(s)\} > 0$). After Nc (user specification) cycles we exit the synthesis procedure with a remainder impedance $Z_f(s)$, and terminate the procedure by adding a termination resistor R_t:

$$R_t = Z_f(s)|_{s\to 0} \tag{5}$$

Generally, the order a driving-point rational function decreases 2 degrees during every synthesis cycle with increasing 1 order of a RLCM ladder. By increasing ladder stage number Nc, we increase the model order and capture more poles.

V. Experimental Results

In this section, we present experimental results. The accuracy and efficiency of the reduction procedure is illustrated through various industrial examples, including interconnects and spiral inductors. We first present the extraction speedup of windowed VPEC model compared to the full inversion based approach. Then we compare waveforms predicted by our synthesized macro-model with the original circuit. In the end, we give the simulation efficiency comparisons scaled with different circuit sizes.

We assume the copper ($\rho = 1.7 \times 10^{-8}\Omega \cdot m$) metal. The partial inductance is extracted by FastHenry [20], where each wire segment is modeled by one filament, and coupling between any pair of segments (including segments in a same line) is considered. Hence a much higher order of distributed RLCM PEEC model is generated. Moreover, volume filaments decomposition is applied to take into account the skin and proximity effects. The capacitance is extracted by lookup table [21]. Because capacitive coupling is short-range effect, only adjacent couplings are considered. By applying an *ac* current source at one input port, we observe the near-end response. All circuits are simulated by SPICE3 on Linux workstation with dual 1GHz P-III CPUs and 2G memory.

We first compare the extraction efficiency between windowing and truncating based VPEC model for a number of wire

1	2	3	4	5	6	7	8
Circuits	#Nodes	Sparse Ratio	Reduction Ratio	Overhead Time(s)	Simulation Time(s) w/o Redu.	Simulation Time(s) w Redu.	Simulation Speedup
ckt1	21	No SP	55.2%	0.12	0.05	0.04	1.2X
ckt2	180	33.3%	90.1%	0.77	0.17	0.04	4.1X
ckt3	3460	77.5%	94.2%	8.6	6.13	0.10	58.3X
ckt4	20650	90.5%	98.1%	21.1	99.14	0.11	901X
ckt5	81900	95.2%	99.7%	23.7	2241.12	0.52	4309X

TABLE I

COMPARISON OF SIMULATION EFFICIENCY BETWEEN THE ORIGINAL AND SYNTHESIZED MODEL.

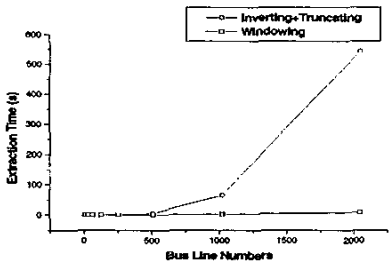

Fig. 2. Extraction time comparisons of wire parasitics using truncating and windowing.

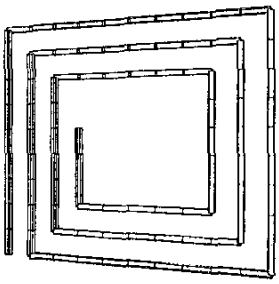

Fig. 3. Discretized spiral inductor for generation of distributed RLCM PEEC/VPEC model.

parasitics up to 2000-bit as in Fig.2. The truncating approach is based on a truncating size (N_W, N_L) = (8, 1) [5], and the window size for windowing is b = 8 to achieve the similar sparsification ratio. The extraction time for truncating based approach includes full inversion and truncating. We find that when the scale of interconnects is small (below 128-bit), the windowing extraction is actually as efficient as truncating approach. But when the scale of wire is as larger as 1000-bit, we find the windowing based extraction is much faster than the truncating approach, and a 100X times speedup is observed for the 2048-bit wires (543.1s vs. 8.6s). Therefore it is more efficient to apply winnowing based VPEC model extraction for large scale RF passive components.

We then present the result of a 3-turn spiral inductor with 92 segments. A distributed RLCM model is generated from PEEC/VPEC extraction as shown in Fig. 3. In Fig. 4 , the frequency domain response of the synthesized macro-model (see Fig. 1) agrees well with original circuit up to 10GHz. We note that the synthesized one-port macro-model can be used to efficiently predict the critical performance parameters of spiral inductor, such as the ω_T and Q factor [19]. The

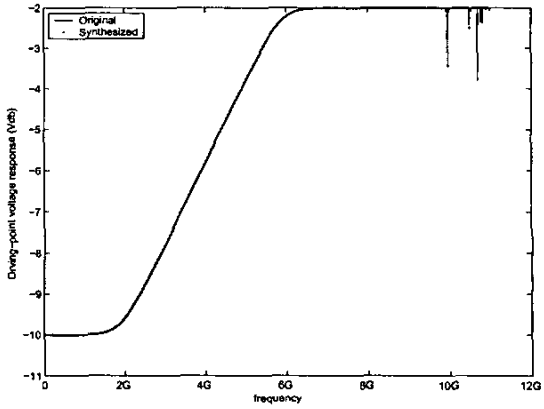

Fig. 4. Frequency-domain driving-point response comparison between original and synthesized models for a 92-segmented spiral inductor.

substrate loss can be included during the distributed RLCM model generation and is under future study.

Table I shows the efficiency of the model reduction procedure as measured in CPU runtime vs. the corresponding sparsification and reduction percentage. Several different sized industry circuits are used. The synthesized models are RLCM ladders up to 3 stages. It compares the simulation time of PEEC input circuits without reduction with that of reduced and realized VPEC output circuits. Simulations of both original circuits and reduced circuits are performed by SPICE3 in frequency domain. As seen from the table, significant speedup (up to 4000X) is obtained for synthesized low-order macro-modeling simulation with little overhead paid in circuit sparsification, reduction and realization. Since macro-model generation is only performed once, their overhead time are not included in the simulation time during the comparison with SPICE3.

VI. CONCLUSIONS AND DISCUSSIONS

The proposed compact modeling methodology leverages the novel circuit reduction [6] and electromagnetic modeling [5] with the well-developed network synthesis [7] which is the potential complexity reduction approach for the design and simulation of on-chip RF passives when considering parasitics Our experimental results show the low-order macro-model can well capture the original system frequency-response up to 10GHz and with 1000x times simulation speedup.

We synthesize the low-order RLCM ladders as one-port macro-models for RF passive components. Such model can not capture time-of-flight effects in ultra-high frequency range. This is the primary error source. Further in this paper, we only synthesize the macro-model for the one-port driving-point impedance. For more general macro-model realization, we also intend to study the synthesis of two-port transfer function in a similar flow.

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