A Wideband Hierarchical Circuit Reduction for Massively Coupled Interconnects

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***Abstract*— We develop a realizable circuit reduction to generate the interconnect macro-model for parasitic estimation in wideband applications. The inductance is represented by VPEC (vector potential equivalent circuit) model, which not only enables the passive sparsification but also gives correct low-frequency response, whereas the recent $Y-\Delta$ circuit reduction intrinsically has inaccurate dc value and low-frequency response due to nodal-susceptance formulation. Applying hierarchical circuit-reduction enhanced by multi-point expansions, we can obtain an accurate high-order impedance function to capture the high-frequency response. The impedance function is further enforced passivity by convex programming, and realized by a Foster's synthesis. Experiments show that our method is as accurate as PRIMA in high frequency range, but leads to a realized circuit model with up to 10X times less complexity and up to 8X smaller simulation time. In addition, under the same reduction ratio, its error margin is less than that for the time-constant based reduction in both time-domain and frequency-domain simulations.**

I. Introduction

As VLSI technology advances with increased operating frequency and decreased feature size, parasitics from on-chip interconnects and off-chip packagings will de-tune the performance of high-speed circuits in terms of slew rate, phase margin and bandwidth. To accurately model parasitics in a wide frequency range, Partial Element Equivalent Circuit (PEEC) [1] in terms of RLCM (M here stands for mutual inductance) circuits are generated from discretized conductors by volume decomposition according to skin-depth and longitudinal segmentation according to wavelength at the maxim operating frequency. Because the PEEC model typically results in a large RLCM circuit with massively coupled partial inductance matrix L, it challenges the circuit level simulation in two aspects: (i) a dense inductively coupled matrix sacrifices the sparsity of circuit matrix; (ii) the model order of the circuit matrix is too high. It slows down the simulation and even makes the simulation infeasible. Therefore, inductance sparsification and model order reduction are two necessary approaches to reduce the complexity.

Since directly truncating small off-diagonal elements of inductance matrix results in loss of passivity [4], there are several passivity-enforced sparsification methods proposed in the literature [5], [6]. Due to the fact that inversion of partial inductance matrix is strictly diagonal dominant, the susceptance (K-element) ($S = L^{-1}$) based sparsification [5] becomes an efficient way to achieve the passive sparsification of the dense inductance matrix. Nevertheless, the order of the circuit matrix can be still large after the sparsification. To further reduce the model complexity, the sub-space projection based model-order-reduction (MOR) techniques [7] are applied to generate a low-order approximation of the original circuit via implicit moment matching [8]. Note that the resulting model for time-domain simulation is a dense state matrix [7]. To achieve a realizable reduction in the flow of RLC-in and RLC-out, the circuit-reduction based on Gaussian variable-elimination is recently proposed as an alternative to the projection-MOR. In [9], time-constant based criteria are used for the first-order realizable circuit-reduction. Although those criteria guarantee the realizability, the reduced model usually loses accuracy when reduction ratio is beyond the criteria guaranteed region. To obtain the higher order realizable circuit-reduction for a higher accuracy, a generalized $Y-\Delta$ transformation based method is proposed in [10], including two steps: (i) a general $Y-\Delta$ transformation by nodal-voltage variable elimination to obtain one-port admittance rational function; and (ii) a circuit-synthesis of admittance function. This method keeps terms of the rational function up to a desired order, and finally realizes the rational function by Brune's one-port synthesis [11] via a geometrical programming process.

However, $Y-\Delta$ transformation based circuit-reduction is restricted to the nodal analysis (NA) formulation as it works on the circuit topology directly. As a result, it needs to construct the nodal-susceptance (instead of inductance). As will be shown in Section II, susceptance under NA formulation creates unwanted dc paths and leads to wrong dc values and inaccurate low-frequency responses. It prevents this method from being applied to interconnects in wideband applications, because the accurate dc information is important to determine the operating point to further perform the correct and stable ac analysis [12]. Moreover, there are two types of numerical errors in this method: (i) common factor cancellation; and (ii) truncation of high-order terms. It can lead to the numerical instability for the resulting admittance function. In this paper, we propose a novel realizable circuit-reduction flow that can preserve the correct dc information and enforce the passivity of the reduction. This macro-modeling flow consists of following steps:

1) With the extracted PEEC model, we generate the sparsified vector potential equivalent circuit (VPEC) model via windowing as: (i) VPEC model enables the passive sparsification and hence accelerates the followed circuit-reduction; (ii) VPEC model has the correct frequency response in the entire frequency region compared to the PEEC model since it is derived from first principles and is equivalent to the PEEC model;
2) We further apply the newly developed hierarchical circuit-reduction method [13] with two enhancements: (i) the multi-point expansion to obtain the accurate yet stable high-order impedance function; and (ii) the convex programming to further enforce the passivity of the resulting impedance function.
3) Finally, we show how this accurate and passive impedance function can be expressed in the generalized Foster's canonical form and hence can be efficiently realized with RLCG elements.

The rest part of this paper is organized below. In Section II, we discuss the inductance formulation in circuit-reduction, and show that nodal-susceptance formulation in $Y-\Delta$ based reduction leads to inaccurate dc and low-frequency response, but the VPEC based formulation obtains frequency response as accurately as the PEEC model. In Section III, we use an enhanced hierarchical circuit-reduction to further reduce VPEC model, and present a generalized Foster's synthesis to realize the reduced impedance function. In Section IV, we show experimental comparisons with the PEEC model, time-constant based circuit-reduction, projection-based reduction by PRIMA and our approach in terms of the accuracy and realized model size. Finally, we conclude in Section V.

II. Inductance Formulation for Circuit-Reduction

In this section, we first briefly review the circuit-reduction, and then discuss the inductance formulation for circuit-reduction by nodal-susceptance and by vector potential equivalent circuit, respectively. We will show that the inductance formulation by nodal-susceptance is not physically equivalent to inductance as unreal dc paths are created.

For a RLCM circuit, when we assume independent current sources at external ports, the circuit matrix by MNA (modified nodal analysis) formulation in s-domain is

$$\mathcal{G}x + s\mathcal{C}x = Bi(s), \qquad v(s) = B^T x \tag{1}$$

where x, v, i are the state variable, output voltage and input current vectors, and $\mathcal{G}, \mathcal{C}, B$ are state and input-output matrices, respectively. (1) can be further written as:

$$\begin{bmatrix} G & A_l^T \\ -A_l & 0 \end{bmatrix} \begin{bmatrix} v_n \\ i_l \end{bmatrix} + s \begin{bmatrix} C & 0 \\ 0 & sL \end{bmatrix} \begin{bmatrix} v_n \\ i_l \end{bmatrix} = \begin{bmatrix} Bi(s) \\ 0 \end{bmatrix}, \tag{2}$$

where G and C are admittance matrices for resistances and capacitances, L is the inductance matrix, which includes mutual inductance, v_n is a vector of nodal voltages , i_l is a branch current vector of the inductors, and A_l is the adjacency matrix for all inductors.

The *circuit-reduction* means applying the Gaussian elimination for state variables like nodal voltage v_n and branch current i_l. If we initially reduce the branch current vector i_l, we actually result in a state equation only with nodal voltage variables

$$[G + sC + \frac{1}{s} A_l S A_l^T][v_n] = [Bi(s)]. \tag{3}$$

This is exactly the nodal analysis (NA) formulation, where $S = L^{-1}$ is the susceptance [16], and $\Gamma = \frac{1}{s} A_l S A_l^T$ is the admittance form for the mutual inductance under NA. The circuit-reduction by further eliminating the nodal voltage-variable v_n is exactly the $Y-\Delta$ transformation in [10]. However, the elimination of i_l (from (2) to (3)) will create unreal dc paths in the resulting nodal-susceptance circuit as shown below.

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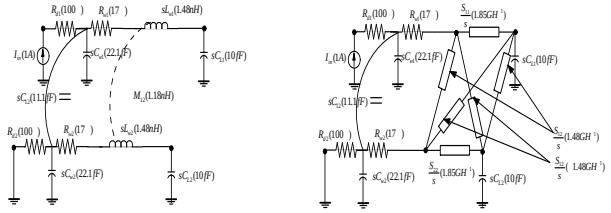

(a) 2-bit PEEC circuit

(b) 2-bit nodal-susceptance circuit
(nodal susceptance can be realized by inductor)

Fig. 1. An example of coupled 2-bit RLCM circuit. (a) is the circuit under PEEC model; (b) is the 6-nodal-susceptance circuit under NA.

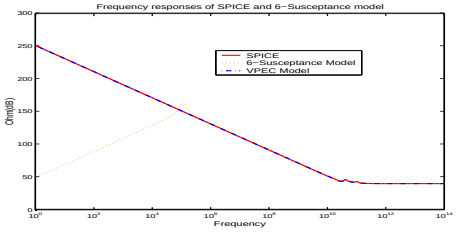

Fig. 2. Frequency responses of PEEC model in SPICE, susceptance under NA and VPEC models for the 2-bit bus.

A. Inductance Formulation by Nodal-Susceptance

We use a 2-bit interconnect example shown in Fig. 1 for the simplicity of illustration. The nodal-voltage equation of susceptance (3) at four voltage nodes (A,B,C,D) is

$$\begin{aligned}
&\frac{S_{11}}{s}V_A - \frac{S_{11}}{s}V_B + \frac{S_{21}}{s}V_C - \frac{S_{21}}{s}V_D = I_1\\
&-\frac{S_{11}}{s}V_A + \frac{S_{11}}{s}V_B - \frac{S_{12}}{s}V_C + \frac{S_{12}}{s}V_D = -I_1\\
&\frac{S_{12}}{s}V_A - \frac{S_{12}}{s}V_B + \frac{S_{22}}{s}V_C - \frac{S_{22}}{s}V_D = I_2\\
&-\frac{S_{12}}{s}V_A + \frac{S_{12}}{s}V_B - \frac{S_{22}}{s}V_C + \frac{S_{22}}{s}V_D = -I_2
\end{aligned} \tag{4}$$

As shown Fig. 1 (b), it is mathematically equivalent to stamp six individual self-susceptance elements into the admittance matrix [10]. Clearly, because S_{ij}/s approaches to an infinite admittance value (thus 0-impedance as short circuit) when $s = 0$, there exist four *unreal* dc-paths between nodes (A,B,C,D), which do not exist before. As a result, it leads to the inaccurate impedance function at dc and low-frequency region.

We compute the exact driving-point impedance rational functions (expanded at $s \sim 0$) using inductance under MNA and nodal-susceptance under NA, respectively. As shown in Fig. 2, the impedance function $Z_{NA}(s)$ gives the exact the response as SPICE does. It becomes a capacitor with value about $43fF$ when s approaches to zero, and becomes a resistor with value 100 ohms when s approaches to infinite. If we use the 6-nodal-susceptance in NA, $Z_{NA}(s)$ gives the exact response as SPICE does in the high-frequency range, but the response is incorrect in the low-frequency range. When s approaches zero, the actual driving-point impedance in Fig.1 (a) should be dominated by three capacitor with total value $43fF$. However, for Fig.1 (b) at dc, the driving-point impedance becomes a resistor with total value 234 ohms due to the unreal dc path. As a result, the circuit-reduction with nodal-susceptance formulation can leads to incorrect low-frequency response in general.

B. Inductance Formulation by VPEC Model

Because the inductance formulation by the nodal-susceptance leads to inaccurate low-frequency response, it is not suitable to generate the reduced interconnect model for wideband applications. On the other hand, directly handling dense mutual inductance in the MNA formulation as in [9] will be computationally expensive. As shown in [6], the inductive effects under the VPEC model (using effective resistances) not only is physically equivalent to the PEEC model, but also enables passive sparsification to accelerate the followed circuit-reduction.

One significant difference between VPEC and nodal-susceptance models for mutual inductance is that VPEC is a physically equivalent circuit model that can exactly represent the original system. As shown in Fig.3, this model consists of electrical circuit (PEEC resistance

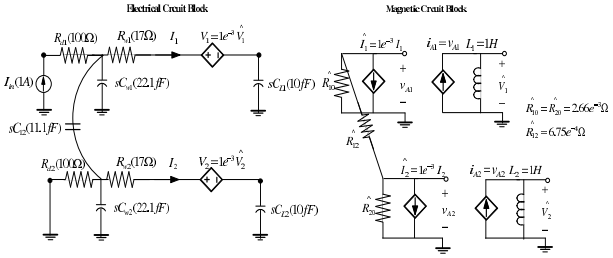

Fig. 3. The VPEC model for the 2-bit example in Fig. 1.

and capacitance) and magnetic circuit (VPEC effective resistance and controlled source), and includes following components: (1) the wire resistance (R_i) and capacitance (C_i) same as those in the PEEC model; (2) a dummy voltage source to sense electrical current I_i to control $\hat{I}_i$ with coefficient equal to filament length $l = 1000um$; (3) a voltage controlled current source to relate $\hat{V}_i$ and $\hat{I}_i$ with gain $g = 1$; (4) an electrical voltage source V_i controlled by $\hat{V}_i$ with coefficient equal to filament length $l = 1000um$; (5) effective resistances including ground $\hat{R}_{i0}$ and coupling $\hat{R}_{ij}$ to consider the strength of inductances; (6) a unit inductance L_i to: (i) take into account of the time derivative of A_i; and (ii) preserve the magnetic energy from the electronic circuit. The effective resistances are determined from:

$$\hat{R}_{ij} = -\frac{1}{l^2 L_{ij}^{-1}}, \qquad \hat{R}_{i0} = \frac{1}{l^2 L_{ii}^{-1} + \sum_{j\neq i} l^2 L_{ij}^{-1}} \tag{5}$$

Clearly, this SPICE compatible implementation does not introduce the unreal dc paths at $s = 0$ as does by the nodal-susceptance. Fig. 2 shows the response of VPEC model for the 2-bit circuit, which is identical to SPICE for the entire frequency range.

To further improve the sparsified VPEC model extraction without the full inversion as in [6], we extend a windowing technique [16]. It reduces the computation complexity to $(O(Nb^3))$, where b is the size of the window. Note that although VPEC model enables efficient inductance sparsification, the order of circuit matrix is still high. Moreover, its SPICE compatible model contains controlled sources such that: (1) the state matrix $A(s) = s\mathcal{C} + \mathcal{G}$ does not satisfy the congrument transformation condition: $A^T + A > 0$ [7] and hence PRIMA based model reduction can not reduce the VPEC model; (2) the existing realizable circuit-reduction approaches [9], [10] can not reduce VPEC model as well as they directly work on the circuit topology. In the following, we present an improved hierarchical circuit-reduction to further reduce the order of VPEC model.

III. Enhanced Hierarchical Circuit-Reduction

We discuss the recently developed s-domain hierarchical circuit-reduction algorithm (H-reduction) [13] to reduce the VPEC model in this part . For (1), we define $A(s) = s\mathcal{C}+\mathcal{G}$, and assume the impulse current source at one port. Hence (1) becomes $Ax = b$. We further distinguish x into three types: x^E for variables to be eliminated, x^P for variables to be preserved, and x^B for boundary variables in between x^E and x^P. Then (1) is rewritten as

$$\begin{bmatrix} A^{EE} & A^{EB} & 0 \\ A^{BE} & A^{BB} & A^{BP} \\ 0 & A^{PB} & A^{PP} \end{bmatrix} \begin{bmatrix} x^E \\ x^B \\ x^P \end{bmatrix} = \begin{bmatrix} b^E \\ b^B \\ b^P \end{bmatrix} \tag{6}$$

By applying the block-level Gaussian elimination [13] to eliminate variables x^E, we have the following reduced system equation:

$$\begin{bmatrix} A^{BB} - A^{BE}(A^{EE})^{-1}A^{EB} & A^{BP} \\ A^{PB} & A^{PP} \end{bmatrix} \begin{bmatrix} x^B \\ x^P \end{bmatrix} = \begin{bmatrix} b^B - A^{BE}(A^{EE})^{-1}b^E \\ b^R \end{bmatrix} \tag{7}$$

For simplicity of illustration, we define $\widetilde{x}$, $\widetilde{b}$ and $\widetilde{A}$ for the reduced system, i.e., (7) becomes $\widetilde{A}\widetilde{x} = \widetilde{b}$. Furthermore, the transfer function of the reduced system is

$$\widetilde{v}(s) = Z(s)\widetilde{i}(s), \qquad Z(s) = Z_0 + sZ_\infty + \widetilde{b}^T\widetilde{A}^{-1}\widetilde{b} \tag{8}$$

where Z_0, Z_∞ are the dc and ultra-high frequency impedance. It becomes the driving-point impedance function when only one port is remained. For the multi-input multi-output system, the transfer function becomes an impedance matrix:

$$Z(s) = Z_0 + sZ_\infty + \widetilde{B}^T\widetilde{A}^{-1}\widetilde{B}, \tag{9}$$

where $\widetilde{b}$ becomes the reduced input-output matrix $\widetilde{B}$.

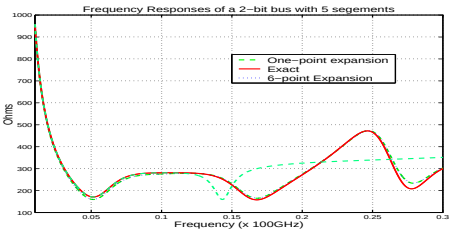

Fig. 4. Driving-point frequency response of a 2-bit bus with 5 segments.

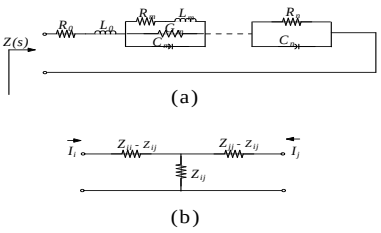

Fig. 5. Foster's Canonical form based equivalent circuit synthesized.

Clearly, since this method directly operates on the MNA state equation, the state variable in x can be easily eliminated even when the state matrix A contains controlled sources. Furthermore, compared to the existing circuit-reduction algorithms [9], [10], this method achieves two advantages: (1) the elimination is in a fashion of divide-conquer and (2) multiple voltage variables and current variables can be simultaneously eliminated. Therefore, the reduction time is much reduced for large scale circuits as shown in [13];

By further applying the Y-DDD (Determinant Decision Diagram) technique, H-reduction can find the cancellation-free impedance function, which removes the common-factor cancellation introduced numerical error. However, this method has the similar truncation error as in [10], which prevents it from getting the high order terms. It can be mitigated by following two enhancements: multi-point expansion and passivity enforcement.

A. Multi-point Expansion and Explicit Waveform Matching

We obtain the impedance function (9) by multiple expansions carried along either real axis or imaginary, where we use a novel frequency-domain waveform matching algorithm to search for the dominant poles at different expansion points instead of the binary search in [14]. The new waveform matching algorithm explicitly matches the frequency waveforms of the reduced rational functions with the exact one in each frequency range starting from each expansion point. This method takes the advantage of the fact that most of dominant poles of high-frequency passive circuits are complex poles. Therefore, the contributions of complex poles become the largest at frequency f_i when its imaginary part is $2\pi f_i$. As a result, we only select all the poles whose imaginary part fall into $[2\pi f_i, 2\pi f_{i+1}]$, where in the frequency range $[f_i, f_{i+1}]$, both the approximated and exact functions match to a user specified error bound.

We find that with multi-point expansion in a desired frequency range, it can capture the dominant poles that are near to each expansion points. Its accuracy is much better than the single-point expansion when the interested frequency range is wide such that lots of poles are far away form the single expansion point s_0. Fig. 4 shows a frequency response of the driving-point impedance for 2-bit bus with 5 segment on each bit. The scope of the frequency range is from dc to 30GHz. We compare the results by one-point ($s = 0$), 6-point expansion and the exact response. Both impedance functions have 10 poles, but the accuracy is quite different, where 6-point expansions can capture the high-frequency response much better than the one-point expansion.

B. Passivity Enforcement

During the multi-point expansion, we can capture stable poles during the pole searching. However, its passivity still needs guaranteed, i.e. $Z(s)$ needs to be a positive real function. The necessary and sufficient condition [17] for $Z(s)$ to be positive real is when there exists a symmetric positive definite (s.p.d.) matrix K such that:

$$\begin{bmatrix} -\mathcal{A}^T K - K\mathcal{A} & -K\mathcal{B} + \mathcal{B} \\ -\mathcal{B}^T K + \mathcal{B}^T & Z_0 + Z_0^T \end{bmatrix} \geq 0 \qquad (10)$$

where $\mathcal{A} = \mathcal{C}^{-1}\mathcal{G}$, and $\mathcal{B} = \mathcal{C}^{-1}B$. As shown in [18], to obtain a passivity enforced $Z'(s)$ we can formulate a convex programming problem to enforce the global passivity by optimizing matrices ($\mathcal{B}$, K, Z_0, Z_∞) at N frequency points s_k ($k = 1, 2, ..., N$)

$$\begin{aligned} &min: t(\mathcal{B}, K, Z_0, Z_\infty) \\ &sub: \\ &(1) \quad Eq.(10) \\ &(2) \quad K, Z_0, Z_\infty \geq 0 \\ &(3) \quad \sum_{k=1}^{N} w_{k,ij} ||Z'_{ij}(s_k) - Z_{ij}(s_k)||_2^2 < t_{ij} \end{aligned} \qquad (11)$$

These constraint-formulations ensure the global positive-realness of $Z(s)$ and are as restrictive as necessary.

C. Realization via Impedance Synthesis

With a order reduced and passivity enforced impedance function, we further discuss how to generate realized macro-models for both frequency/time domain simulation by a generalized Foster's synthesis [11]. We first show how to synthesize the one-port model from the driving-point impedance rational function $Z(s)$, where $Z(s)$ can be rewritten in the Foster's canonical form, i.e., a partial fraction form with N conjugate-poles p_n and M real-poles p_m:

$$Z(s) = Z_0 + sZ_\infty + \sum_{m=1}^{M} \frac{a_m}{s - p_m} + \sum_{n=1}^{N} \left(\frac{a_n}{s - p_n} + \frac{a_n^*}{s - p_n^*}\right) \qquad (12)$$

It can be synthesized as an equivalent circuit in Fig. 5 (a) with following relations to determine R,L,C,G elements:

$$\begin{aligned} &R_0 = Z_0, \qquad L_0 = Z_\infty; \\ &C_m = \frac{1}{a_m}, \qquad R_m = -\frac{1}{C_m p_m}; \\ &C_n = \frac{1}{2Re\{a_n\}}, \qquad G_n = C_n(X_n - 2Re\{p_n\}); \\ &L_n = \frac{1}{C_n|p_n|^2 + G_n X_n}, \qquad R_n = -L_n X_n. \end{aligned} \qquad (13)$$

where $X_n = \frac{Re\{a_n p_n^*\}}{Re\{a_n\}}$.

Using an additional T-transformation, this one-port synthesis can be easily extended to the multi-port synthesis. As shown in Fig. 5 (b) for a two-port impedance matrix, each branch impedance is realized according to (13). Further different from the approach in [15], (i) we obtain a passive and accurate rational function without the vector-fitting, where the vector-fitting can not guarantee the global passivity; and (ii) we do not need over-constrained passivity conditions, where over-constrained passivity conditions in [15] enforce the passivity, but can lose the accuracy [18]. Therefore, our synthesized circuit is passive and accurate.

IV. Experimental Results

In this section, we compare our realizable circuit-reduction with time-constant based circuit-reduction [9] and projection-based reduction PRIMA in both frequency and time domains, and study the accuracy, realization efficiency and scalability of our approach. We use coupled bus together with non-linear drivers as our examples. We assume the copper ($\rho = 1.7 \times 10^{-8}\Omega \cdot m$) for metal and low-$k$ dielectric ($\epsilon = 2.0$). The conductor is volume-discretized according to the skin-depth and longitudinal segmented by one tenth of wavelength. The capacitance is extracted by FastCap [2] and only adjacent capacitive coupling. The partial inductance is extracted by FastHenry at 30GHz [3]. The inductive coupling between any pair of segments is considered. We then generate the distributed PEEC model by π-type of RLCM topology to connect each segment, and further obtain the full VPEC model via LU-factorization based inversion [6] or the sparse VPEC via a windowing. The reduction starts from VPEC model for our method but from PEEC model for the other two reductions. Moreover, the reduced state-matrix from PRIMA is realized by controlled sources [19] for SPICE compatible simulation. All circuits are simulated by SPICE3 on Linux workstation with 1GHz P-III dual-CPU and 2G memory.

A. Time and Frequency Domain Comparison

We first compare waveforms of models with different order at the far-end of the driver-output by a 1V transient input for a 2-bit bus with 20 segments connected to nonlinear drivers. The original PEEC model contains 42 resistors, 63 capacitors, 40 self-inductors, and 760 mutual-inductors. The reduced model is realized via a two-port Foster's synthesis. The waveform is compared in Fig. 6 for two reduced models with different orders and the original PEEC model. When we use 25 poles to generate the reduced model, we obtain

TABLE I
SIMULATION EFFICIENCY COMPARISON BETWEEN ORIGINAL AND SYNTHESIZED MODEL.

1	2	3	4	5	6	7	8	9	10	11	12	13	14
Circuits	#Elements	#Poles	Simu-time(s)				Model-size(Kb)				Delay-error (%)		
			H-redu	time-const.	Prima	Original	H-redu	time-const.	Prima	Original	H-redu	time-const.	Prima
ckt1	84	10	0.15	0.12	0.50	0.51	0.85	0.86	3.51	3.52	-0.16%	-0.86%	-0.15%
ckt2	258	10	0.15	0.15	0.92	5.31	0.85	0.86	3.51	11.23	-0.24%	-1.12%	-0.22%
ckt3	905	25	0.32	0.43	2.25	19.51	1.68	1.70	19.8	41.1	-0.41%	-4.43%	-0.37%
ckt4	5255	30	0.52	0.89	3.13	661.46	1.92	2.23	28.2	243.6	-0.62%	-6.83%	-0.58%
ckt5	20505	30	0.52	1.08	5.98	1356.66	1.92	2.53	28.2	957.9	-1.04%	-12.91%	-0.83%

a realized model with 12-stage RLCG elements (total 45 circuit-elements) and 61X (19.51s vs. 0.32s) transient simulation speedup, where the two waveforms are visually identical. When using 10 poles, we obtain total 25-elements in the reduced model but 130X simulation speedup, where the waveform error is 0.3ns in terms of delay but 0.1mV in terms of slew rate. Clearly, the waveform with 25th-order macro-model is the choice in terms of both accuracy and speedup, and such a high-order model is enabled by the multi-point expansion.

Fig. 7 further shows the driving-point responses in frequency-domain for the above example. When we also use 25 poles to generate reduced model by PRIMA, we find that accuracies of two reduced models are very close to the original circuit up to 40GHz, but the size of the compatible one-port model from PRIMA by controlled sources is 12X larger in terms of model size than our realized model and 8X slower in terms of simulation time (2.4s vs 0.3s). On the other hand, under the same reduction-ratio, we find the time-constant based reduction is not accurate beyond 5GHz.

B. Scalability of Reduced Models

We further present the scalability of our reduced model in Table I by time-domain transient simulations for following aspects: (i) runtime of simulation; (ii) realization efficiency (realized model size); and (iii) accuracy in terms of delay. We compare reduced circuits from H-reduction and PRIMA by the same reduction order, i.e. the same number of poles for approximation. The reduced model using time-constant based reduction is obtained with similar model size as H-reduction. Firstly, we find our realized RLCG circuit model size is 10X smaller on average than the SPICE compatible circuit from PRIMA. Therefore, similar simulation speedup (8X) is observed when we run both circuits in SPICE3. When we further compare the simulation time of our reduced models with the PEEC circuits, a significant speedup (up to 2712X for ckt5) is obtained. Furthermore, the waveform accuracy in terms of delay is given in Column 12-14. The reduced models are very accurate with worst case delay error being -1.04% even with 478X (957.9Kb vs. 1.92Kb) reduction ratio in terms of model size. But for the same reduction ratio as our reduction, we find the time-constant based reduction introduces large errors (up to 12.91%) because too many nodes are eliminated and the reduction criteria cannot be satisfied.

Note that the sparsification in VPEC model can dramatically reduce the number of mutual inductive couplings, and maintain the similar accuracy [6]. As a result, it reduces the reduction cost for the large circuit. For example, in the case of ckt5 (the largest one) in Table I, we obtain a 97.5% sparsification from 19,900 to 498 mutual-inductors. Due to this sparsification, it reduces the H-reduction time by 10X (365.4s to 47.8s), and is much smaller than the reduction time (512.5s) of time-constant based reduction.

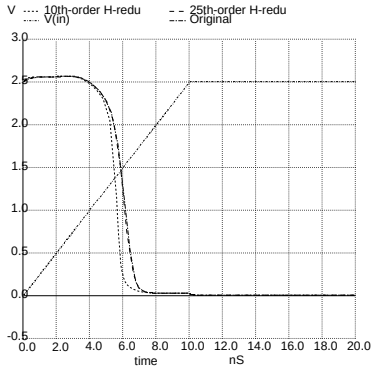

Fig. 6. The SPICE3 time-domain waveform comparisons for 2-bit bus with 20 segments, between the original PEEC model, and realized models with 10th-order and 25th-order by H-reduction.

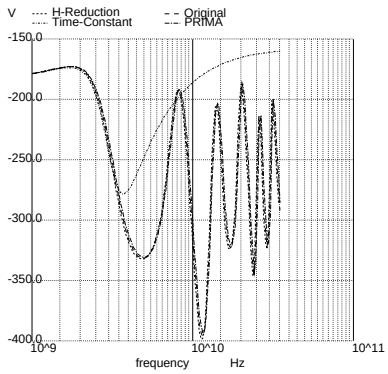

Fig. 7. The SPICE3 frequency-domain waveform comparisons for 2-bit bus with 20 segments, between the original PEEC model, realized models by time-constant based reduction, 25th-order H-reduction, and 25th-order PRIMA.

V. CONCLUSIONS AND DISCUSSIONS

In this paper, we present a novel circuit-reduction flow via physical VPEC model for inductance, an enhanced hierarchical circuit-reduction to generate high-order accurate and passive impedance function, and an efficient Foster's canonical synthesis. Our experiment results show that the new circuit-reduction flow has more accurate low-frequency response than the $Y-\Delta$ transformation [10], and also has the better accuracy in the high-frequency range than the time-constant based reductions [9]. Furthermore, it has similar accuracy as projection based model order reduction (PRIMA), but with a much smaller realized RLCM circuit.

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