Wideband Modeling of RF/Analog Circuits via Hierarchical Multi-Point Model Order Reduction *

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ABSTRACT

This paper proposes a novel wideband modeling technique for high-performance RF passives and linear(ized) analog circuits. The new method is based on a recently proposed s-domain hierarchical modeling and analysis method [27]. Theoretically, we show that the s-domain hierarchical reduction is equivalent to implicit moment matching around $s = 0$, and that the existing hierarchical reduction method by one-point expansion is numerically stable for general tree-structured circuits. Practically, we propose a hierarchical multi-point reduction scheme for high-fidelity, wideband modeling of general passive or active linear circuits. A novel explicit waveform matching algorithm is proposed for searching the dominant poles and residues from different expansion points based on the unique hierarchical reduction framework. Experimental results with large analog circuits, on-chip spiral inductors are presented to validate the proposed method.

I. INTRODUCTION

High-fidelity modeling of radio-frequency (RF) passives and active analog circuits are critical for top-down constraint-driven design methodology for mixed-signal system-on-a-chip (SoC) designs [7].

The compact modeling of passive RLC interconnect networks has been an intensive research area in the past decade due to the increasing signal integrity effects and interconnect-dominant delays in current SoC designs [13]. The most popular methods are the projection-based methods [5,17,18], where modeling is done by explicit moment matching [18] or implicit moment matching [5, 17] via some numerical eigenvalue computation algorithms. Another quite different approach to circuit complexity reduction is by means of local node elimination and realization [1, 4, 20, 23, 24]. The major advantage of these methods over projection-based methods is that the reduction can be done in a local manner and no overall solutions of the entire circuit are required and reduced models can be easily realized using RLCM elements. This idea was first explored by selective node elimination for RC circuits [4, 23], where time constant analysis is used to select nodes for elimination.

Most of those existing model order reduction algorithms, however, mainly reduce passive RLC networks. Compact modeling methods for general linear active analog circuits with controlled sources were less exploited. For general active linear analog circuits, behavioral modeling by means of symbolic analysis has been studied in the past. But most of existing approaches still suffer from the circuit-size limitation problem as symbolic expressions grow exponentially with circuit sizes [7]. Hierarchical decomposition is an efficient way to cope the circuit-size limitation problem. But both the *sequence of expressions* generated by symbolic topologic [26] and network hierarchical analysis methods [8] and the hierarchical DDD (determinant decision diagrams) graphs by DDD-based hierarchical decomposition method [29] are difficult to interpret. The resulting symbolic expressions are too complicated to gain insights into circuit behavior or be incorporated into the higher level simulators as simulation-friendly mathematical behavioral models.

Recently, a general s-domain hierarchical model reduction algorithm was proposed [27, 28]. The new method promises the compact modeling for both passive and active linear networks. But due to truncations of high order terms and numerical noises in the reduction process, obtaining accurate, high-fidelity models in very high frequency ranges is a difficult task for general structured linear circuits. In the following Section III, we first show theoretically that the s-domain hierarchical reduction is equivalent to implicit moment matching around $s = 0$, and that the existing hierarchical reduction method by one-point expansion [27, 28] is numerically stable for general tree-structured circuits. In Section IV, we propose a new hierarchical multi-point expansion scheme via a novel explicit waveform matching algorithm for searching the dominant poles and residues from different expansion points. The resulting algorithm can be used for the high-fidelity, wideband modeling of any multi-input multi-output passive circuits up to RF frequencies and active analog circuits in both frequency and time domain. Experimental results with large analog circuits, on-chip spiral inductors, high-speed transmission lines demonstrate the effectiveness of the proposed method in Section V. Section VI concludes the paper.

II. REVIEW OF HIERARCHICAL CIRCUIT REDUCTION ALGORITHM

The hierarchical reduction algorithm is a general high-order node-elimination based reduction algorithm in s-domain based on MNA (modified nodal formulation) formulation [27, 28]. It is based on the general Schur decomposition process and a graph-based de-cancellation algorithm to obtain the reduced circuit models in terms of rational functions or function matrices. Although both $Y-\Delta$ transformation algorithm [20] and the hierarchical reduction method is essentially based on Gaussian elimination, the hierarchical reduction method is more general and applicable to any linear circuit due to MNA formulation, while $Y-\Delta$ transformation is based nodal analysis (NA) formulation as it performs the reduction directly on circuit topologies.

One critical issue during the hierarchical reduction is cancellation. Two type of cancellations have been observed [27]: symbolic term cancellation, where two product terms consisting of the composite admittances cancel out; *symbolic common-factor* cancellation, where the numerators and the denominators of the resulting product terms consisting of the composite admittances will have a symbolic common factor,

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which happen when there are at least two first-order cofactors exist in a product term.

A general s-domain reduction algorithm was proposed in [27,28] where de-cancellation is carried out numerically in frequency domain (s-domain).

III. Hierarchical Reduction Versus Moment Matching

In this section, we first discuss how the s-domain hierarchical reduction is related to the implicit moment matching. Then we discuss the numerical stability of the hierarchical reduction process.

A. Moment Matching Connection

Consider a linear system with n state variables in vector $\mathbf{x}$, the system is given by

$$s\mathbf{x} = \mathbf{A}\mathbf{x} + \mathbf{b}, \tag{1}$$

where $\mathbf{A}$ is a $n \times n$ system matrix, $\mathbf{b}$ is the input vector to the circuit. Then we can obtain $\mathbf{x} = (\mathbf{I}s - \mathbf{A})^{-1}\mathbf{b}$. Let's consider single-input single-output system where we have only one input b_j at node j and we are interested in state response at node i. In this case we have

$$x_i(s) = H_{ij}(s)b_j = \frac{\Delta_{ij}}{det(\mathbf{I}s - \mathbf{A})}b_j, \tag{2}$$

where Δ_{ij} is the first-order cofactor of matrix $\mathbf{M} = (\mathbf{I}s - \mathbf{A})$ with respect to the element at the row i and column j in $\mathbf{M}$. $H_{ij}(s)$ is the transfer function. So the exact solution of any state variable or its transfer function in s-domain can be represented by a rational function of s.

Hierarchical reduction basically is to reduce the $n \times n$ matrix $\mathbf{M}$ into a very smaller $m \times m$ matrix $\mathbf{M}'$ based on block Gaussian elimination such that x_i can be trivially solved symbolically by using Eq. (2). During this reduction process, all the rational functions involved are truncated up to a fixed maximum order and the final solution will be a rational function with the same order for its numerator and its denominator. We then have the following theoretical result for the computed state variable $x'_i(s)$ from the hierarchical reduction process in s-domain.

Proposition 1 *The state variable $x'_i(s)$ computed by the s-domain hierarchical reduction with q as the maximum order for all the rational functions will match the first q moments of the exact solution $x_i(s)$ expanded by Taylor series at $s = 0$.*

The proof of the proposition is omitted due to limited space.

For a general multi-input and multi-output system, each element in the reduced $m \times m$ admittance matrix $\mathbf{M}'(s)$ become an rational function [28]:

$$a^{BB*}_{u,v} = \frac{\det(M[1,...,m,u|1,...,m,v])}{\det(M^{II})}, \tag{3}$$

where, $M[1,...,m,u|1,...,m,v]$ is the submatrix that consists of matrix M^{II}, which actually is $M[1,...,m|1,...,m]$, plus row u and column v of matrix M. Then we have the following results without proof.

Corollary 1 *Each rational admittance function $a'^{BB*}_{u,v}(s)$ in the reduced $m \times m$ matrix, $M'(s)$, by the hierarchical reduction process will match the first q moments of the exact rational function $a^{BB*}_{u,v}(s)$ expanded by Taylor series at $s = 0$.*

B. Numerical Stability of the Hierarchical Reduction

The hierarchical reduction process is essentially equivalent to the implicit moment matching at $s = 0$. As a result, the frequency response that is far away from $s = 0$ will become less accurate due to the truncation of higher order terms. Another source of numerical errors comes from the numerical de-cancellation process where polynomial divisions are required to remove the common-factor (cancellations) in the newly generated rational functions, which will in turn introduce errors from numerical term cancellation (sum of two symbolic terms equals to zero, but not equals to zero due to numerical errors). Such numerical noises will cause the higher order terms less accurate even we try to keep them. In Fig. 1, we show that the responses from the 3-way, 2-level partitioned $\mu A741$ circuit [29] under different maximum reduction orders for rational functions. As we can see that increasing the rational function order does not increase the accuracy of the response after the order reaches 8. This is the typical numerical stability problem with the moment matching method [18]. However, unlike explicit moment matching methods, the hierarchical reduction is numerical stable for tree-structured circuits. We then show the following results:

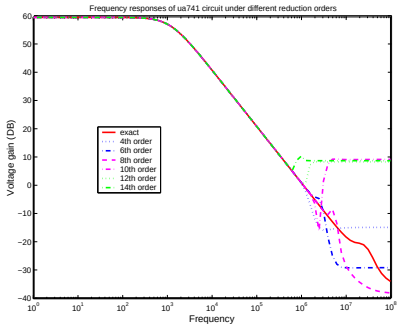

Fig. 1. Responses of $\mu A741$ circuit under different reduction orders.

Proposition 2 *For tree-structured circuits, the hierarchical reduction process can be performed such that there is no common-factor cancellation in the generated rational functions.*

The proof of the proposition is omitted due to limited space.

The significance of Proposition 2 is that the hierarchical reduction process becomes numerical stable for almost arbitrary order. The only cancellation left is the term cancellation, where the sum of two symbolic terms is zero, which will not introduce any noticeable numerical error in the reduction process. Fig. 2 shows the voltage gain responses (real part) of a RC tree with about 100 nodes (also 100 capacitors) under different reduction orders. As can be seen, the reduced voltage gain will match the exact one well when order reaches about 60.

The fact that no common-factor de-cancellation (polynomial divisions) are required was also exploited in the direct truncation of transfer functions method (DTT) [10] where only polynomial additions are required to compute the truncated transfer functions for tree-structured RLC circuits only. The DTT reduction process becomes a linear process, which is also true for the hierarchical reduction process as no new fill-ins are generated. But for general structured circuits, polynomial divisions are required in node elimination based reduction methods due to common-factor cancellations. But polynomial divisions due to truncations will not be numerically stable for very high frequency ranges far away from DC as shown before.

To mitigate this problem, we propose to use multi-point expansions to obtain accurate rational functions or reduced ad-

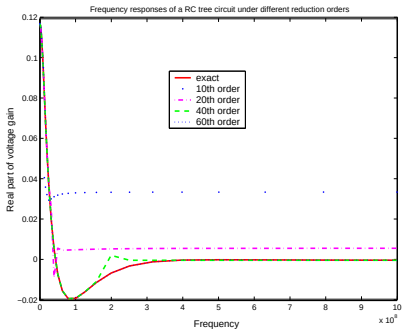

Fig. 2. Responses of a RC tree circuit under different reduction orders.

mittance matrices for modeling general multi-input and multi-output linear system as shown in the next section.

IV. Multi-Point Expansion Hierarchical Reduction

The multi-point expansion scheme by real or complex frequency shifts have been exploited before in projection based reduction approaches to improve the modeling accuracy [3, 9]. The basic idea for such a strategy is that dominant poles that are close to the expansion points can be more accurately captured than the poles that are far away from the expansion points in the moment matching based approximation framework. Therefore instead of expanding at one point, we can expand at multiple points to accurately capture all the dominant points in the given frequency range along real or complex axis.

In this paper, we extend this concept to the hierarchical reduction algorithm. Specifically, at each expansion point, the driving point function or each rational admittance function in a reduced admittance matrix can be written into the partial fraction form

$$f(s) = \sum_{i}^{n} k_i/(s-p_i). \tag{4}$$

By intelligently selecting the poles and their correspond residues from different expansions and combine them into one rational function, we can obtain more accurate rational function for very high frequency ranges. In this paper, we propose an explicit waveform matching scheme based on hierarchical reduction framework to find the dominant poles and residues for both SISO (single-input single output) and MIMO systems (multi-input multi-output) systems, which is shown experimentally to be superior to the existing pole searching algorithm.

A. Multi-Point Expansion In Hierarchical Reduction

To expand the circuit at arbitrary location in the complex s-plane, say $s_k = \alpha_k + \omega_k j$, we can simply substitute s in Eq.(2) by $s + s_k$. Then Eq.(2) will become

$$x_i(s) = H_{ij}(s)b_j = \frac{\Delta_{ij}(s+s_k)}{det(\mathbf{I}(s+s_k) - \mathbf{A})} b_j. \tag{5}$$

As shown in [3], poles that dominate the transient response in interconnect circuits are near the imaginary axis with larger residues. But for many active linear analog circuits like Opamps and filter circuits, poles are placed explicitly by designers and they are typically real poles. Hence we should expand along real axis for active analog circuits while expand along imaginary axis for RF passive circuits. Since only capacitors and inductors are associated with complex frequency variable s, expansion at real α or complex $\omega_i j$ point essentially is equivalent to analyzing a new circuit where each capacitor C has a new resistor (with real value $\alpha_i C$ or complex value $\omega_i C j$ connected in parallel with it and each inductor L has a new resistor (with real value $\alpha_i L$ or complex value $\omega_i L j$) connected in series with it [19].

In this paper, we show that the multi-point expansion can be done very efficiently in the hierarchical reduction framework. The rational functions are constructed in a bottom up fashion in a Y-parameter determinant decision diagrams (YDDDs) in the hierarchical reduction algorithm [27]. When a capacitor C or an inductor L (its YDDD node) is visited, we build a simple polynomial $0 + Cs$ or $0 + Ls$ to multiply or add it with existing polynomials seen at that DDD node. In the presence of a non-zero expansion point, α_i or $\omega_i j$, we can simply build new polynomial $\alpha_i C + Cs$ or $\omega_i C j + Cs$ for the capacitor and $\alpha_i L + Ls$ or $\omega_i L j + Ls$ for the inductor respectively. So we do not need to rebuild the circuit matrix and YDDD graphs used for $s = 0$ reduction. Instead we only need to rebuild the rational functions by visiting every YDDD node once, which has the time complexity linear in terms of YDDD sizes, a typical time complexity for DDD graph based methods [25].

B. Explicit Waveform Matching Algorithm

One critical issue in multi-point expansion is to determine which poles are accurate and should be included in the final rational function at each expansion point. In the complex frequency hoping method [3], a binary search strategy was used where poles (common poles) seen by both expansion points and those poles with distance to the expansion points shorter than the common poles are selected. Such a *common-pole matching* algorithm, however, is very sensitive to the numerical distance criteria for detecting the same poles. For accurate detecting of common poles, small distance is desirable, but it will lead to more expansion points; and even worse is that the same pole may be treated as different poles seen by different expansion points. Also this method may fail to detect some dominant poles as the circle for search accurate poles may be too small as shown in the experimental results.

In this paper, we propose a new reliable pole search algorithm, which is based on the explicit frequency waveform matching. The new algorithm is based on the observation that complex pole p_i and its residue k_i in the partial fraction form, $k_i/(s-p_i)$, have the largest impacts at frequency f_i when imaginary part of the pole equal to the $2\pi f_i$. Fig. 3 shows a typical response of $k_i/(s-p_i)$, where $k_i = 2.78 \times 10^{12} + 2.34 \times 10^{10} j$ and $p_i = -4.93 \times 10^8 + 2.58 \times 10^{10} j$. The peaks of both real (absolute value) and magnitude are around 4.11×10^9, which is equal to $2.58 \times 10^{10}/(2\pi)$. The reason for this is that both real and imaginary parts of $k_i/(s-p_i)$ reach a peak when their a common denominator $(pr)^2 + (\omega - pi)^2$ reach a minimum when $\omega - p_i = 0$, where $s = \omega j$ and $p_i = pr + pij$. Complex pole with negative imaginary part typically will not have significant impacts on the upper half complex plane.

The idea of *frequency waveform matching* is to explicitly match the approximate frequency waveforms with that of exact ones. Specifically, at an expansion point, f_i, we perform the hierarchical reduction and then determine an accurate maximum frequency range $[f_i, f_{i+1}]$ such that the errors between responses (magnitude, real or imaginary parts) of the reduced rational functions and that of the exact ones are bounded by a pre-specified error bound. Then f_{i+1} will be the next expansion points. All the poles whose imaginary part fall within the range $[2\pi f_i, 2\pi f_{i+1}]$ will be selected because their contributions in this frequency range are the largest. The new algorithm

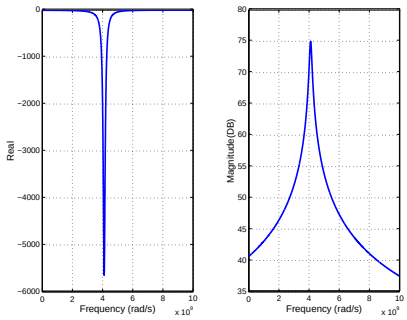

Fig. 3. Responses of a typical $k_i/(s-p_i)$.

does not have the duplicate poles issues as the accurate poles can only be located at one place. The accuracy of the found poles is assured by the explicit waveform matching. Experimental results show that it tends to use less number of expansion points than common-pole matching method with less CPU time.

The new waveform matching algorithm works well for expansion along the imaginary axis. For real axis expansion, as not frequency waveforms can be matched, we still use common-pole matching algorithm.

C. Multi-Point Expansion for MIMO System Reduction

For a multi-input multi-output system, by using the modified nodal analysis, the reduced circuit matrix $M'(s) = [y_{ij}(s)]_{m\times m}$ will become a $m \times m$ admittance matrix. Each admittance y_{ij} is a complex rational function with real or complex coefficients (if expansion point are on imaginary axis). In this case, we explicitly watch the error of each admittance against the exact response. The exact value of each admittance can also be computed by visiting the DDD graphs representing the admittances. Since there are many sharing among those admittances, the cost of evaluating all the admittances are similar to evaluating one admittance since every DDD node needs to be visited just once for each frequency point [29].

D. Passivity and Realization

For RF passive components and transmission lines, passivity is required for the reduced model. Actually, since we obtain the actual poles and residues of original circuits, the resulting rational functions or rational function matrices will almost be stable and passive, and can be in fact be made passive by the convex programming based approach [2].

Also for the one-port modeling using rational functions, exact circuit realization can be done by using Foster's canonical form [30]. Foster's canonical form can map each pole/residue or complex pole pair/residue pair into one unique RLC template circuit without introducing any error for one-port case. Such a mapping, however, may introduce some negative RLC elements. But as long as the rational functions are passive or made passive, the realized circuits will be passive as the transformation between the circuit and mathematic models are reversible. We notice that negative elements are also used in PVL based reduction method [6].

For transfer function realization, at least 2×2 (two-port) admittance matrix has to be realized. Given a 2×2 admittance matrix

$$Y_{2\times 2} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}, \qquad (6)$$

it can be realized exactly by using the π-model template shown in Fig. 4, where each branch admittance will be realized by the one-port Foster's method. Such a realization can also be extended to multi-port case.

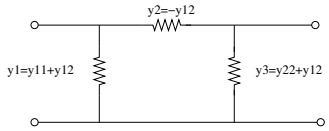

Fig. 4. A general two-port realization π model.

One advantage of such realization is that the transform from the admittance matrix to circuit is error-free (compared to the mathematical models). This method will use more elements than a restricted multiple-port implementation method using Foster's canonical form [14], which however can't realize all the circuits it requires each individual complex pole/residue pair, $k_i/(s-p_i)+k_i^*/(s-p_i^*)$, is positive real (can be realized by RLC elements with positive values), which is generally not the case.

V. Experimental Results

The proposed algorithm has been implemented in C++ and all the data are collected on a Linux workstation with dual 1.6GHz AMD Althon CPUs and 2G memory.

A. Modeling for $\mu A741$ circuit

The first example is the 3-way partitioned 2-level $\mu A741$ circuit, where we show that one-point expansion is not accurate enough in Section B. For this Opamp circuit, the dominant poles are the real poles on the real axis as they are placed by the designers intentionally. To accurately obtain the dominant poles in the frequency range up to 20MHz, we expand the circuit along the real axis in the given frequency range using the common-pole search algorithm. The three dominant real poles are found: $-7366.9, -1.05\times 10^7, -1.31\times 10^7$. The response of the computed transfer function and the exact one are shown in Fig. 5. The obtained transfer functions are very accurate

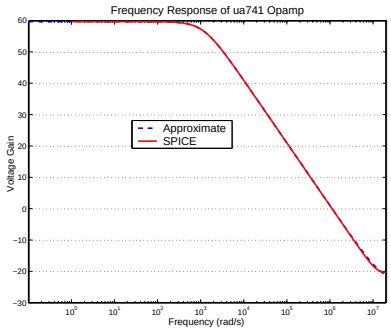

Fig. 5. Voltage Gain Responses of $\mu A741$ Opamp.

compared with the exact up to 20MHz.

B. On-Chip Spiral Inductor

The second example is a 3-turn spiral inductor with 13 sections and substrate. A PEEC (partial element equivalent circuit) [22] model is first built for the spiral inductor. We assume the copper ($\rho = 1.7\times 10^{-8}\Omega\cdot m$) for metal and the low-$k$ dielectric ($\varepsilon = 2.0$). The substrate modeled as a lossy ground

plane (heavily doped) with $\rho = 1.0 \times 10^{-5}\Omega \cdot m$. The conductor is volume-discretized according to the skin-depth, and longitudinal segmented by one 10th of wave-length. The substrate is also discretized as in [15]. The capacitance is extracted by FastCap [16] and only adjacent capacitive coupling is considered since capacitive coupling is short-range. The partial inductance is extracted by FastHenry at 50GHz [11]. The inductive coupling between any pair of segments (including segments in the same line) is considered. We then generate the distributed PEEC model by π-type of RLC-topology to connect each segment, and it results a SPICE netlist with 232 passive RLCM elements. The substrate parasitic contribution (Eddy current loss) is lumped into the above conductor segment. Note that for more accurate extraction at ultra-high frequency, it needs full-wave PEEC model description [12]. For mutual inductance, a vector potential equivalent model (VPEC) is used [31], which is more hierarchical reduction friendly as not coupling inductor branch currents are involved and circuit partitions can be done easily.

B.1 Comparison with Common-Pole Matching Method in Frequency Domain

For the spiral inductor, driving point impedance is obtained by the multi-point hierarchical reduction process. We use both the common-pole matching algorithm in the complex frequency hopping method and the new waveform matching algorithm to search for the dominant poles along the imaginary axis.

For a fair comparison, we make sure the resulting rational functions will have the similar accuracy. For common-pole matching algorithm, if two poles are located within 1% of their magnitudes, they are regarded as the same pole. For waveform matching algorithm, the error bound between the approximate one and the exact is set to 0.1%. As a result, common-pole approach takes 26 expansion with 37.1 seconds, waveform marching method use 15 expansion with 22.57 seconds. The responses obtained using both method versus the exact response up to 100Ghz are shown in the Fig. 6. The responses from both methods match the exact ones very well all the way to 100Ghz. Our experience show that CPU time of common-pole method is highly depends on the common-pole detection criteria. For instance if we set the criteria for common-pole detection to 0.5%, then 65 expansions are carried out. Also as more expansions are carried out, the number of actual common poles seen by two consecutive expansions become larger, but they may be treated as different poles due to small distance criteria, which in turn leads to significant distortions of the frequency responses.

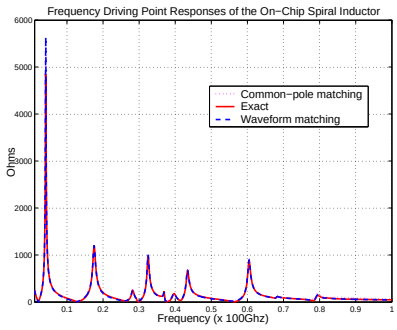

Fig. 6. Frequency Response of the 13-turn spiral inductor and its reduced model by using waveform matching and common-pole method.

B.2 Time-domain Simulation of a LC Oscillator

We further demonstrate the accuracy and efficiency of the inductor macro-model in time-domain harmonic simulation. Note that the synthesized one-port macro-model can be used to efficiently predict the critical performance parameters of spiral inductor, such as the ω_T, Q factor, and even the resonance starting-condition for a oscillator. [21].

We use the Colpitts LC oscillator as an example as shown in Fig. 8 (b) where the active circuit behaves like *negative resistance* to make the oscillator work as shwon in Fig. 8 (a).

In the experiment, the synthesized one-port model is from a 25-order rational function with 24 poles and results in a macro-model with 40 RLC elements. As shown in Fig. 7, the waveform at steady state of synthesized model and original model match very well but we observe the 10X times (5.17s vs. 0.52s) runtime speedup by using the reduced model.

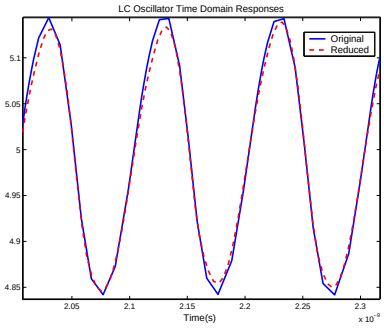

Fig. 7. Time-domain comparison between original and synthesized models for a Colpitts LC oscillator with a 13-segment spiral inductor.

B.3 Modeling of High-Speed 2-bit coupled transmission Line circuits

The last example is 2-bit coupled transmission lines with 10 uniform segments which are extracted using the same method as the spiral inductor without considering the substrate loss and are modeled by PEEC lumped RLCM elements with about 480 RLCM elements.

We first realize the driving point impedance of one transmission line. The impedance rational functions are still obtained by both waveform matching and common-pole matching algorithms. The frequency response up to 30Ghz are shown in Fig. 9. We notice that response given by common-pole method has significant discrepancy compared with the exact one between 1GHz to 10GHz. Detailed analysis shows that the common-pole algorithm fails to find a pole at 5.7*Ghz*, which

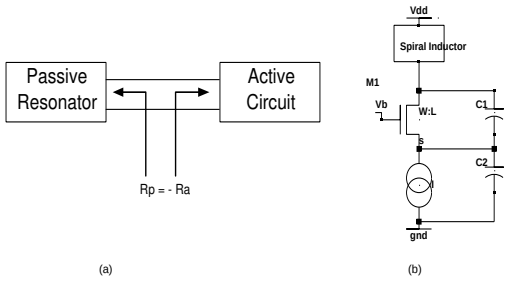

Fig. 8. Colpitts LC oscillator with spiral inductors.

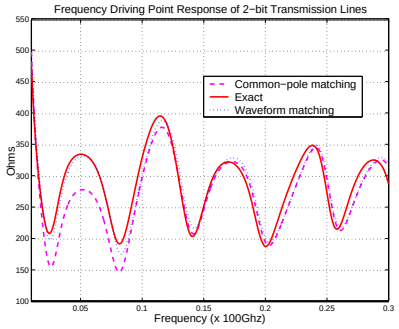

Fig. 9. Frequency Response of 2-bit Transmission Lines using waveform matching and common-pole method.

is $-0.24E11 + 0.36E11i$, which has peak response at $5.7Ghz$ ($0.36E11/(2\pi) = 5.7E9$). The reason is that this poles fall out of circle of the two expansion points which see a common-pole that are more close to the two expansion points.

To realize the transfer functions from one end of the transmission line to another end, a simple two-port realization method shown in Section D is used. The 2×2 reduced admittance matrix is obtained by using hierarchical reduction via explicit waveform matching up to 10Ghz. There are 21 expansion points with about 12 poles for each admittance rational function. The total RLC elements is 75, which represents 84.4% reduction ratio. Fig. 10 shows the step responses of the synthesized circuit and the original circuit.

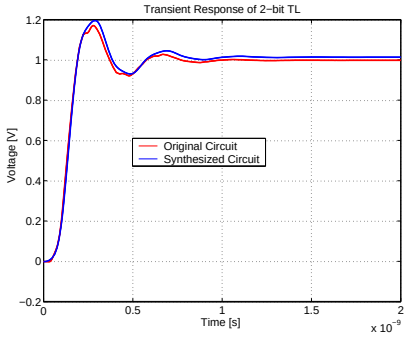

Fig. 10. Transient Response of 2-bit transmission lines.

VI. Conclusion

We have proposed a new hierarchical multi-point reduction algorithm for wideband modeling of high-performance RF passives and linear(ized) analog circuits. In the theoretical side, we showed that the s-domain hierarchical reduction is equivalent to the implicit moment matching around $s = 0$. We also analyzed the numerical stability of the existing hierarchical reduction algorithm and showed that the hierarchical one-point reduction is numerically stable for general tree-structured circuits. In the practical side, we have proposed a hierarchical multi-point reduction scheme for high-fidelity, wideband modeling of general passive and active linear circuits. A novel explicit waveform matching algorithm is proposed for searching the dominant poles and residues from different expansion points, which is shown to be more efficient than the existing pole search algorithm. Experimental results with large analog circuits, on-chip spiral inductors and high speed transmission lines have demonstrated the effectiveness of the proposed method.

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