

Power/Ground Network Aware and Row-Based Solutions to the Crosstalk Driven Routing Problem *

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Abstract-This paper gives power/ground network aware and row-based solutions to the crosstalk driven routing problem. Routability and timing issues are also considered. The algorithm has been implemented and tested on MCNC benchmarks. Compared with the recent work introduced in [11], the proposed algorithm can achieve more than 72% on average improvements for the adjacent edges while considering power/ground network, which greatly reduces potential vias.

I. INTRODUCTION

Chip design is with increasingly shrinking geometries yet increasingly higher frequencies. Coupling effects and crosstalk have gained more concerns for chip performance optimization [1]. Crosstalk elimination can be performed in two different ways. One is with the circuit design method, such as adding suitable capacitances or inserting buffers. The other is with the help of CAD tools, such as routing tool in the physical design phase. So, crosstalk elimination has become a challenge to chip routing.

Some existing works focus on coupling noise and crosstalk elimination in the routing phase, which mainly fall into three categories, noise modeling [2], [3], noise minimization [4]-[7], and simultaneous noise minimization and performance optimization [8]-[11]. [2] derived expressions for a coupling capacitance and a crosstalk voltage height. [3] declared that on-chip inductance, especially mutual inductance, should be considered for high-performance interconnect design and presented the effective coupling model, called the K_{eff} model. [4] described a two-pass algorithm including region-based crosstalk risk estimation and crosstalk reduction. [5] presented a cost function taking crosstalk into consideration, and is used during the phase of constructing the routing tree. [6] proposed

a three-phase algorithm based on crosstalk budgeting, simultaneous shield insertion and net ordering (SINO), and local refinement. Both [8] and [9] proposed performance optimization global routing algorithms considering crosstalk reduction. The former mainly focuses on coupling capacitance and uses spacing method. The latter considers coupling inductance and is based on shield insertion. [10] presented an efficient RLC crosstalk reduction algorithm by using Tabu search method and achieved about 20x speedup compared with [9]. The latest progress is the global routing algorithm, AT-PO-GR, to minimize the routing area under congestion, timing, and RLC crosstalk constraints [11].

However, [9]-[11] did not take actual power/ground (P/G) network and potential via minimization into consideration. The main contribution of this paper is the P/G network aware and row-based solutions to the crosstalk driven routing problem. This algorithm (1) takes P/G network into consideration to meet the practical applications, (2) and gives a row-based routing solution to minimize potential vias, which is useful for good manufacturability.

The remainder of this paper is organized as follows. Section II formulates the routing problem considering P/G network. In Section III, we discuss the routing algorithm in detail. Section IV shows experimental results and discussions. Section V concludes the whole work and gives some possibilities for future work.

II. PROBLEM FORMULATION

A. GRG with P/G network

With the progress in multi-layer VLSI routing technology, routing area is a whole chip plane. Thus, a net can be specified as a set of nodes in global routing graph (GRG). Then, the problem of routing a net can be described as a rectilinear Steiner tree (RST) problem of specified nodes in GRG [12].

But generally, while we mapping the P/G network on the

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GRG, we'll not get the same/similar grid in the graph. Fig.1 shows the general relationship between the mapping of P/G network and the grid in GRG. We can see that P/G mapping is sparse than GRG grid. Then, while performing crosstalk elimination with shielding, we should consider this problem, here we call it the *incongruous grid problem*, which limits the shielding style and shielding number. We can only get fewer horizontal shields and more vertical ones. And the horizontal shields are longer ones relative to one GRG grid.

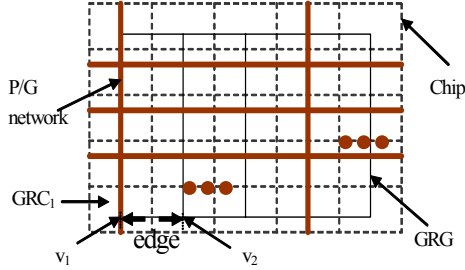


Fig.1. GRG with P/G network.

B. RLC Noise Model

The LSK model for RLC crosstalk [3], [7] is used in this paper. Different from earlier noise model [2], the LSK model considers coupling inductance between adjacent and non-adjacent sensitive nets. A formula-based K_{eff} model has been developed in [3] to calculate the inductive coupling coefficient $k_{it,jt}$. Furthermore, the total amount of inductive coupling induced on segment N_{it} can be represented by the sum of the inductive coupling coefficient $K_{it} = \sum_{j \neq i} k_{it,jt}$ for all net segments N_{jt} that are sensitive to N_{it} . To consider the effect of interconnect length and the general case where the total coupling is not uniform in all routing regions, a length-scaled K_{eff} (LSK) model was proposed in [7], where the LSK value is defined as $LSK = \sum_t l_t \cdot K_{it}$, where l_t is length of R_t and K_{it} is total coupling for N_{it} in region t .

C. Problem Formulation

Let

$$S_{it} = \begin{cases} 1, & \text{edge } t \text{ be used by net } i, \\ 0, & \text{otherwise.} \end{cases} \quad (1)$$

where S_{it} is a kind of stamps indicating whether edge t contains net i .

Then we have

$$\text{Minimize } L = \sum_{i=1}^{N_n} \sum_{t=1}^{N_e} S_{it} l_t$$

Subject to

$$f_t = \sum_{i=1}^{N_n} S_{it} + s_n + o_t \leq c_t, \forall t \in E; \quad (2)$$

$$T(i, j) \leq T_D(i, j), \forall i \in N, \forall j \in s(i); \quad (3)$$

$$LSK_{ij} \leq \overline{LSK}_{ij}, \forall i \in N, \forall j \in s(i); \quad (4)$$

Formula (2) is the congestion constraint, which forbids the overflow on each GRG edge. Formula (3) guarantees the actual delay value from source i to sink j , $T(i, j)$, is no more than the given timing constraint $T_D(i, j)$. Formula (4) sets the upper bound of LSK , \overline{LSK}_{ij} , for each source sink pair ij . The actual LSK value of this pair, LSK_{ij} , could not exceed the bound.

III. OUR ROUTING ALGORITHM

A. Incongruous Grid Problem

Fig.2 shows a local part of GRG. We can see 3 GRG edges, edge60, edge61, and edge62. Fig.3 shows an example of previous routing result. Brown lines denote the shields, black lines denote the net segments, and dashed lines are unused tracks. Since shields provided by P/G network are as long as three GRG edges, the previous routing results should be improved to meet the practical applications. We can adjust orders of the horizontal net segments shown in Fig. 4.

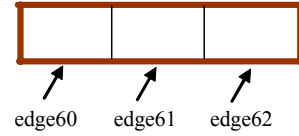


Fig. 2. A local P/G network and GRG edges.

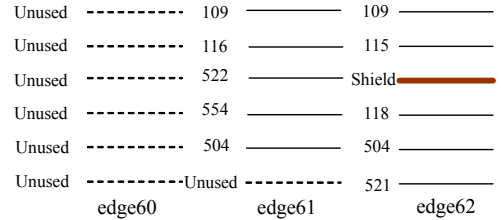


Fig. 3. An example of previous routing result.

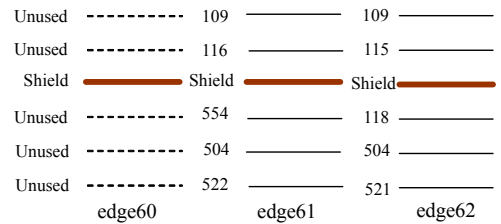


Fig. 4. The result after adjusting.

B. Row-Based Solution

Previous routing algorithms [9]-[11] performed crosstalk elimination only in single GRG edge. So, the routing results cause "dog-leg", i.e., segments of the same net in adjacent

GRG edges but are in different tracks (denoted by the order in the global routing phase), which makes more potential vias in detailed routing. Fig.5 shows an example. Two segments of Net1 are not in the same track. We try to find a row-based solution to tackle this “dog-leg” problem in this Section.

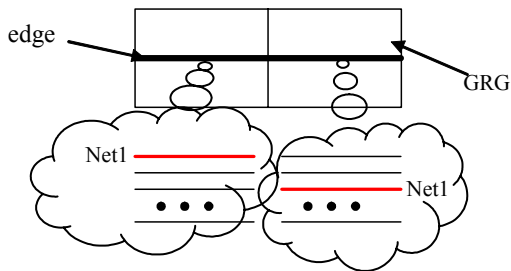


Fig. 5. The “dog-leg” problem.

C. Our Methods

1. Obtain Row-Based Solution

We still use Tabu search method [9] to eliminate crosstalk noise. But we use a new cost formula of a GRG edge as follows to take the “dog-leg” problem into consideration.

$$\text{cost}(x) = w_1 c_1 + w_2 c_2 + w_3 c_3 + w_4 c_4 + w_5 c_5 \quad (5)$$

where $w_1, w_2, w_3,$ and w_4 are the weights that equal to 13, 2, 13, and 10, respectively. c_1 is the number of adjacency of sensitivity rate, c_2 is the sum of violation K_{eff} value, c_3 is the number of K_{eff} violation, and c_4 is the number of shield inserted. w_5 equals 15, $c_5 = (1 - a / b)$, a is the number of the adjacent segments of a net in the same tracks, b is the capacity of the GRG edge.

2. Tackle Incongruous Grid Problem

Aware of P/G network, we assume that the horizontal shields are as long as 3 GRG edges. We try to make the 3 adjacent horizontal GRG edges have the same shield order by using the following method.

Firstly, we partition all the horizontal GRG edges into edge groups, each of which includes 3 adjacent edges. Then, in the same edge group, we can get the *critical edge*, which has the largest shield number. After that, we let the same shields track (i.e., the same shield order) in the other two edges (*non-critical edges*). At last, we can adjust the segments in the *non-critical edges* to make use of the assigned shields. Formula (5) is also used here to minimize the cost. Fig.4 shows an example. Edge62 in Fig.4 is the critical edge. Then, we add one shield as the same order in edge60 and edge61, respectively. After that, we adjust the segments in these two edges. At last, we got the minimal cost routing solution shown in Fig.4.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

Our algorithm has been implemented in C language. It performs on a SUN V880 workstation with Unix OS. We compared our results with that of AT-PO-GR [11].

A. Benchmark Data

We tested 5 MCNC benchmarks given in TABLE I.

TABLE I
BENCHMARK DATA

Circuits	Number of net	Grids
C2	745	9*11
C5	1764	16*18
C7	2536	16*18
S13207	4953	24*26
Avq	21581	65*67

B. Results and Discussions

RB denotes the algorithm to get a row-based solution and IG denoted the algorithm considering incongruous grid problem.

TABLE 2

COMPARISON OF NUMBER OF ADJACENT EDGES HAVE SAME TRACK POSITION

Circuits	AT-PO-GR	RB	IG
C2	116	339	202
C5	361	413	654
C7	382	416	797
S13207	1382	2322	4770
Avq	3207	5793	12513
Aver imp	-----	72.84%	159.85%

TABLE 3

COMPARISON OF TOTAL WIRE LENGTH

Circuits	AT-PO-GR	RB	IG
C2	462204	465886	465886
C5	1320742	1327700	1327700
C7	1516366	1520446	1520446
S13207	9881044	9894684	9894684
Avq	9899034	9873887	9873887
Aver imp	-----	0.29%	0.29%

TABLE 4

COMPARISON OF TOTAL RUNNING TIME

Circuits	AT-PO-GR	RB	IG
C2	87.21	70.44	98.08
C5	257.93	212.20	275.13
C7	331.25	279.21	345.41
S13207	2049.16	1436.15	1822.97
Avq	6171.94	5612.33	6479.56
Aver imp	-----	18.33%	-3.47%

TABLE 5

COMPARISON OF TOTAL AREA

Circuits	AT-PO-GR	RB	IG
C2	168*204	174*203	175*203
C5	304*332	301*333	302*333
C7	342*365	360*377	364*377
S13207	1208*1410	1203*1420	1216*1420
Avq	1216*1001	1215*1003	1223*1003
Aver imp	-----	-2.30%	-3.08%

1. We compare the number of adjacent net segments (in the same track order) in TABLE 2. It clearly shows that RB improves the adjacent edges by 72.84% on average

compared to that of AT-PO-GR, which indicates the effectiveness of our methods in aligning routing solutions, thus reducing potential doglegs and vias for detailed routing. We also note that IG is on average 159.85% more than that of AT-PO-GR. This is because we add empty tracks and have more possibility to adjust the net segments.

2. As shown in TABLE 3, the total wire length of RB and IG are almost the same as that of AT-PO-GR because our goal is to minimize the wire length.
3. According to TABLE 4, the running time of RB is slightly shorter than that of AT-PO-GR because the area is larger and we are more flexible in routing. The running time of IG is about 20% longer than that of RB because we add a long shield adjusting process.
4. From TABLE 5, we can see that the area of RB is about 3%-8% larger than that of AT-PO-GR. That is because we use new cost computation formula, the area owns a smaller proportion than previous. The area of IG is slightly larger than that of BR because in some cases, the maximal track number of a GRG edge may increase after long shield adjusting (see Section C).

C. An Example

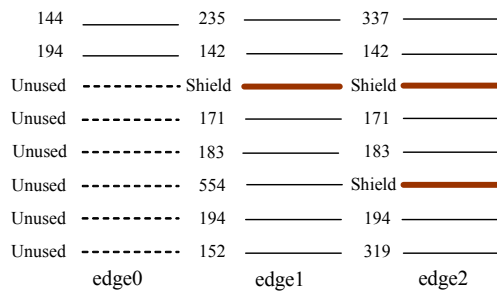


Fig.6. GRG edges before long shield adjusting.



Fig.7. The long shield adjusting result.

We can see that the critical edge in Fig.6 is edge2, and edge1 has the maximal height of 8. But when we add a shield into edge1, the height of it must increase 1. From Fig.7, we can see that the new maximal height is 9. If the maximal

height of a row increases, the total area will increase.

In Fig.6, we can see that only the segments of edge1 have the possibility to be move to the same position as the edge0. But in Fig.7, in long shield adjusting process, the empty tracks of the left could be used. So we can move the segment 194 to the same position as the edge1. So the number of net segments in adjacent edges have the same track position increases.

V. CONCLUSIONS AND FUTURE WORK

A performance and RLC crosstalk driven routing algorithm considering P/G network and row-based solution is presented in this paper. The experimental results show this algorithm can (1) take P/G network into consideration to meet the practical applications, (2) and can give a row-based routing solution to minimize potential vias, which is useful for good manufacturability.

As our future work, we plan to make our algorithm more practical to real chip routing, and design better strategies for crosstalk elimination.

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