Short Papers

Piecewise Linear Model for Transmission Line With Capacitive Loading and Ramp Input

Jun Chen and Lei He

***Abstract*—Transmission line effects become increasingly significant for on-chip high-speed interconnects. Efficient and accurate transmission line models are required for analysis and synthesis of such interconnects. In this paper, we first present an efficient model for the far-end response of a single transmission line considering ramp input and capacitive loading. Our model divides the time axis into a number of regions according to the time of flight and the input rising time, and then approximates the far-end response by piecewise linear (PWL) waveform in each region. We name the resulting model as the PWL model. Experiments show that the waveform from the PWL model differs from the SPICE simulation result with the average voltage difference less than 0.9% $V_{\rm dd}$, and the PWL model is at least 1000× faster than SPICE simulation. We further apply the PWL model to calculate the delay, rising time, and oscillation amplitude of the coplanar waveguide structure, and achieve less than 10% average error compared to SPICE simulation. Combining the PWL model and decoupling technique, we analyze the far-end response of bus structures and obtain waveform almost perfectly matching the SPICE simulation result.**

***Index Terms*—Inductance, interconnect modeling, signal integrity, transmission line, very large scale integration (VLSI) interconnect.**

I. Introduction

Inductance effects in on-chip interconnects becomes increasingly important with smaller transition time and lower wire resistance (as a result of copper interconnect), especially in global interconnects such as clock tree, power/ground network, and parallel buses [1]–[3]. Significant inductance causes prominent transmission line effects such as overshoot and undershoot. To accurately analyze these phenomena, we need to model the high-speed interconnects by transmission line models. Because of the high integration level, these models need to be highly efficient for interconnect modeling and synthesis in very large scale integration (VLSI) designs.

Existing work on transmission-line modeling can be divided into two types. The first type is numerical simulation, such as the convolution simulation [4], [5], state-based approach [6], and waveform relaxation techniques [7], [8]. Although these methods can provide accurate solutions, generally they are too time consuming for large-scale analysis. To improve the efficiency, reduced-order modeling techniques, such as asymptotic waveform evaluation (AWE) [9], [10], Pade approximation [11], and Krylov subspace methods [12], have been proposed to model transmission lines with a finite number of poles of the transfer function. Although these methods can provide solutions more efficient than SPICE simulation, it is still time-consuming, if not impossible, to apply them in VLSI interconnect synthesis.

Manuscript received February 27, 2004; revised August 28, 2004. This paper was supported in part by the National Science Foundation under CAREER Award CCR-0401682, in part by the Semiconductor Research Corporation under Grant 1100, in part by the University of California under a MICRO grant sponsored by the Analog Devices, in part by Fujitsu Laboratories of America, in part by the Intel Corporation, in part by LSI Logic, and in part by a Faculty Partner Award from IBM. This paper was recommended by Associate Editor D. Blaauw.

The authors are with the Electrical Engineering Department, University of California, Los Angeles, CA 90095 USA (e-mail: jchen@ee.ucla.edu; lhe@ee.ucla.edu).

Digital Object Identifier 10.1109/TCAD.2005.847895

The second type of transmission line models is closed-form solutions. This type of solution is usually much more efficient than numerical approaches and can be used for iterative VLSI interconnect synthesis. Based on two-pole approximation, [13] proposed a closed-form solution to the far-end delay and noise of a single transmission line with loading, but the model is unable to consider the distributed nature of transmission lines with limited poles and therefore is not accurate. Based on a series of modified Bessel functions, [14] and [15] provided an accurate closed-form solution for the far-end response of a single transmission line, but they only consider step inputs. Based on the reflection characteristics of the traveling wave in transmission lines, [16] proposed a traveling wave analysis (TWA) model for the far-end response of a single transmission line, but the model computes the waveform based on a three-pole model and an equivalent *RC* model, which may lead to significant errors as will be shown in Section II. Based on the solution from [14], a recent work [17] provided a closed-form solution to the delay of the ramp response of an open-ended transmission line by linear approximation, but the model only works when the far-end rising time is less than twice of the time of flight. In summary, none of the existing efficient models [13]–[17] consider both ramp input and loading capacitance with high accuracy.

To meet the demand of a fast and accurate transmission line model for large-scale on-chip interconnect synthesis, we provide an efficient model for the far-end response of a transmission line considering both capacitive loading and ramp inputs. This model divides the time axis into a series of regions according to the time of flight and input rising time, and then approximates the responses by piecewise linear (PWL) waveform. We call this model the PWL model. Experiments show that the waveform computed by the PWL model matches the SPICE simulation result with an average voltage difference less than 0.9% and the model is at least 1000× faster than SPICE simulation. We further apply the PWL model to compute the delay, rising time, and oscillation at the far end of coplanar waveguide (CPW) structures and achieve less than 10% average error compared to SPICE simulation. Compared to the existing methods [14] and [16], it reduces errors by 90% on average with similar or shorter runtime. Then, with the decoupling model proposed in [18], we apply the PWL model to analyze the far-end response of bus structures. The waveform derived from the PWL model almost perfectly matches those obtained from SPICE simulations.

The rest of the paper is organized as follows. In Section II, we present and verify the PWL model. In Section III, we apply the PWL model to analyze CPW structures and bus structures. We conclude the paper in Section IV with a discussion of future work.

II. PWL Model for Transmission Line

In this section, we present the PWL model for a single transmission line. The PWL model includes three steps: 1) transform the transmission line to a new transmission line without loading capacitance based on moment matching; 2) construct the step response based on the PWL assumption and the solution to an open-ended transmission line from [14]; and 3) derive the ramp response based on the step response from step 2.

We first briefly review the solution for an open-ended transmission line presented in [14], and then discuss the PWL model step by step in Sections II-B-II-D. For a clear explanation, in Table I we summarize the notations used in this paper. Generally, we use subscript "i" for the notations related to the input, subscript "o1" for those related to the far-end step response, and subscript "o2" for those related to the far-end ramp response.

TABLE I
NOTATIONS

R	total wire resistance
L	total wire inductance
C	total wire capacitance
R_d	driver resistance
C_L	loading capacitance
t_{ri}	input rising time
t_f	flight time of the original transmission line
t'_f	flight time of the transformed transmission line
t_{do}	delay at far-end
t_{ro}	rising time at far-end
V_i	input waveform
V_{o1}	voltage response at far-end with step input
V_{o2}	voltage response at far-end with ramp input

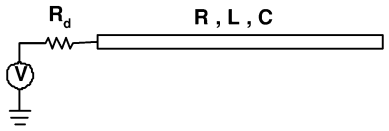

Fig. 1. Single open-ended transmission line.

A. Accurate Solution for Open-Ended Transmission Line

The authors of [14] proposed an accurate transient solution for a single open-ended transmission line with a linear driver as shown in Fig. 1. The driver is modeled as a voltage source with a driver resistance, and input is assumed to be a step input. Using the inverse Laplace transformation, [14] first rigorously derived the accurate solution for an infinite long transmission line, and the transient voltage at the position x along the transmission line is

$$V_{\inf}(x,t) = V_{\rm dd}\frac{Z_0}{Z_0+R_d}e^{(-R/2L)t}u_0(t-x\sqrt{LC}) \times \left\{ \begin{array}{l} I_0\left(\sigma\sqrt{t^2-(x\sqrt{LC})^2}\right) \\ +\frac{1}{1-\Gamma}\sum_{k=1}^{k=\infty}\left(\frac{t-x\sqrt{LC}}{t+x\sqrt{LC}}\right)^{k/2} I_k\left(\sigma\sqrt{t^2-(x\sqrt{LC})^2}\right) \\ \cdot\left(4-(1+\Gamma)^2\Gamma^{k-1}\right) \end{array} \right\} \quad (1)$$

where the characteristic impedance of the transmission line $Z_0 = \sqrt{L/C}$, the reflection coefficient at the near end $\Gamma = (R_d - Z_0)/(R_d + Z_0)$, $\sigma = R/(2L)$, and $I_k(k = 0, 1, 2, \ldots)$ is the kth order modified Bessel function.

Based on this solution and the reflection theory, the transient solution for an open-ended transmission line with a finite length ℓ is derived as

$$\begin{aligned} V_{\rm fin}(t) &= 2V_{\inf}(t) + 2V_{\rm dd}\frac{Z_0}{Z_0+R_d}e^{-(R/2L)t}\sum_{n=1}^{q}\sum_{i=0}^{n}\sum_{j=0}^{\infty} \\ &\times \frac{n(n-i+j)!}{i!j!(n-i)!}(-1)^i\Gamma^{(n-i+j)} \\ &\times u_0(t-(2n+1)\ell\sqrt{LC}) \\ &\times \left\{ \begin{array}{l} \left(\frac{t-(2n+1)\ell\sqrt{LC}}{t+(2n+1)\ell\sqrt{LC}}\right) I_{i+j}\left(\sigma\sqrt{t^2-\left((2n+1)\ell\sqrt{LC}\right)}\right) \\ +\frac{1}{1-\Gamma}\sum_{k=1}^{k=\infty}\left(\frac{t-(2n+1)\ell\sqrt{LC}}{t+(2n+1)\ell\sqrt{LC}}\right)^{(i+j+k)/2} \\ \cdot I_{i+j+k}\left(\sigma\sqrt{t^2-\left((2n+1)\ell\sqrt{LC}\right)^2}\right) \\ \times\left(4-(1+\Gamma)^2\Gamma^{k-1}\right) \end{array} \right\}. \end{aligned} \quad (2)$$

The solution in (2) is accurate, but it does not consider loading or input rising time.

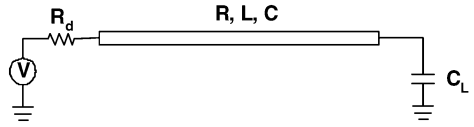

Fig. 2. Circuit model of a single transmission line.

B. Consideration of Capacitive Loading

In this section, we consider the capacitive loading at the far end of the transmission line. As shown in Fig. 2, we model the driver by a voltage source and a driver resistor, and the loading by a loading capacitor. The input can be either step input or ramp input.

Assuming the total resistance, capacitance, and inductance for the transmission line are *R*, *C*, and *L*, as in Fig. 2, the transfer function according to [19] is

$$\begin{aligned} H(s) &= \frac{V_o(s)}{V_i(s)} \\ &= \frac{1}{(1+sR_sC_L)\cosh(\theta)+\left(\frac{R_s}{Z_0}+sC_LZ_0\right)\sinh(\theta)} \\ &= \frac{1}{1+\sum_{i=1}^{\infty}b_is^i} \end{aligned} \quad (3)$$

where

$$\begin{aligned} \theta &= (R+sL)sC \\ Z_0 &= \sqrt{(R+sL)/sC} \\ b_1 &= R_dC_L + \frac{RC}{2} + R_dC + C_LR \\ b_2 &= \frac{LC}{2} + \frac{R^2C^2}{24} + \frac{R_dRC_LC}{2} + \frac{(R_dC+C_LR)RC}{6} + C_LL. \end{aligned} \quad (4)$$

The time of flight of the transmission line is $t_f = \sqrt{LC}$. It is difficult to obtain the time-domain response by directly integrating the function (3) with the loading capacitance. However, (2) provides an accurate closed-form solution to a single open-ended transmission line. Therefore, we propose to transform the original transmission line with C_L [Fig. 3(a)] to a new open-ended transmission line without C_L [Fig. 3(b)]. We match the transfer functions of the two transmission lines. More precisely, we match the first two moments of the two transfer functions as shown in Fig. 3. Assuming the C' and L' are the total capacitance and inductance of the open-ended transmission line after transforming, the transfer function of the transformed transmission line is

$$\begin{aligned} H'(s) &= \frac{1}{\cosh(\theta')+\frac{R_s}{Z'_0}\sinh(\theta')} \\ &= \frac{1}{1+\sum_i b'_is} \end{aligned} \quad (5)$$

where

$$\begin{aligned} \theta' &= (R+sL')sC' \\ Z'_0 &= \sqrt{(R+sL')/sC'} \\ b'_1 &= \frac{RC'}{2} + R_dC' \\ b'_2 &= \frac{L'C'}{2} + \frac{R'^2C'^2}{24} + \frac{R_dRC'^2}{6}. \end{aligned} \quad (6)$$

To obtain C' and L', we match the first two moments of (3) and (5) by setting

$$\begin{aligned} b'_1 &= b_1 \\ b'_2 &= b_2. \end{aligned} \quad (7)$$

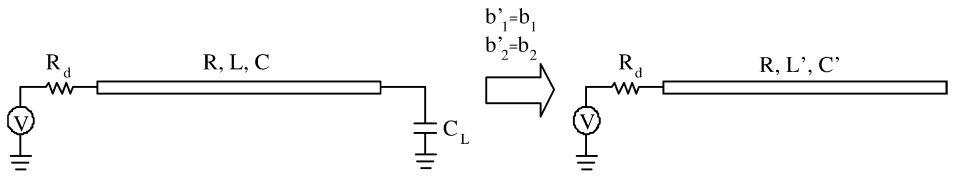

Fig. 3. Transformation to an open-ended line. (a) Original transmission line with loading. (b) Transformed transmission line without loading.

Therefore, we have

$$C' = \frac{b_1}{R_d + \frac{R}{2}}$$
$$L' = \frac{2\left(b_2 - \frac{R^2C'^2}{24} - \frac{R_dRC'^2}{6}\right)}{C'}. \quad (8)$$

The time of flight of the transformed transmission line can be seen in (9), which can be seen at the bottom of the page. By matching the first two moments, we map the effect of C_L into C' and L'. t'_f can be viewed as the effective time of flight considering the loading capacitance. Normally, $t'_f > t_f$, but when C_L and in turn C' is sufficiently large, t'_f calculated by (9) may be smaller than t_f. In this case, t'_f is not physically meaningful. Because of the large capacitive loading, the circuit is capacitively dominant. Naturally, when $t'_f > t_f$, we can just match the first moment and obtain

$$b'_1 = b_1$$
$$\Rightarrow C' = \frac{b_1}{R_d + \frac{R}{2}}$$
$$\Rightarrow t'_f = \sqrt{C'L} \quad (10)$$

where L does not change in this special case and because $C' > C, t'_f > t_f$ holds.

C. PWL Model for Step Response

The open-ended transmission line after transformation can be solved accurately by (2) originally developed in [14]. However, without the loading, the resulting waveform has steep risings at $t = (2n-1)t'_f (n = 1, 2, 3, \ldots)$, which is not true with the loading capacitance present. Furthermore, it is not efficient to compute the entire waveform simply by time stepping as in [14]. Therefore, we develop a PWL model to approximate the waveform.

In the open-ended transmission line after transforming, the signal initiated at $t = 0$ from the driver is reflected at $t = (2n-1)t'_f (n = 1, 2, 3, \ldots)$ at the far end. Correspondingly, the far-end response changes rapidly around these time points, but changes slowly between these points. Therefore, the time axis can be divided into a series of regions, $(0, t'_f), (t'_f, 3t'_f), (3t'_f, 5t'_f), \ldots$ according to the time of flight. Two straight lines are used to approximate the response in each region: one line with a steep slope for the first rising/falling edge around $(2n-1)t'_f (n = 1, 2, 3, \ldots)$, and the other line with a relative flat slope for the plateau waveform between $((2n-1)t'_f, (2n+1)t'_f)(n = 1, 2, 3, \ldots)$. The lines for the rising/falling edges are determined by the voltages and slopes at $(2n-1)t'_f$, and the lines for the plateau waveforms are determined by the voltages and slopes at $2nt'_f$.

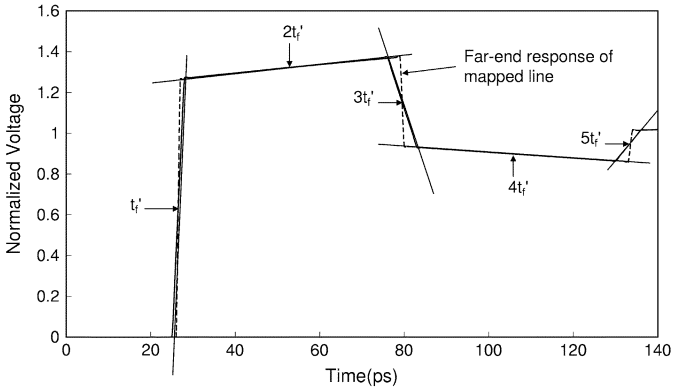

Fig. 4. Illustration of the PWL model.

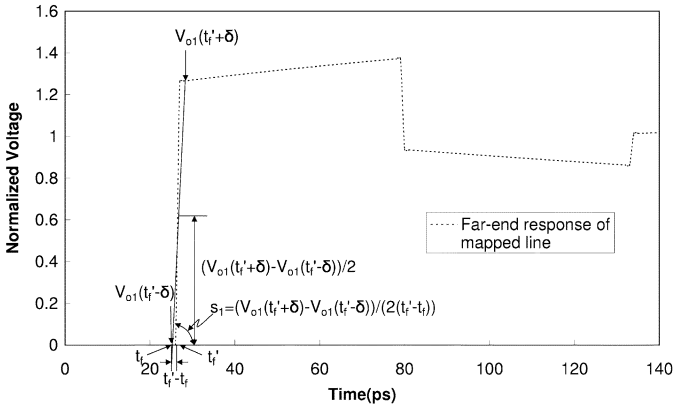

Fig. 5. Computation of the slope and voltage at t'_f.

Our algorithm works as follows. We first compute the waveform voltages and slopes at $nt'_f, (n = 1, 2, 3, \ldots)$. Then, we draw straight lines passing through these points with the calculated slopes. Finally, we obtain the crossing points of adjacent lines, and approximate the waveform by connecting these crossing points. Fig. 4 illustrates the process.

In the following, we explain how to compute the voltages and slopes at $nt'_f (n = 1, 2, \ldots)$ for the PWL model. Without losing generality, we assume input signal rises from 0 to $V_{\rm dd}$. In Fig. 5, we illustrate the computation of the slope at t'_f. At this time point, the voltage rises from 0 to $V_{o1}(t'_f + \delta)$, where δ is a small quantity of time and chosen to be $0.001t_f$ in our model. Because of the loading capacitance, the rising of the voltage is not steep but slower with a finite slope. To determine the slope, we approximate the time when the voltage reaches the 50%

$$t'_f = \sqrt{L'C'}$$
$$= \sqrt{\left(LC + \frac{R^2C^2}{12} + R_dRC_LC + \frac{(R_dC + C_LR)RC}{3} + 2C_LL - \frac{R^2C'^2}{12} - \frac{R_dRC'^2}{3}\right)} \quad (9)$$

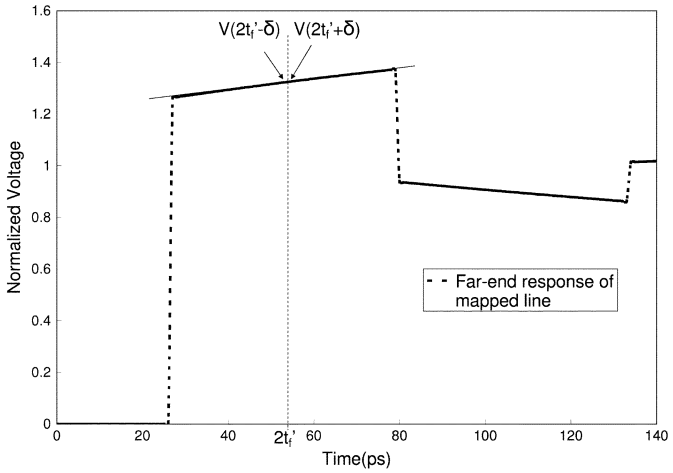

Fig. 6. Computation of the slope and voltage at $2t'_f$.

of the amplitude of the voltage rise by t'_f, which is the effective time of flight with the loading. Physically, the signal reaches the far end at time t_f, which is the real time of flight of the transmission line and the starting point of the voltage rise. Therefore, we obtain the slope at t'_f as

$$s_1 = \frac{\frac{V_{o1}(t'_f+\delta)}{2}}{t'_f - t_f} = \frac{V_{o1}(t'_f+\delta)}{2(t'_f - t_f)} \tag{11}$$

where the voltage $V_{o1}(t'_f + \delta)$ is computed by the formula from [14]. The voltage at t'_f is approximated by half of the rise as

$$v_1 = \frac{V_{o1}(t'_f+\delta)}{2}. \tag{12}$$

To solve the slope and voltage at $2t'_f$, we approximate the waveform in region $(t'_f, 3t'_f)$ by the response of the transformed open-ended line directly. As shown in Fig. 6, by the finite difference method we solve the slope at $2t'_f$ as

$$s_2 = \frac{dV_{o1}(2t'_f)}{dt} = \frac{V_{o1}(2t'_f+\delta) - V_{o1}(2t'_f-\delta)}{2\delta} \tag{13}$$

and the voltage at $2t'_f$ as

$$v_2 = \frac{V_{o1}(2t'_f+\delta) + V_{o1}(2t'_f-\delta)}{2}. \tag{14}$$

In this case, the approximating line is the tangent line at $2t'_f$.

The slope at $3t'_f$ is computed in the similar way as that at t'_f. However, because the rapid voltage change at $3t'_f$ in the far-end response comes from the reflected wave which has traveled a round trip along the line, we approximate the time to reach 50% of the falling by $2(t'_f - t_f)$ instead of $(t'_f - t_f)$. Therefore, the slope at $3t'_f$ is

$$s_3 = \frac{\frac{V_{o1}(3t'_f+\delta)-V_{o1}(3t'_f-\delta)}{2}}{2(t'_f - t_f)} = \frac{V_{o1}(3t'_f+\delta) - V_{o1}(3t'_f-\delta)}{4(t'_f - t_f)} \tag{15}$$

and the voltage at $3t'_f$ is approximated by

$$v_3 = \frac{V_{o1}(3t'_f+\delta) + V_{o1}(3t'_f-\delta)}{2}. \tag{16}$$

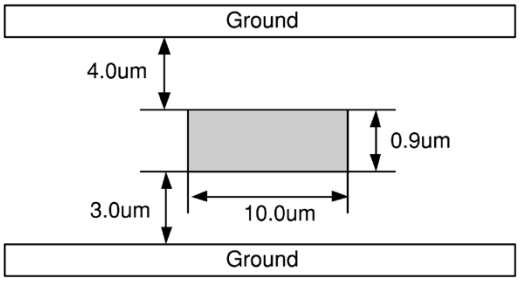

Fig. 7. Transmission line structure used in experiments.

The rest of the regions are calculated in the similar fashion. Regions $((2n-1)t'_f - \delta, (2n-1)t'_f + \delta)$ are similar to the region $(3t'_f - \delta, 3t'_f + \delta)$, where the slope and voltage are

$$\begin{aligned} s_{2n-1} &= \frac{V_{o1}\Big((2n-1)t+\delta\Big) - V_{o1}\Big((2n-1)t-\delta\Big)}{4(t'_f - t_f)} \\ v_{2n-1} &= \frac{V_{o1}\Big((2n-1)t+\delta\Big) - V_{o1}\Big((2n-1)t-\delta\Big)}{2}. \end{aligned} \tag{17}$$

Regions $((2n-1)t'_f, (2n+1)t'_f)$ are similar to the region $(t'_f, 3t'_f)$, where the slope and voltage are

$$\begin{aligned} s_{2n} &= \frac{V_{o1}\Big((2n)t'_f+\delta\Big) - V_{o1}\Big((2n)t'_f-\delta\Big)}{2\delta} \\ v_{2n} &= \frac{V_{o1}\Big((2n)t'_f+\delta\Big) + V_{o1}\Big((2n)t'_f-\delta\Big)}{2}. \end{aligned} \tag{18}$$

After obtaining the slopes and voltages for all the regions, the PWL waveform is readily constructed from all the straight lines determined by these slopes and voltages.

To verify the PWL model, we compare the far-end responses from the PWL model with the results of SPICE simulation [14], [16]. The experiments are carried out on a transmission line with $R = 1.92$ mΩ/μm, $C = 0.302$ fF/μm, and $L = 0.155$ pH/μm. We obtain these parameters by assuming that the transmission line has the structure shown in Fig. 7. The wire dimensions are the same as those in the redistribution layer (RDL) in TSMC 0.13-μm technology [20], and *R*, *L*, and *C* are extracted by FastHenry [21] and FastCap [22]. In SPICE simulations, the transmission line is modeled by uniform distributed *RLC* segments. Each segment is 5 μm long. We experiment with different wire lengths, driver sizes, and loading capacitances. We show an underdamped waveform in Fig. 8 and an overdamped waveform in Fig. 9, respectively. From the figures, the PWL model produces the best results that are very close to SPICE waveforms in both underdamped and overdamped cases. The waveforms from PWL model deviate slightly from SPICE simulation results around the knee points because of the PWL property of the model. The waveforms from [16] deviate from the SPICE simulation results greatly. This is because the waveform construction in [16] is based on a three-pole model which is not a good approximation when the transmission line effects are significant. [14] gives better results than [16], but it still has large errors due to the lack of considering capacitive loading. To quantitatively compare the waveforms, we also compute the average voltage difference compared to SPICE simulation for the waveforms in Figs. 8 and 9 between $t = t_f$ and $t = 300$ ps (the voltage is 0 V before $t = t_f$ and stable at $V_{\rm dd}$ after $t = 300$ ps) and show the results in Table II. From the table, the voltage difference of the PWL model is less than 0.9% $V_{\rm dd}$, which is at least 3× smaller than those of [16] and [14].

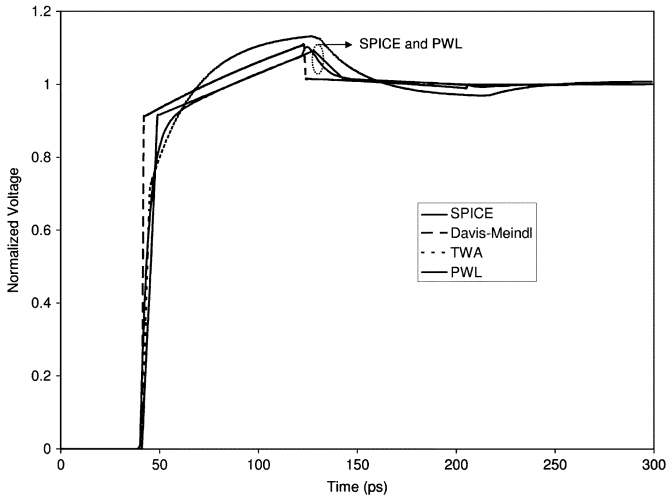

Fig. 8. Underdamped far-end waveform of a step input. $l = 6000\ \mu$m, $R_d = 16\ \Omega, C_L = 0.2$ pf.

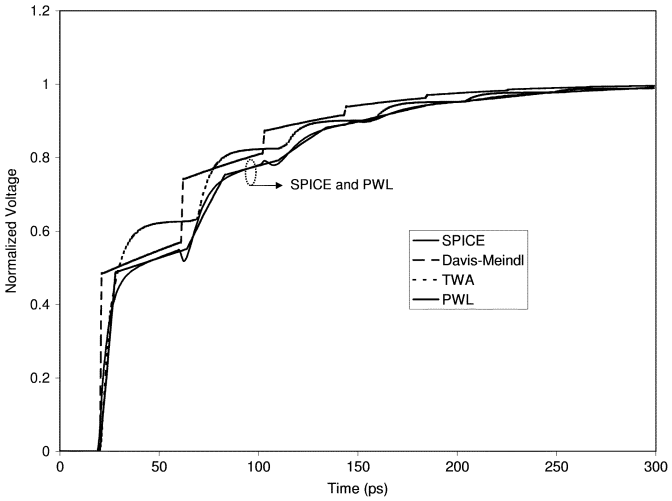

Fig. 9. Overdamped far-end waveforms of a step input. $l = 3000\ \mu$m, $R_d = 60\ \Omega, C_L = 0.2$ pf.

TABLE II
AVERAGE VOLTAGE DIFFERENCE IN $\%V_{\rm dd}$

Model	Fig.8	Fig.9
Davis-Meindl	0.025	0.013
TWA	0.030	0.027
PWL	0.009	0.004

D. PWL Model for Ramp Response

Based on the step response, we can further compute the ramp response with a finite rising time t_{ri}. As shown in Fig. 10, the input waveform has two knee points at $t = 0$ and $t = t_{ri}$. Correspondingly, the far-end response waveform has knee points at $(2n-1)t_f$ and $(2n-1)t_f + t_{ri} (n = 1, 2, 3, \ldots)$ as shown in Fig. 10. Therefore, according to the time of flight and input rising time, we divide the time domain into a series of regions with the boundary points of $(2n-1)t_f$ and $(2n-1)t_f + t_{ri}, (n = 1, 2, 3, \ldots)$ (The order of these time points depends on the detailed values of t_f and t_{ri}). Similar to the step response in Section II-C, we approximate the waveform in each region with a straight line. Based on this observation, we construct the PWL waveform for a ramp input as follows. We first find the voltage

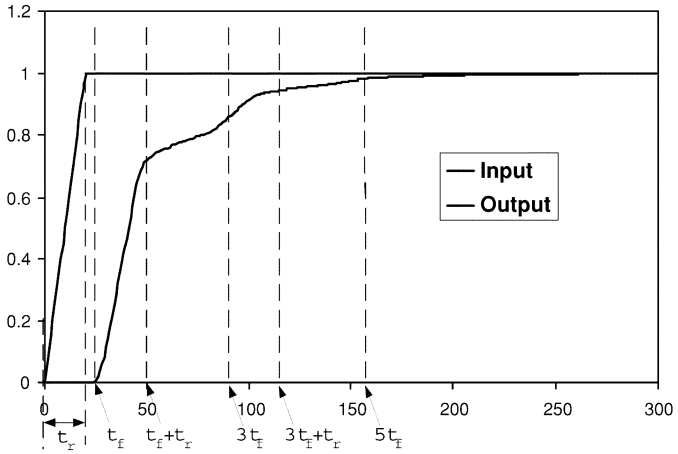

Fig. 10. Regions of ramp response.

and slope at the middle point of each region, and then approximate the waveform by a straight line passing through the point with the computed slope and voltage. The entire waveform is then approximated by connecting the crossing points of adjacent lines.

In the following, we explain how to compute the slopes and voltages for the ramp response. From the linear circuit theory [17], the ramp response can be computed from the step response by the following formula

$$V_{o2}(t) = \int_{-\infty}^{\infty} V_{o1}(t) \frac{dV_i(t-\tau)}{dt} dt = \frac{1}{t_{ri}} \int_{t-t_{ri}}^{t} V_{o1}(t)\, dt \tag{19}$$

where V_{o1} is the step response. Because we have already obtained the PWL waveform of the step response V_{o1} in Section II-C, we can compute the slope and voltage efficiently without resorting to the Bessel function-based formula (2). Taking the derivative of (19) on both sides, we obtain the slope of the ramp response at time t as

$$\frac{dV_{o2}(t)}{dt} = \frac{V_{o1}(t) - V_{o1}(t - t_{ri})}{t_{ri}}. \tag{20}$$

Because $V_{o1}(t)$ is a PWL waveform, the integration in (19) can be computed easily as a sum and the voltage of the ramp response at time t is

$$V_{o2}(t) = \frac{1}{t_{ri}} \sum_{(t_i, t_{i+1}) \subseteq (t-t_{ri}, t)} \frac{V_{o1}(t_i) + V_{o1}(t_{i+1})}{2} (t_{i+1} - t_i) \tag{21}$$

where (t_i, t_{i+1}) is a linear piece in the PWL expression of $V_{o1}(t)$ in $(t - t_{ri}, t)$. Because of the simplicity of (20) and (21), the computation of ramp response from step response is extremely efficient. We compute the slope and voltage at the middle point of each region defined above, and then construct the ramp response with the straight lines determined by the slopes and voltages.

To verify the PWL model for ramp response, we compare the waveform from the PWL model with the results of SPICE [14], [16]. We carry out experiments on the same structure shown in Fig. 7. We show an underdamped waveform in Fig. 11 and an overdamped waveform in Fig. 12. From the figures, the PWL model again produces the waveforms closest to the results of SPICE simulation in both cases. The waveforms from both [14] and [16] deviate from the results of SPICE simulation greatly due to both the lack of consideration of ramp input and the inaccuracy of the models discussed in Section II-C. Table III

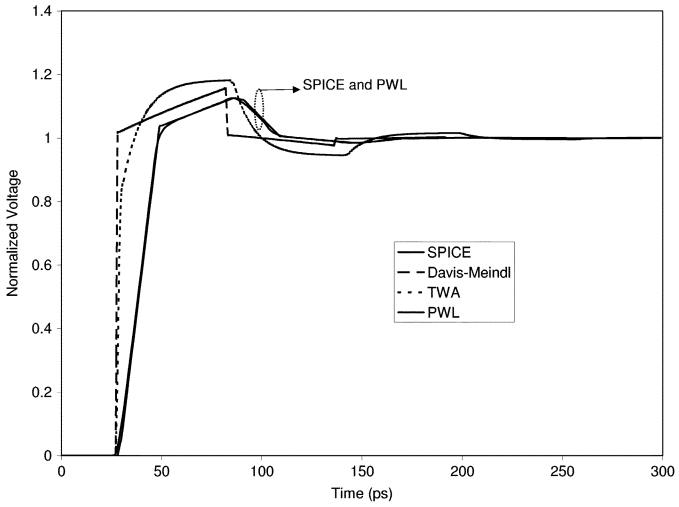

Fig. 11. Underdamped ramp response. $l = 4000\ \mu$m, $R_d = 15\ \Omega, C_L = 0.1$ pf. Input rising time is 20 ps.

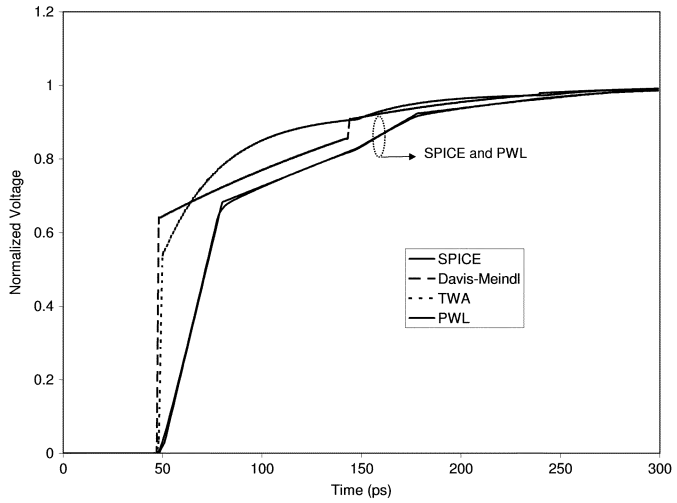

Fig. 12. Overdamped ramp response. $l = 7000\ \mu$m, $R_d = 30\ \Omega, C_L = 0.3$ pf, Input rising time is 30 ps.

TABLE III
AVERAGE VOLTAGE DIFFERENCE IN $\%V_{\rm dd}$

Model	Fig.11	Fig.12
Davis-Meindl	0.064	0.059
TWA	0.059	0.072
PWL	0.005	0.002

shows the average voltage difference for different models. From the table the voltage difference of the PWL model is less than 0.5% $V_{\rm dd}$ which is much smaller than those of [14] and [16].

We further study the error margin introduced by the transformation from the original loaded transmission line to an open-ended line In Figs. 13–15, we show the far-end rising time, 50% delay and oscillation amplitude computed from both SPICE and the PWL model with different loadings and wire lengths. The geometry of the wire is the same as in Fig. 7. The unit of loading is the minimum inverter size. From Figs. 13 and 14, it is clear that the model is highly accurate compared to SPICE in terms of rising time and 50% delay. The model has relatively larger error when the loading becomes larger. However, the maximum relative error is only 6.5%. With regard to oscillation amplitude, the PWL model is highly accurate compared to SPICE when the loading is less than 300×, and the error is less than 10% according to Fig. 14. When the loading becomes larger and the oscillation amplitude becomes smaller, the relative error increases. However, the maximum absolute error is less than 2% $V_{\rm dd}$. Since the loading of an on-chip interconnect is normally smaller than 1000× of the minimum inverter, the PWL model can be safely applied to model on-chip transmission lines with small errors.

III. APPLICATIONS OF PWL MODEL

In this section, we first apply the PWL model to analyze the CPW and then multiple coupled *RLC* lines sandwiched between two ground planes. We model the two interconnect structures by transmission lines and use the PWL model to solve the transmission lines. We compare the results with SPICE simulation under the distributed *RLC* circuit models for the two interconnect structures. Clearly, the errors in the experiments include those from circuit modeling and the PWL model. This is different from the comparison in Section II where an transmission line is assumed and no error of circuit modeling is considered.

A. Analysis of CPW

1) Circuit Model: With increasing clock frequency, CPW clock tree becomes common practice to overcome the issues of signal integrity. As shown in Fig. 16, a CPW consists of a central signal wire (S) sandwiched between two grounded shielding wires (G), where l is the length of the wires, h is the thickness of the wires, s is the spacing between the signal wire and the shielding wires, and w and g are the widths of the signal wire and the shielding wire respectively. The CPW structure can be modeled by self and coupling parasitics as shown in Fig. 17. R_s, C_s, and L_s are the self resistance, ground capacitance, and self inductance of the signal wire. R_g and L_g are the self resistance and inductance of the shielding wires. $C_{\rm sg}$ and $L_{\rm sg}$ are the coupling capacitance and coupling inductance between the signal wire and a shielding wire. $L_{\rm ss}$ is the coupling inductance between the two shielding wires. Such a model is complicated to analyze. Noticing that in a CPW structure most current on the signal wire returns from the shielding wires, we can assume all the current returns from the shielding wires and thus model the CPW as a single transmission line as shown in Fig. 2 but with the parameters defined by the following effective loop parasitics [23], [17]

$$\begin{aligned} R &= R_s + R_g/2 \\ L &= L_s - 2L_{\rm sg} + \frac{L_{\rm gg}}{2} + \frac{L_g}{2} \\ C &= 2C_{\rm sg} + C_s. \end{aligned} \tag{22}$$

2) Calculation of Delay, Rising Time, and Oscillation Amplitude: With the single transmission line model (22)–(22), we compute the far-end response of CPW structures with the PWL model. After obtaining the waveform, the delay, rising time, and oscillation amplitude can be easily computed by linear interpolation. To achieve high efficiency, we do not need to compute the whole waveform. Instead, we take a need-based approach based on the PWL model. In this approach, a knee point is calculated only when it is needed by the computation. For example, the maximum overshoot will happen around $3t_f'$, so calculating the knee points up to $4t_f'$ is needed. Similarly, maximum undershoot will happen around $5t_f'$, thus we only need to calculate the regions up to $6t_f'$. To compute the delay t_{do} and the rising time t_{ro}, we just need to calculate the knee points till the voltage meet the corresponding bound, for example, 90% for t_{ro}.

3) Runtime: The runtime of the PWL model is proportional to the number of linear segments computed. The most time-consuming computation in the model is the calculation of the modified Bessel functions when constructing the step response. Four points need to be com-

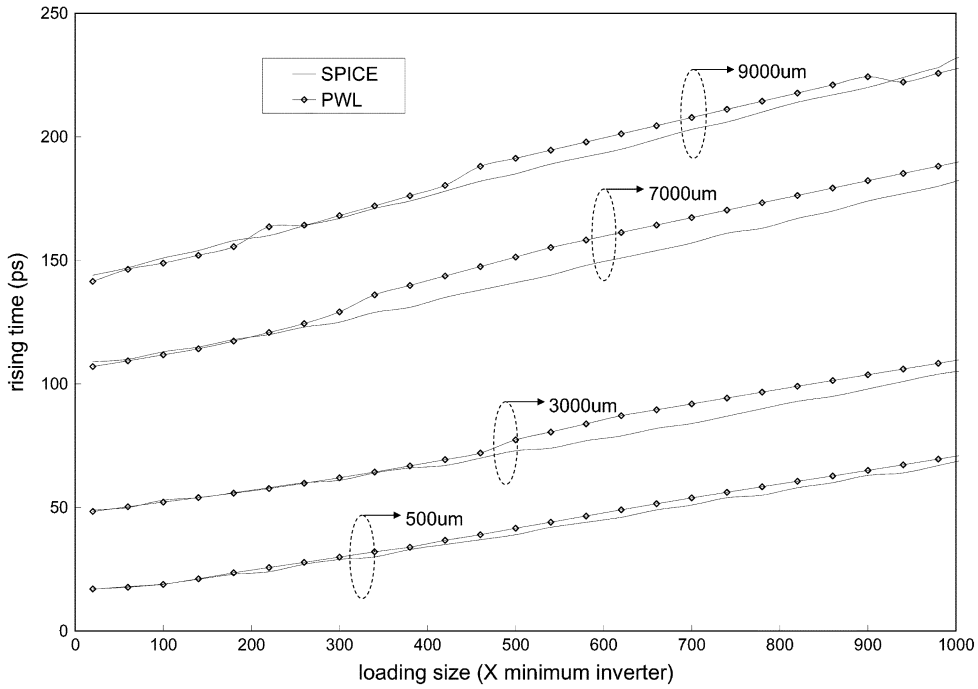

Fig. 13. Rising time for different loadings. $R_d = 30\ \Omega$. Input rising time is 20 ps.

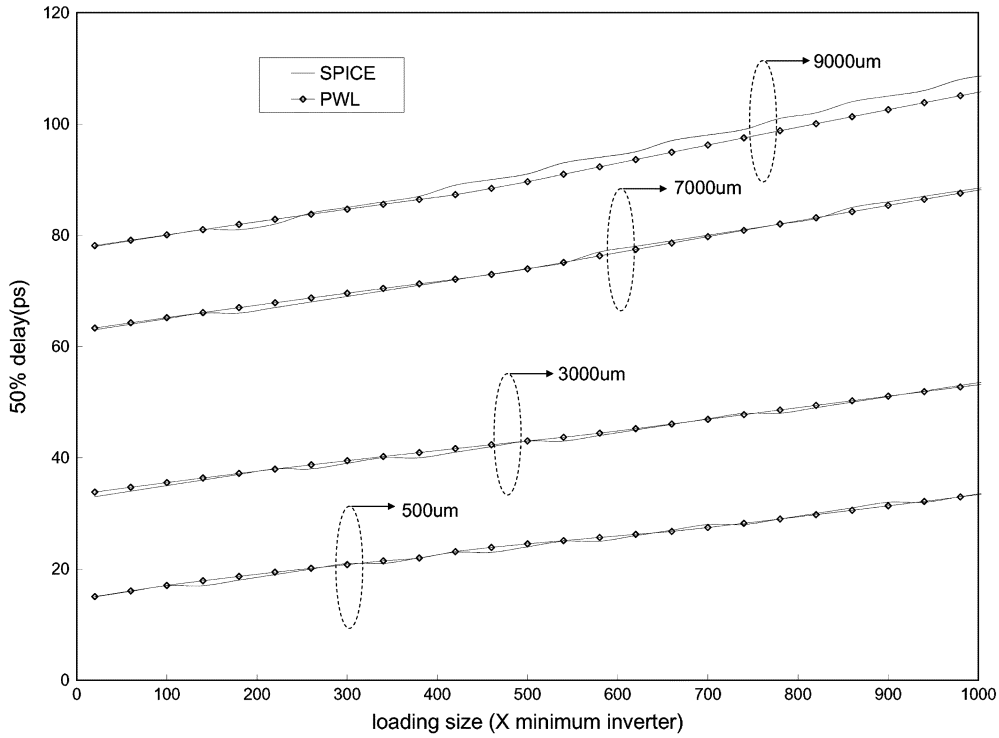

Fig. 14. Delay for different loadings. $R_d = 30\ \Omega$. Input rising time is 20 ps.

puted based on the modified Bessel function for each region defined in Section II. However, with the need-based procedure discussed in Section III-A2, we only need to calculate a few regions to obtain the delay, rising time, and noise, thus the algorithm is very efficient as will be shown in the next section.

4) Experiments: We carry out a set of experiments to compare the runtime and accuracy of the PWL model to SPICE simulation and the efficient models [16], [14]. In SPICE simulation, both the signal wire and the ground wires are modeled by uniformly distributed *RLC* segments. Each segment is 5 μm long. The coupling between wires is modeled by mutual inductance and capacitance as shown in Fig. 17. The wire thickness is 1 μm in our experiments. We present some sample CPW structures in Table IV and summarize the experiment results in Table V. According to Table V, both our model and [16] are at least 1000$\times$ faster than SPICE, and [14] is about 100$\times$ faster than SPICE. The error of the PWL model is less than 10% for delay and noise, and is less than 20% for rising time in the worst case. The PWL model sometimes obtains smaller rising time compared to SPICE simulation. This

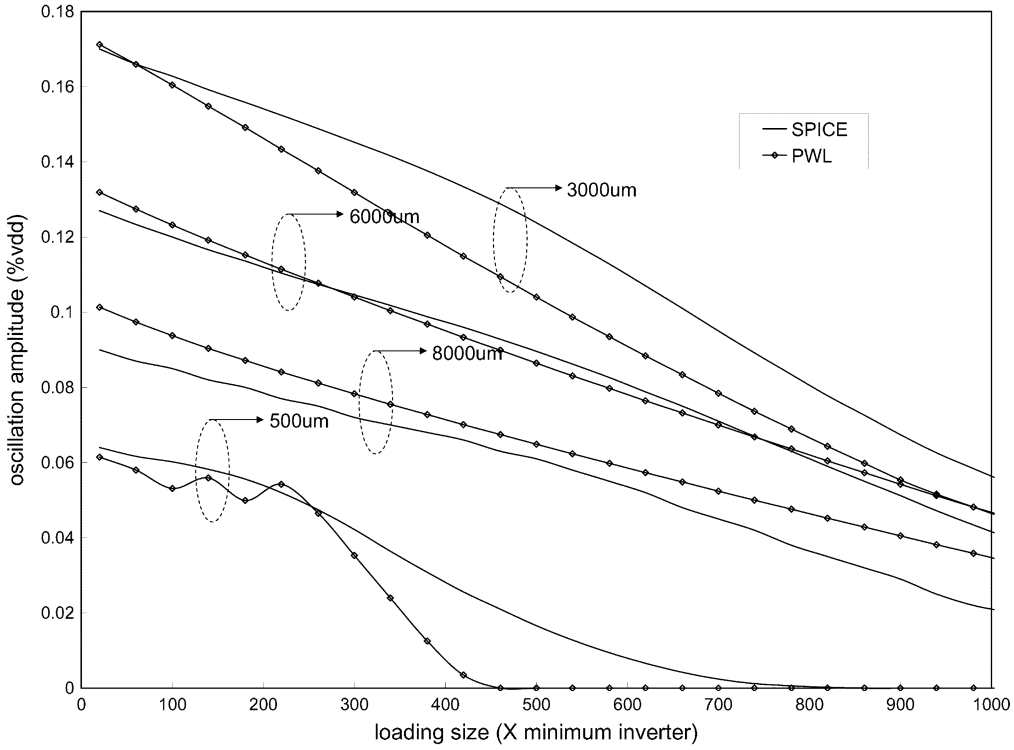

Fig. 15. Noise for different loadings. $R_d = 15\ \Omega$. Input rising time is 20 ps.

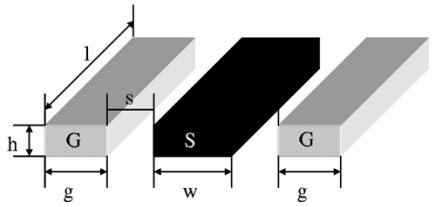

Fig. 16. CPW structure.

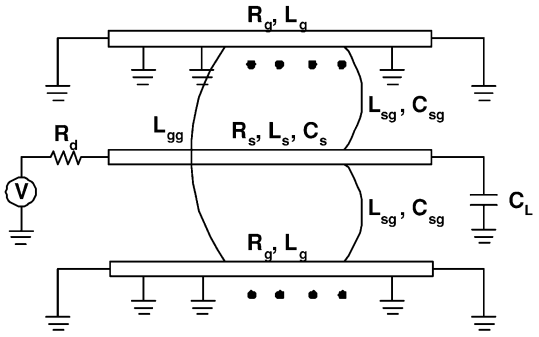

Fig. 17. Circuit model of CPW.

is because the time point of 90% $V_{\rm dd}$ happens to be around the knees. The error is normally less than 20% however. In contrast, both [16] and [14] can introduce significantly large errors in delay, rising time and oscillation amplitude. The PWL model reduces errors by 90% on average compared to [14] and [16].

B. Analysis of Multiple Coupled Lines

On-chip global buses are normally long and wide. Because strong inductive coupling exists between these wires, the signal integrity of such structures is a great concern in modern VLSI designs. Because a parallel bus cannot be modeled as individual transmission lines due to the coupling between wires, we can not directly apply the PWL model to analyze the bus structure. However, with the decoupling technique in [18] we can transform multiple aligned lines to independent transmission lines, on which we can apply the PWL model. In this section, we combine this decoupling technique and the PWL model to analyze multiple coupled transmission lines. According to the transformation in [18], we first transform the coupled lines to the same number of decoupled lines with independent drivers and loadings, and then we analyze each decoupled transmission line with the PWL model, and finally obtain the response of the original coupled lines by linear combination of the responses of the decoupled lines.

TABLE IV
SAMPLE EXPERIMENT SETTINGS (ALL GEOMETRIES ARE IN MICROMETERS)

setting	l	w	s	g	$R_d(\Omega)$	$C_L(fF)$	$t_{ri}(ps)$
1	3000	6	1	4	30	45	0
2	5000	10	2	5	40	45	0
3	10000	8	2	8	24	90	0
4	1000	8	1	4	60	90	30
5	5000	10	2	10	24	45	30
6	10000	10	1	10	24	90	30

We carry out experiments on a five-net structure shown in Fig. 18. All the lines are aligned and identical with the same drivers and loadings. The length of the lines is 5000 μm and the spacings between the lines are 1.0 μm. The driver resistance is 30 Ω and the loading capacitance is 0.2 pF. The rising time of inputs is 30 ps. As an example, we show the result of one experiment in Figs. 19 and 20. In this example, line 2 switches from ground to $V_{\rm dd}$, line 3 switches from $V_{\rm dd}$ to ground and all other lines are held to the ground at the near end. We compare the results from the PWL model with those obtained from SPICE simulations. In SPICE simulation, we model each transmission line with uniformly distributed *RLC* segments. Each segment is 5 μm long. The coupling between wires is model by mutual inductance and capacitance. Fig. 19 shows the responses of the two aggressor nets 2 and 3. The waveforms from the PWL model and SPICE simulation match so well that it is

TABLE V
RUNTIME AND RESULTS FROM DIFFERENT MODELS. SPICE AND [14] CALCULATE UP TO 300 ps BY TIME STEPPING (1 ps/STEP)

Model		runtime (s)				50% delay (ps)				rising time (ps)				amplitude of oscillation ($\%Vdd$)			
setting	type	SPICE	PWL	[16]	[14]	SPICE	PWL	[16]	[14]	SPICE	PWL	[16]	[14]	SPICE	PWL	[16]	[14]
1	underdamped	88.10	0.01	0.01	0.18	24	25	25	24	10	8	9	6	4.6	4.5	9.2	5.1
2	overdamped	148.10	0.01	0.01	0.18	42	42	42	41	83	83	46	80	0	0	0	0
3	underdamped	368.23	0.01	0.01	0.12	83	84	83	80	58	56	48	48	8.6	8.9	10.3	8.8
4	overdamped	23.23	0.01	0.01	0.73	33	33	12	9	47	47	26	26	0	0	0	0
5	underdamped	121.39	0.01	0.01	0.20	55	55	39	38	26	26	10	1	4.6	5.2	11.3	8.0
6	underdamped	344.70	0.01	0.01	0.02	112	113	96	93	28	25	26	1	13.5	14.2	16.7	15.7

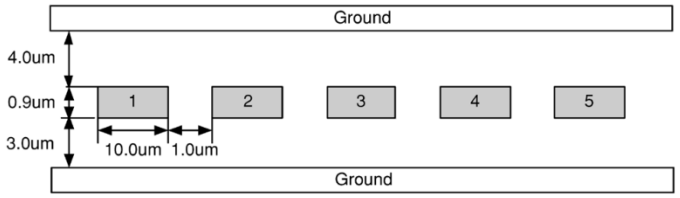

Fig. 18. Five coupled parallel transmission lines.

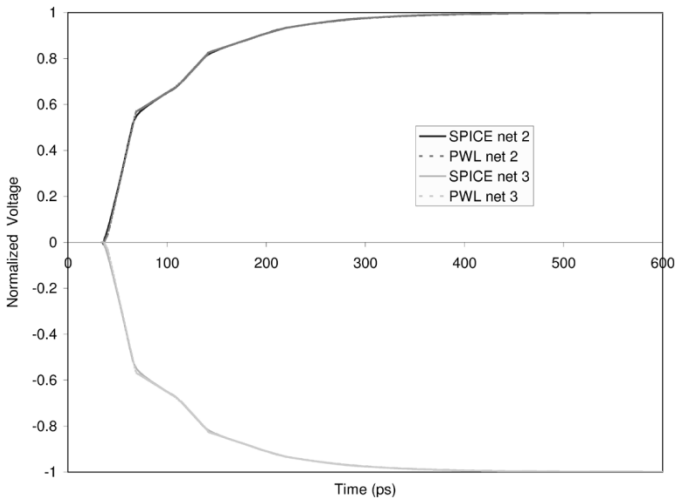

Fig. 19. Far-end response of aggressor nets 2 and 3.

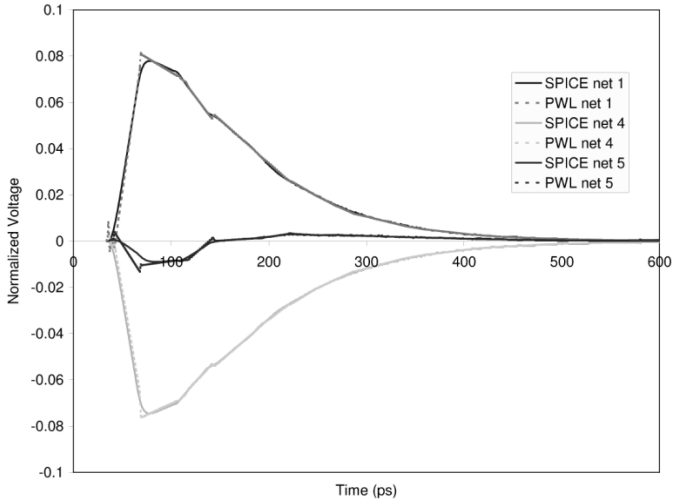

Fig. 20. Far-end response of victim nets 1, 4, and 5.

hard to distinguish them in the figures. Fig. 20 shows the responses of victim nets 1, 4, and 5. The PWL model still well matches the overall waveform shape with small discrepancy. The model deviates a little from the SPICE simulation around the first knee due to the PWL nature of the model, but it captures the rising edges, oscillation amplitude, and failing tails of the waveform almost perfectly.

IV. CONCLUSION

We have developed an efficient model for the far-end transient response of a single transmission line with capacitive loading and ramp inputs for high-speed on-chip interconnect analysis. The model divides the time axis into a number of regions according to the time of flight and input rising time, and approximates the response by PWL waveform. We call this model the PWL model. The waveform derived from the PWL model matches SPICE simulation result with the average voltage difference less than 0.9% $V_{\rm dd}$. The PWL model is at least 1000× faster than SPICE simulation. To the best of our knowledge, the PWL model is the first efficient transmission line model considering both loading capacitance and ramp inputs. We have further applied the PWL model to compute the delay, rising time and oscillation amplitude of the CPW structure. Experiments show the PWL model achieves less than 10% average error compared to SPICE simulation. Combining the PWL model and the decoupling technique, we also have computed the far-end responses of bus structures, and the resulting waveform almost perfectly matches the SPICE simulation result.

In this work we only considered capacitive loading. We will extend our model to consider more general terminations such as *RC* and *RLC* loading. Furthermore, we only considered linear drivers and receivers, but for on-chip applications the drivers and receivers are normally active devices. The nonlinearity of the devices will impact the accuracy of the model, and we plan to extend our model to consider the nonlinearity of drivers and loadings in our future work.

REFERENCES

[1] Y. I. Ismail and E. G. Friedman, *On-Chip Inductance in High Speed Integrated Circuits*. Norwell, MA: Kluwer, 2001.
[2] L. Shen and N. Chang, "Challenges in power-ground integrity," in *Proc. Int. Conf. Computer-Aided Design*, 2001, pp. 641–654.
[3] A. Deutsch *et al.*, "The importance of inductance and inductive coupling for on-chip wires," in *Proc. IEEE Elect. Perform. Electron. Packag.*, 1997, pp. 53–56.
[4] J. Schutt-Aine and R. Mittra, "Scattering parameter transient analysis of transmission lines loaded with nonlinear terminations," *IEEE Trans. Microwave Theory Tech.*, vol. 36, no. 3, pp. 529–536, Feb. 1988.
[5] J. Roychowdhury and D. Pederson, "Efficient transient simulation of lossy interconnect," in *Proc. Design Automation Conf.*, 1991, pp. 740–745.
[6] J. Roychowdhury, A. R. Newton, and D. O. Pederson, "An impulse-response based linear time-complexity algorithm for lossy interconnect simulation," in *Proc. Int. Conf. Computer-Aided Design*, 1991, pp. 62–65.
[7] F. Y. Chang, "Waveform relaxation analysis of RLCG transmission lines," *IEEE Trans. Circuits Syst.*, vol. 37, no. 11, pp. 1394–1415, Nov. 1990.
[8] M. J. Gander and A. E. Ruehli, "Solution of large transmission line type circuits using a new optimized waveform relaxation partitioning," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 2003, pp. 636–641.

[9] T. K. Tang, M. S. Nakhla, and R. Griffith, "Analysis of lossy multiconductor transmission lines using the asymptotic waveform evaluation technique," *IEEE Trans. Microwave Theory Tech.*, vol. 39, no. 12, pp. 2107–2116, Dec. 1991.

[10] S. K. Das and W. T. Smith, "Application of asymptotic waveform evaluation for analysis of skin effect in lossy interconnects," *IEEE Trans. Electromagn. Compat.*, vol. 39, no. 2, pp. 138–146, May 1997.

[11] S. Lin and E. S. Kuh, "Transient simulation of lossy interconnects based on the recursive convolution formulation," *IEEE Trans. Circuits Syst. I: Fundam. Theory Applicat.*, vol. 39, no. 11, pp. 879–892, 1992.

[12] A. Odabasioglu, M. Celik, and L. Pileggi, "PRIMA: Passive reduced-order interconnect macromodeling algorithm," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 17, no. 8, Aug. 1998.

[13] A. Kahng and S. Muddu, "An analytical delay model for *RLC* interconnects," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1996, pp. 237–240.

[14] J. A. Davis and J. D. Meindl, "Compact distributed *RLC* interconnect models. I. Single line transient, time delay, and overshoot expressions," *IEEE Trans. Electron Devices*, no. 11, pp. 2068–2077, Nov. 2000.

[15] R. Venkatesan, J. A. Davis, and J. D. Meindl, "A physical model for the transient response of capacitively loaded distributed *RLC* interconnects," in *Proc. Design Automation Conf*, 2001, pp. 763–766.

[16] Y. Eo, J. Sim, and W. R. Eisenstadt, "A traveling-wave-based waveform approximation technique for the timing verification of single transmission lines," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 21, no. 6, pp. 723–730, Jun. 2002.

[17] R. Escovar and R. Suaya, "Transmission line design of clock trees," in *Proc. Int. Conf. Computer-Aided Design*, 2002, pp. 334–340.

[18] J. Chen and L. He, "A decoupling method for analysis of coupled RLC interconnects," in *Proc. Great Lakes Sympos. VLSI*, 2001, pp. 41–46.

[19] H. You and M. Soma, "Crosstalk analysis of interconnection lines and packages in high-speed integrated circuits," *IEEE Trans. Circuits Syst.*, vol. 37, no. 8, pp. 1019–1026, Aug. 1990.

[20] TSMC Processing Technology [Online]. Available: http://www.tsmc.com/english/technology/t01.htm

[21] M. Kamon, M. Tsuk, and J. White, "Fasthenry: A multipole-accelerated 3-D inductance extraction program," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 9, pp. 1750–1758, Sep. 1994.

[22] K. Narbos and J. White, "FastCap: A multipole accelerated 3-D capacitance extraction program," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 10, no. 11, pp. 1447–1459, Nov. 1991.

[23] L. He, N. Chang, S. Lin, and O. S. Nakagawa, "An efficient inductance modeling for on-chip interconnects," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 1999, pp. 457–460.

Delay Analysis of CMOS Gates Using Modified Logical Effort Model

A. Kabbani, D. Al-Khalili, and A. J. Al-Khalili

***Abstract*—In this paper, modified logical effort (MLE) technique is proposed to provide delay estimation for CMOS gates. The model accounts for the behavior of series-connected MOSFET structure (SCMS), the input transition time, and internodal charges. Also, the model takes into account deep submicron effects, such as mobility degradation and velocity saturation. This model exhibits good accuracy when compared with Spectre simulations based on BSIM3v3 model. Using UMC's 0.13-μm and TSMC's 0.18-μm technologies, the model has an average error of 4.5% and a maximum error of 15%.**

***Index Terms*—CMOS, delay model, DSM, logic gates, logical effort.**

I. Introduction

The evolution of CMOS technology allows designs with millions of gates to be integrated on a single chip. The performance of such designs is greatly affected by the optimization process at each design level of abstraction. This in turn is influenced by the used technology library in terms of efficiency and proper driving strength [1]. Modeling of cell performance is a crucial issue in circuit optimization. In particular, it is useful to characterize the performance of the cells of the newly emerging virtual library technique [2]–[5]. In this technique, cells are initially generated on the fly without defining transistor dimensions. These dimensions are then determined in a subsequent phase based on a user defined cost function. In order to achieve optimized transistor sizing, an efficient technique to predict and characterize the performance of these cells is needed.

Many authors have tackled CMOS gate delay modeling. Relying on the nth power current model, a closed-form expression is developed in [6]–[8] to model the delay in series-connected MOSFET structure (SCMS). However, the nth power model depends on many extracted device-dependent parameters which need to be determined through simulation. The models in [6] and [7] depend on a degradation factor to extend CMOS inverter delay to SCMS. The effect of the internal node prarasitics on the degradation factor is introduced in [8]. Meanwhile, in [9], the PMOS and NMOS structures are replaced by equivalent transistors that have the same dc characteristics and parasitics. In [10], a technique to reduce complex CMOS gates into equivalent inverters is introduced. This technique depends on the α power model to predict the transistor widths of the equivalent inverter, but it does not provide a delay model for CMOS gates [8]. Another technique to model the behavior of CMOS gates is presented in [11]. This model introduces many parameters that need to be extracted by simulation such as the drive ability of the transistors and the pseudo empirical coefficients to account for the nonlinear relationship between the delay and the ramp input duration.

Manuscript received April 1, 2004; revised June 29, 2004. This paper was recommended by Associate Editor D. Blaauw.

A. Kabbani is with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON M5B 2K3 Canada (e-mail: adnan@ee.ryerson.ca).

D. Al-Khalili is with the Department of Electrical and Computer Engineering, Royal Military College, Kingston, ON K7K 7B4 Canada (e-mail: alkhalili-d@rmc.ca).

A. J. Al-Khalili is with the Department of Electrical and Computer Engineering, Concordia University, Montreal, PQ H3G 1M8 Canada (e-mail: asim@ece.concordia.ca).

Digital Object Identifier 10.1109/TCAD.2005.847892