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## A Provably Passive and Cost-Efficient Model for Inductive Interconnects

Hao Yu and Lei He

**Abstract**—To reduce the model complexity for inductive interconnects, the vector potential equivalent circuit (VPEC) model was introduced recently and a localized VPEC model was developed based on geometry integration. In this paper, the authors show that the localized VPEC model is not accurate for interconnects with nontrivial sizes. They derive an accurate VPEC model by inverting the inductance matrix under the partial element equivalent circuit (PEEC) model and prove that the effective resistance matrix under the resulting full VPEC model is passive and strictly diagonal dominant. This diagonal dominance enables truncating small-valued off-diagonal elements to obtain a sparsified VPEC model named truncated VPEC (tVPEC) model with guaranteed passivity. To avoid inverting the entire inductance matrix, the authors further present another sparsified VPEC model with preserved passivity, the windowed VPEC (wVPEC) model, based on inverting a number of inductance submatrices. Both full and sparsified VPEC models are SPICE compatible. Experiments show that the full VPEC model is as accurate as the full PEEC model but consumes less simulation time than the full PEEC model does. Moreover, the sparsified VPEC model is orders of magnitude (1000×) faster and produces a waveform with small errors (3%) compared to the full PEEC model, and wVPEC uses less (up to 90×) model building time yet is more accurate compared to the tVPEC model.

**Index Terms**—Circuit simulation, inductance sparsification, interconnect modeling.

### I. INTRODUCTION

As very large scale integration (VLSI) technology advances with decreasing feature size as well as increasing operating frequency, inductive effects of on-chip interconnects become increasingly significant in terms of delay variations, degradation of signal integrity, and aggravation of signal crosstalk [1], [2]. Since inductance is defined with respect to the closed current loop, the loop–inductance extraction needs to simultaneously specify both the signal net current and its returned current. To avoid the difficulty of determining the path of the returned current, the partial element equivalent circuit (PEEC) model [3] can be

used, where each conductor forms a virtual loop with the infinity and the partial inductance is extracted.

To accurately model inductive interconnects in the high frequency region, resistor–inductor–capacitor–mutual inductance (RLCM) networks under the PEEC formulation are generated from discretized conductors by volume decomposition according to the skin depth and longitudinal segmentation according to the wavelength at the maximum operating frequency. The extraction based on this approach [4]–[6] has high accuracy but typically results in a huge RLCM network with densely coupled partial inductance matrix  $L$ . A dense inductively coupled network sacrifices the sparsity of the circuit matrix and slows down the circuit simulation or makes the simulation infeasible. Because the primary complexity is due to the dense inductive coupling, efficient yet accurate inductance sparsification becomes a need for extraction and simulation of inductive interconnects in the high-speed circuit design.

Because the partial inductance matrix in the PEEC model is not diagonal dominant, simply truncating off-diagonal elements leads to negative eigenvalues and the truncated matrix loses passivity [7]. There are several inductance sparsification methods proposed with guaranteed passivity. The return-limited inductance model [8] assumes that the current for a signal wire returns from its nearest power/ground (P/G) wires. This model loses accuracy when the P/G grid is sparsely distributed. The shift truncation model [9] calculates a sparse inductance matrix by assuming that the current returns from a shell with shell radius  $r_0$ . But it is difficult to determine the shell radius to obtain the desired accuracy. Because the inverse of the inductance matrix called  $K$  element (susceptance) matrix is strictly diagonal dominant, off-diagonal elements can be truncated without affecting the passivity [10], [11]. Because  $K$  is a new circuit element not included in a conventional circuit simulator such as SPICE, new circuit analysis tools considering  $K$  have been developed [12], [13]. Alternatively, double-inversion-based approaches have been proposed in [11] and [14]. Using the control volume to extract adjacently coupled effective resistances to model inductive effects, the vector potential equivalent circuit (VPEC) model is recently introduced [15]. Its sparsified and SPICE-compatible circuit model is obtained based on a locality assumption that the coupling under the VPEC model exists only between adjacent wire filaments.

This paper presents an in-depth study on the VPEC model. The authors find that the locality assumption in [15] does not hold in general and its integration-based extraction becomes impractical for large-sized interconnects as it requires to optimize the size of the control volume for each filament. The authors rigorously derive an accurate full VPEC model considering the coupling between any pair of filaments by inverting the partial inductance matrix. The authors further prove that the resulting circuit matrix for the full VPEC model is passive and strictly diagonal dominant. The diagonal dominance enables truncating small-valued off-diagonal elements to obtain a sparsified VPEC model named truncated VPEC (tVPEC) model with guaranteed passivity. To avoid inverting the entire inductance matrix, the authors also present another sparsified VPEC model with preserved passivity, the windowed VPEC (wVPEC) model, by inverting a number of inductance submatrices. Both full and sparsified VPEC models are SPICE compatible.

The rest of this paper is organized as follows. Section II introduces an accurate inversion-based VPEC model with detailed derivation in the Appendix. The resulting full VPEC model considers coupling between any pair of filaments. In contrast, the VPEC model in [15] is integration based, localized but not accurate in general. In Section III, the authors prove that the effective resistance matrix  $\hat{G}$  in the full VPEC model is passive and strictly diagonal dominant. Section IV presents a truncation-based sparsification that leverages the passivity of the  $\hat{G}$  matrix. It

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TABLE I  
TABLE OF NOTATIONS

$a_i$	$i$ th filament
$A^k$	$k$ th component of vector potential $A$
$A_i^k$	$k$ th component of averaged $A$ at $a_i$
$\mathcal{B}_{ij}^k$	$k$ th component of the flux from $a_i$ to $a_j$
$\mathcal{B}_{i0}^k$	$k$ th component of the flux from $a_i$ to vector potential ground;
$I_i^k$	$k$ th component of electrical branch current at $a_i$
$\hat{I}_i^k$	$k$ th component of magnetic branch current at $a_i$
$\hat{R}_{ij}^k$	$k$ th component of coupling effective resistance between $a_i$ and $a_j$
$\hat{R}_{i0}^k$	$k$ th component of ground effective resistance of $a_i$
$V_i^k$	$k$ th component of electrical branch voltage at $a_i$
$\hat{V}_i^k$	$k$ th component of magnetic branch voltage at $a_i$

truncates small-valued off-diagonal elements of the  $\hat{G}$  matrix obtained from the full inversion of the inductance matrix. In Section V, the authors further present a more efficient sparsification approach based on windowing. It avoids inverting the full inductance matrix and is more efficient and more accurate compared to the truncation-based sparsification. Section VI further presents the scalability of the runtime and model size for the sparsified VPEC, full VPEC, and PEEC model. Finally, Section VII concludes the paper.

## II. INVERSION-BASED FULL VPEC MODEL

The VPEC model from [15] considering coupling only between adjacent filaments can be called the localized VPEC model. In this section, the authors first derive the system equation of the full VPEC to model the inductive effect between any pair of filaments and then show that the localization assumption in [15] does not hold in general. They then introduce the inversion-based method to calculate the full VPEC model. Finally, experiments are presented to show that the full VPEC is as accurate as the PEEC model.

### A. Full VPEC

Same as in FastHenry [5] with the magneto-quasi-static assumption, the conductor can be divided into a number of rectilinear filaments. The current density is constant over the cross section of the filament. In this paper, the authors use superscripts  $x, y, z$  to denote spatial components of a vector variable. Let  $\mathbf{A}$  be the vector potential determined by the distribution of the current density  $J$ . Then  $J^k$  and  $A^k$  are the components in the  $k$  direction ( $k = x, y, z$ ). The authors further use the subscript  $i$  for variables associated with filament  $a_i$  ( $i \in N$ ), and every filament  $a_i$  has a length  $l$  by adequately discretizing in the  $k$  direction. Table I summarizes the notations used in this paper with detailed definitions in the Appendix.

To extract the VPEC, the integration-based approach in [15] needs to determine the localized flux  $\mathcal{B}_{ij}^k$  ( $j \in n_i$ ), where  $n_i$  is the set of filaments adjacent to  $a_i$ . The explicit calculation of  $\mathcal{B}_{ij}^k$  is hard, and only considering the localized flux as in [15] loses the accuracy. The integration-based VPEC model in [15] needs to use a control volume for each filament, but no method was presented in [15] to find an accurate control volume. To avoid explicitly calculating  $\mathcal{B}_{ij}^k$  and using the locality assumption, the authors derive a full VPEC model and then present an inversion-based extraction in Section II-B. The detailed derivation of the full VPEC model is presented in the Appendix, where the authors obtain two Kirchhoff's current law (KCL) and Kirchhoff's current law (KVL) equations

$$\frac{A_i^k}{\hat{R}_{i0}^k} + \sum_{j \neq i, j \in N} \frac{(A_i^k - A_j^k)}{\hat{R}_{ij}^k} = \hat{I}_i^k \quad (1)$$

$$\frac{\partial A_i^k}{\partial t} = \hat{V}_i^k \quad (2)$$

where the vector potential current and voltage are related to the electrical branch current and voltage by

$$\hat{I}_i^k = I_i^k \quad \text{and} \quad \hat{V}_i^k = \frac{V_i^k}{l}. \quad (3)$$

Clearly, we can see the physical meaning of the effective resistance by (1): given a unit current change at the  $i$ th filament, the vector potential observed at the  $j$ th filament is exactly  $\hat{R}_{ij}^k$  when all other filaments are connected to vector potential ground. Furthermore, (2) describes the relation between the vector potential and its corresponding electrical voltage drop caused by the inductive effect.

The authors present a SPICE-compatible VPEC model for three filaments in Fig. 1. The model consists of two blocks: the electrical circuit (PEEC resistance and capacitance) and the magnetic circuit (VPEC effective resistance and unit inductance). They are connected by controlled sources. It includes the following components.

- 1) The resistance  $R_i$  and capacitance  $C_i$  in the electrical circuit are the same as those in the PEEC model.
- 2) A dummy voltage source to the sense current  $I_i^k$  in the electrical circuit controls  $\hat{I}_i^k$  in the magnetic circuit [see (32) in the Appendix].
- 3) A voltage-controlled current source is used to relate  $\hat{V}_i^k$  and  $\hat{I}_i^k$  with gain  $g = 1$  in the magnetic circuit.
- 4) A voltage source  $V_i^k$  in the electrical circuit is controlled by  $\hat{V}_i^k$  in the magnetic circuit [see (34) in the Appendix].
- 5) Effective resistances including ground  $\hat{R}_{i0}^k$  and coupling  $\hat{R}_{ij}^k$  [see (30) and (29) in the Appendix] are used to represent the strength of inductances in the magnetic circuit.
- 6) A unit inductance  $L_i$  in the magnetic circuit a) takes into account the time derivative of  $A_i^k$  [see (2)] and b) preserves the magnetic energy from the electrical circuit.

Although the number of magnetic circuit blocks increases with more filaments, sparsified VPEC models will be introduced in Sections III–V to greatly reduce coupling resistances in magnetic circuit blocks with preserved passivity. Moreover, because the VPEC model largely reduces reactive elements (i.e., inductance) and its effective resistance is less densely stamped in the modified nodal analysis (MNA) matrix compared to the partial inductance under the PEEC model, the full VPEC model reduces the simulation time compared to the PEEC model (see experiments in Section VI).

Note that the summation in KCL (1) for the full VPEC model is carried out over each pair of filaments. In contrast, this summation in [15] is carried out only for adjacent filaments. Pacelli [15] obtained the localized model by modeling the flux  $\mathcal{B}_{ij}^k$  as a “current” flow through  $\hat{R}_{ij}^k$ . It is based on the analogy with the conducting current flow at a surface  $S$  (Ohm's law)

$$\mathbf{I} = -\sigma \int_S \nabla \phi \cdot d\mathbf{S}. \quad (4)$$

Equation (4) means that the conducting current  $\mathbf{I}(x, y, z)$  is locally related to the flux of the electrical field  $\mathbf{E}(x, y, z)$  ( $-\nabla \phi$ ) on the surface  $S$ . Equation (4) is correct because electrons only locally transport in the conductor. However, for the magnetic coupling problem, the flux  $\mathcal{B}_{ij}^k$  is caused by the magnetic field that is not localized. Therefore, the authors still need nonlocal resistances to accurately model the long-range effect of inductance. Hence, the KCL (1) in this paper is related to not only the localized  $\hat{R}_{ij}^k$  ( $j \in n_i$ ) but also all other  $\hat{R}_{ij}^k$  ( $j \neq i, j \in N$ ). The experimental results below will show that compared to the PEEC model, the full VPEC model considering all filaments is accurate, but not the localized VPEC model from [15].

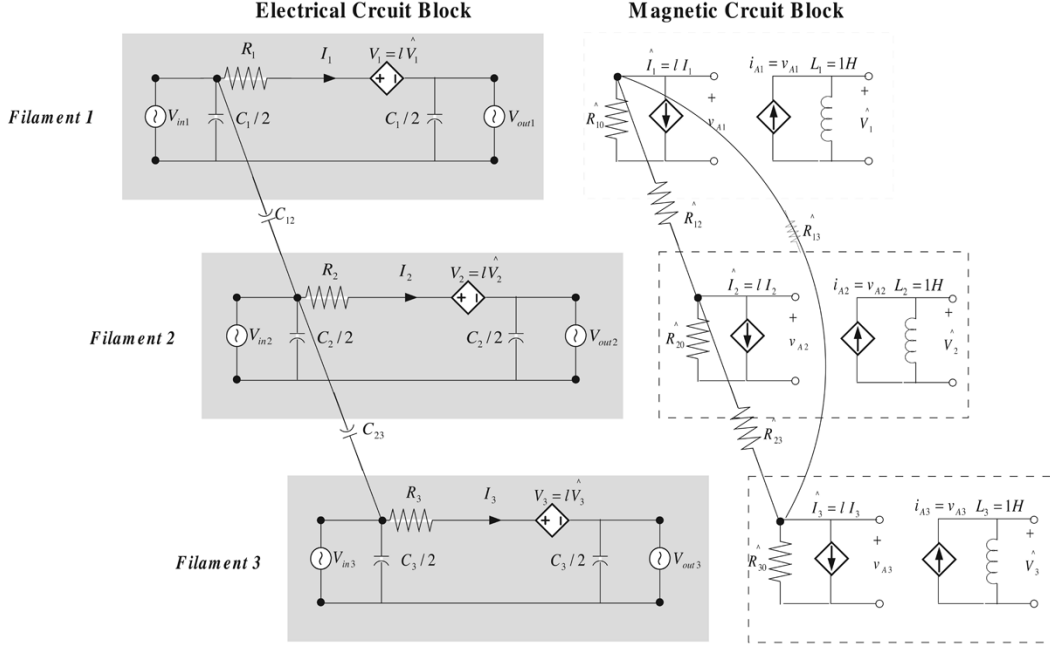


Fig. 1. VPEC model for three filaments.

### B. VPEC via PEEC Inversion

Due to the difficulty of explicitly determining  $\mathcal{B}_{ij}^k$ , there is no efficient calculation method for effective resistances in [15]. In this part, the authors will derive the circuit-level system equation based on the VPEC effective resistance matrix  $\hat{G}$  and then present an efficient method to calculate effective resistances from the inversion of the partial inductance matrix.

The authors take the time derivative at both sides of (1) and then use (2) to replace the time derivative of the vector potential. Consequently, the authors obtain

$$\left( \frac{1}{\hat{R}_{i0}^k} + \sum_{j \neq i} \frac{1}{\hat{R}_{ij}^k} \right) V_i^k + \sum_{j \neq i} \left( -\frac{1}{\hat{R}_{ij}^k} \right) V_j^k = l^2 \frac{\partial I_i^k}{\partial t}. \quad (5)$$

The authors define the circuit matrix  $\hat{G}$  of the VPEC model as

$$\hat{G}_{ij}^k = -\frac{1}{\hat{R}_{ij}^k}, \quad \hat{G}_{ii}^k = \left( \frac{1}{\hat{R}_{i0}^k} + \sum_{j \neq i} \frac{1}{\hat{R}_{ij}^k} \right). \quad (6)$$

Then, the system equations can be rewritten as

$$\hat{G}_{ii}^k V_i^k + \sum_{j \neq i} \hat{G}_{ij}^k V_j^k = l^2 \frac{\partial I_i^k}{\partial t}. \quad (7)$$

Compared to the system equation based on the inductance matrix  $L^k$  and its inverse  $S^k = (L^k)^{-1}$

$$\begin{aligned} L_{ii}^k \frac{\partial I_i^k}{\partial t} + \sum_{j \neq i} L_{ij}^k \frac{\partial I_j^k}{\partial t} &= V_i^k \\ S_{ii}^k V_i^k + \sum_{j \neq i} S_{ij}^k V_j^k &= \frac{\partial I_i^k}{\partial t}. \end{aligned} \quad (8)$$

The authors find that  $\hat{G}^k$  and  $S^k$  only differ by a geometrical factor  $l^2$

$$\hat{G}^k = l^2 S^k. \quad (9)$$

Therefore, starting with the  $L$  matrix under the PEEC model, the authors first obtain the inverse of  $L$  and then have  $\hat{R}$  under the VPEC model the extraction formula

$$\hat{R}_{ij}^k = -\frac{1}{l^2 S_{ij}^k}, \quad \hat{R}_{i0}^k = \frac{1}{l^2 S_{ii}^k + \sum_{j \neq i} l^2 S_{ij}^k}. \quad (10)$$

Because the major computation effort is the inversion of the  $L$  matrix, the authors call this method as an inversion-based VPEC model, where effective resistances are obtained from a unique relation (10). This inversion-based VPEC model leverages the existing PEEC extractor. In contrast, the localized VPEC model is integration based and needs to explicitly calculate the local flux  $\mathcal{B}_{ij}^k$  ( $j \in n_i$ ) from scratch, where its accuracy is sensitive to the size of the control volume during the integration [15]. Therefore, it has a high accuracy only for a few number of filaments and needs to optimize the size of the control volume for each filament when system has a large number of filaments. Clearly, it becomes impractical for the full-chip extraction.

Note that the above (7)–(10) can be used to derive the  $K$  element (susceptance) based model in [10] and [11] from first principles. Although the  $K$  element method and VPEC are both derived from the inverse of  $L$ , the VPEC model is realized quite differently from the  $K$  element: 1) the VPEC model is SPICE compatible but the  $K$  element needs to introduce the new circuit element to the simulator; and 2) the current  $K$  element simulator is based on nodal analysis [13], where the admittance form of the  $K$  element is  $\Gamma = A_l L^{-1} A_l^T / s$  ( $A_l$  is the incident matrix for the inductance) in the frequency domain. Clearly, the  $\Gamma$  matrix becomes indefinite when  $s \rightarrow 0$ . Therefore, it will lose correct *dc* information. On the other hand, the VPEC model can be stamped in the MNA matrix with the correct *dc* information in both frequency and time-domain simulations [16], which enables the correct circuit reduction [17] to further reduce the model order.

### C. Accuracy Comparisons

In this part, the authors use the aligned parallel bus to compare the PEEC model with the full VPEC model and localized VPEC model.

1) *PEEC Model Extraction*: The experiment setting is illustrated as follows. The authors assume the copper conductor ( $\rho = 1.7 \times$

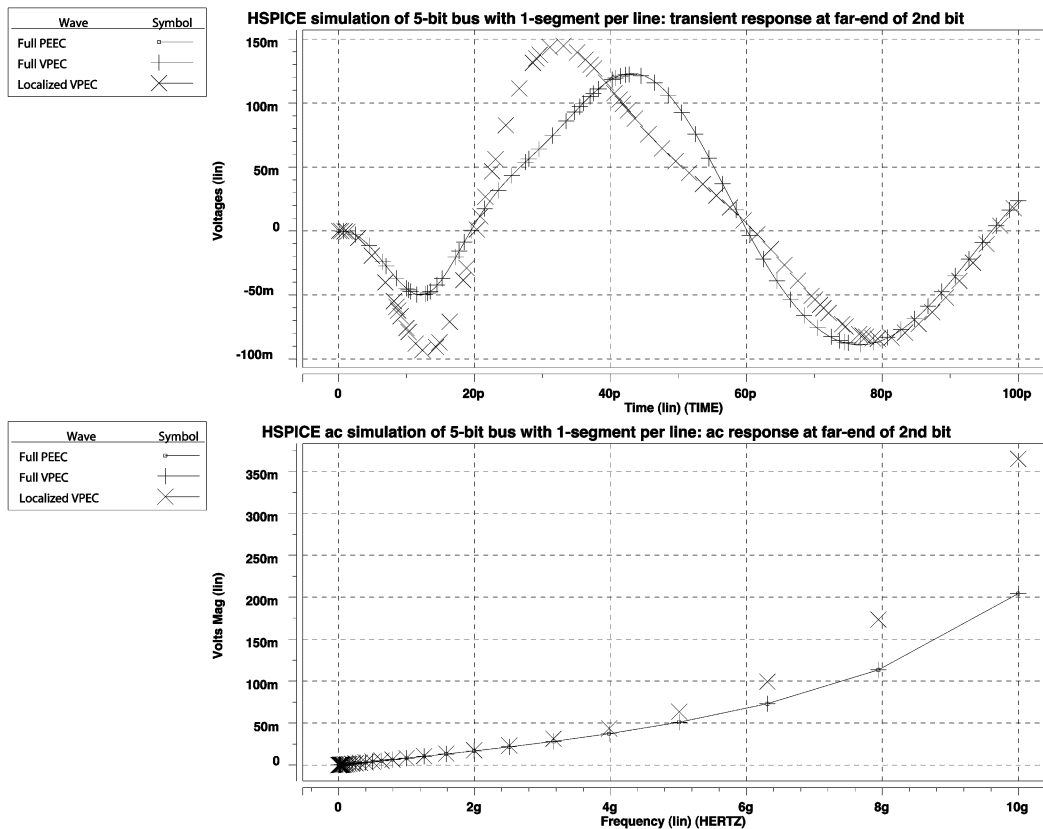


Fig. 2. For a 5-bit bus, (a) a 1-V step voltage with 10 ps of rising time and (b) a 1-V ac voltage are applied to the first bit and all other bits are quiet. The responses of the PEEC model, full VPEC model, and localized VPEC model are measured at the far end of the second bit.

$10^{-8} \Omega \text{ m}$ ) and low- $k$  ( $\epsilon = 2$ ) dielectric. The conductor is volume discretized according to skin depth and longitudinal segmented by one-tenth of the wavelength. Capacitance is extracted by a lookup table [18] interpolated from FastCap [4]. Because capacitive coupling is a short-range effect, only adjacent couplings are considered. Partial inductance is extracted by FastHenry [5] at 10 GHz (as the maximum operating frequency), where each wire segment is modeled by one filament, and coupling between any pair of segments (including segments in a same line) is considered. The authors then generate the distributed  $\pi$  type RLCM circuit under the PEEC model. Furthermore, interconnect drivers and receivers are modeled by the resistance  $R_d = 120 \Omega$  and the loading capacitance  $C_L = 10 \text{ fF}$ . All circuit models are simulated by HSPICE on a SUN Ultra-5 workstation. Note that the same experiment setting is applied for all other experiments in this paper unless specified otherwise.

2) *Simulation of Aligned Parallel Bus:* A 5-bit bus with one segment per line is considered. Each bus line is  $1000 \mu\text{m}$  long,  $1 \mu\text{m}$  wide, and  $1 \mu\text{m}$  thick. The space between lines is  $2 \mu\text{m}$ . With the extracted RLCM parameters under the PEEC model, the authors further construct the full VPEC model (with coupling  $\hat{R}_{ij}$  between all bits) from this paper and the localized VPEC model (with coupling  $\hat{R}_{ij}$  between adjacent bits) from [15]. They measured responses at the far-end of all five bits and compared waveforms of the second bit in Fig. 2(a) and (b) for both time-domain and frequency-domain simulations, where a 1-V step voltage with 10 ps of rising time is used for time-domain transient simulation and a 1-V ac voltage for the frequency-domain (1 Hz to 10 GHz) simulation. Clearly, the full VPEC model and the PEEC model obtain identical waveforms in both frequency- and time-domain simulations, but the localized VPEC model introduces nonnegligible error and is not accurate compared to the PEEC model, where the time-domain response shows 15% waveform difference and the frequency-domain response shows a large deviation beyond 5 GHz.

Note that when the number of conductors is small, there is no simulation speedup observed. However, for larger sized interconnect examples in Sections IV–VI, the simulation time of the full VPEC model (without sparsification) is less than that for the PEEC model. The detailed analysis of complexity scaling can be found in Section VI. Furthermore, in the comparison, the authors did not use the implementation of the localized model from [15], which depends on the height of the integration box (i.e., the size of the controlled volume) and is an approximated solution without a method to find the accurate size of the controlled volume. Instead, the authors find an accurate full VPEC model and then only keep the adjacently coupled resistances to obtain an accurate localized VPEC model.<sup>1</sup>

### III. INDUCTANCE SPARSIFICATION UNDER THE VPEC MODEL

This section first derives the magnetic energy under the VPEC model and then proves that the circuit matrix  $\hat{G}$  under the VPEC model is positive definite. Moreover, the authors prove that  $\hat{G}$  is also strictly diagonal dominant. This property enables the passivity preserved matrix sparsification methods. Finally, the authors present the sparsification flow for the VPEC model.

#### A. Magnetic Energy in VPEC Model

Generally, the magnetic energy is given by the space integral [19]

$$\begin{aligned} u_m &= \frac{1}{2} \int_{\tau} \mathbf{A} \cdot \mathbf{J} d\tau \\ &= \sum_{k=x,y,z} u_m^k. \end{aligned} \quad (11)$$

<sup>1</sup>Based on the communication with [15], the localized VPEC model used in this paper has a similar accuracy compared to the one used in [15].

For the full VPEC model, (11) can be rewritten to

$$\begin{aligned} u_m^k &= \frac{1}{2} \int_{\tau} A^k J^k d\tau \\ &= \frac{1}{2} \sum_i A_i^k I_i^k \\ &= \frac{1}{2} \sum_i A_i^k \hat{I}_i^k. \end{aligned} \quad (12)$$

Furthermore, when the KCL (31) is rewritten in terms of the  $\hat{G}$  matrix

$$\sum_j G_{ij}^k A_i^k = \hat{I}_i^k \quad (13)$$

the authors have for the magnetic energy under the full VPEC model the relation

$$u_m^k = \frac{1}{2} \sum_{i,j} G_{ij}^k A_i^k A_j^k. \quad (14)$$

It is proven below that the  $\hat{G}$  matrix is positive definite.

### B. Property of the $\hat{G}$ Matrix

*Theorem 1:* The circuit matrix  $\hat{G}^k$  ( $k = x, y, z$ ) in the VPEC model is positive definite.

Because  $\hat{G}$  only differs from the  $K$  matrix by a positive geometric constant, the proof of the matrix property (passivity and strict diagonal dominance) for  $K$  is equivalent for  $\hat{G}$ . The existing proofs in [10] and [13] are based on the analogy  $[L] = \mu\epsilon[C^{-1}]$ , which holds when  $[C][L] = \text{constant}$ . However, this relation does not hold in general as shown in [20]. Below, the authors present a direct proof for the VPEC model.

*Proof:* According to (14), because the energy  $u_m^k$  ( $k = x, y, z$ ) is positive, it automatically results in a positive definite matrix  $\hat{G}^k$  [21].

Therefore, the corresponding VPEC model is passive. However, to further guarantee a passive model after truncating small-valued off-diagonal elements from the original positive definite matrix, the authors will prove that the matrix  $\hat{G}$  is strictly diagonal dominant [21], i.e.,  $\hat{G}_{ii}^k > \sum_j |\hat{G}_{ij}^k|$ . ■

*Lemma 1:* All the effective resistances  $\hat{R}_{i0}^k$  and  $\hat{R}_{ij}^k$  ( $k = x, y, z$ ) in the VPEC model are positive.

*Proof:* The authors present the proof based on the KCL (1). Since effective resistances are only determined by the geometry of the filaments, it will not depend on the applied external sources. Without loss of generality, the authors assume that an impulse current  $I_i^k$  is applied at filament  $a_i$  along the  $z$  direction and all other filaments  $a_j$  are connected to the vector potential ground. Note that for the filament  $a_i$ , its average vector potential  $A_i^k$  is in the same direction of  $I_i^k$ ; for any other grounded filament  $a_j$ , its average vector potential  $A_j^k$  is zero, but its induced current  $-I_j^k$  is in the opposite direction to  $I_i^k$  according to Lenz's law. Hence, for filament  $a_j$ , (31) becomes

$$\frac{(A_j^k - A_i^k)}{\hat{R}_{ij}^k} = \frac{-A_i^k}{\hat{R}_{ij}^k} = -II_j^k$$

where the induced current  $I_j^k$  is determined by the coupling flux between  $a_i$  and  $a_j$ . Equation (1) can be further rewritten to

$$\hat{R}_{ij}^k = \frac{A_i^k}{II_j^k} > 0. \quad (15)$$

The positiveness of the ground resistance  $\hat{R}_{i0}^k$  can be easily proved in a similar fashion. With this lemma, the authors can further prove the following theorem. ■

*Theorem 2:* The circuit matrix  $\hat{G}^k$  ( $k = x, y, z$ ) in the VPEC model is strictly diagonal dominant.

*Proof:* According to (6)

$$\sum_{j \neq i} |\hat{G}_{ij}^k| = \sum_{j \neq i} \frac{1}{\hat{R}_{ij}^k} \quad (16)$$

and

$$\sum_{j \neq i} |\hat{G}_{ij}^k| < \frac{1}{\hat{R}_{i0}^k} + \sum_{j \neq i} \frac{1}{\hat{R}_{ij}^k} = \hat{G}_{ii}^k$$

or

$$\hat{G}_{ii}^k > \sum_{j \neq i} |\hat{G}_{ij}^k|. \quad (17)$$

That is, the circuit matrix  $\hat{G}$  is strictly diagonal dominant. Note that truncating small off-diagonal entries from a strictly diagonal dominant matrix still leads to a positive definite matrix, i.e., a passive circuit model [21]. Based on Theorem 2, such a truncation-based sparsification still leads to passive circuit models. Intuitively, truncating small off-diagonal entries in the  $\hat{G}$  matrix (equivalent to truncating larger off-diagonal entries in  $\hat{R}$  matrix) results in ignoring larger resistors in the equivalent resistance network. Because larger resistors are less sensitive to and also contribute less to current change, the resulting sparsified model can still have a good waveform accuracy as presented in Section IV. Moreover, the proof assumes that wires can be decomposed into short wires with similar length. Therefore, in the experiments, the authors always segment wires to one-tenth of the maximum operating frequency when wire lengths are different (see spiral inductor in Section V). ■

### C. VPEC-Based Inductance Sparsification

With Theorem 2, the authors present the flow below for the inductance sparsification based on the VPEC model.

- Generate the partial inductance matrix  $L$  by FastHenry or the formula from [22] and [23].
- (Option 1: tVPEC model) Invert the full  $L$  matrix to obtain matrix  $\hat{G}$ ,  $\hat{R}$ , and full VPEC model, and then generate the sparsified VPEC model by truncating the full VPEC model.
- (Option 2: wVPEC model) Find a sparse approximated inverse matrix  $S'$  of  $L$  to obtain  $\hat{G}'$ ,  $\hat{R}'$ , and the sparsified VPEC model simultaneously.

Note that during the inductance extraction at low frequency, the authors assume that each wire segment is modeled by one filament. When the frequency is beyond 10 GHz, the volume filament [5] or conduction mode [24] based decomposition can be applied to consider the skin and proximity effects. In this paper, the authors use the three-dimensional (3-D) frequency-dependent solver FastHenry [5] to accurately extract the partial inductance matrix. Because inductance has weak dependence on geometry, the formula-based [23] or lookup table-based [25] approaches can also be applied to efficiently obtain the full-chip inductance.

As further discussed in Sections VI and V, the authors will apply two sparsifications that depend on the scale of the interconnect: 1) when the scale of interconnect is small (less than 1000 wires), the direct LU or Cholesky factorization-based inversion is sufficiently efficient

TABLE II  
SETTINGS AND RESULTS OF GEOMETRICAL tVPEC MODELS

Models and Window Sizings	No. of Elements	Run Time (second)	Average Voltage Difference (volt)	Standard Deviation (volt)
Full PEEC	32 896	2535.48 (1×)	0	0
Full VPEC(32,8)	32 896	772.89 (3×)	1.00e-5	6.26e-4
gtVPEC(32,2)	11 392	311.22 (8×)	5.97e-5	1.84e-3
gtVPEC(16,2)	3488	152.57 (16×)	-1.23e-4	4.56e-3
gtVPEC(8,2)	2240	85.14 (32×)	-2.17e-4	8.91e-3

$[O(N^3)]$ , and the authors can apply simple truncation-based sparsifications; 2) when the scale of interconnect is large, the authors extend a window-based extraction [11] to obtain a sparse approximated inverse of  $L$  and simultaneously extract a sparsified VPEC model. It reduces the computation expense to  $O(Nb^3)$ , where  $b$  is the size of the window. As shown by experiments, the wVPEC model also reduces the error introduced by the sparsification when compared to the tVPEC model.

#### IV. tVPEC MODEL

This section presents the tVPEC model. After the full inversion of  $L$ , the authors obtain a strictly diagonal dominant matrix  $\hat{G}$ . As explained in Section III, its small-valued off-diagonal elements can be truncated without loss of passivity. The authors present two truncating approaches below: the geometrical VPEC (gtVPEC) and numerical VPEC (ntVPEC) truncations. The first one is applicable to the aligned parallel bus, and the second is applicable to conductors of any shapes.

##### A. Geometrical Truncation

For the aligned parallel bus, the authors can define a truncating window  $(N_W, N_L)$  for each wire segment, where  $N_W$  and  $N_L$  are the numbers of coupled segments in the directions of wire width and length, respectively. The coupling along the wire length is the forward coupling, and the one along the wire width is the aligned coupling. Because of the symmetry introduced by aligning and paralleling, each wire segment will have the same sized truncating window. As a result, the tVPEC model only contains  $\hat{R}_{ij}$  within the truncating window for each wire segment and is called gtVPEC in Table II.

The authors consider a 32-bit bus with eight segments per line and four differently sized truncating windows, (32, 8), (32, 2), (16, 2), and (8, 2), and summarize the experiment setting and result in Table II. Clearly, there is a smooth tradeoff between runtime and accuracy for different truncating window sizes, where the average voltage differences and associated standard deviations are calculated for all time steps in SPICE simulation. The authors first compare results of different truncating windows. The truncating window (8, 2) achieves the highest speedup of 30× and the largest difference of about 0.2 mV on average, less than 2% of the noise peak, and the truncating window (32, 2) has the highest accuracy with 0.06 mV on average but a reduced speedup of 10×. Furthermore, the small difference between windows (32, 8) and (32, 2) implies that the forward couplings between nonadjacent segments are negligible. However, an  $N_W$  larger than  $N_L$  (as shown in Table II) is needed to achieve a high accuracy. This implies that the aligned coupling is stronger than the forward coupling and considering only the adjacent aligned coupling may lead to a large error.

##### B. Numerical Truncation

For numerical truncation, the authors define the coupling strength as the ratio of an off-diagonal element to its correspondent diagonal element at each row of  $\hat{G}$ . They then truncate those off-diagonal elements with coupling strength smaller than a specified threshold.

Fig. 3 plots simulation results under the numerical sparsification for the nonaligned parallel bus with 128 bits and one segment per line. The

sparse factor is the ratio between the numbers of circuit elements in the truncated and full VPEC models. The waveform difference is small in terms of the noise peak for sparse factors up to 30.5%. Table III summarizes the truncation setting and simulation result, where values in parentheses of column 1 are truncating thresholds, and the runtime includes both SPICE simulation and matrix inversion in case of VPEC models. One can see from the table that up to 30× speedup is achieved when the average waveform differences is up to 0.377 mV, less than 1% of the noise peak. A larger speedup factor can be expected as a higher waveform difference can be tolerated in practice. The authors also compare the full VPEC model and the PEEC model. The full VPEC simulation is 7 times faster and has a negligible waveform difference.

#### V. wVPEC MODEL

The sparsification in Section IV needs full matrix inversion and becomes computationally expensive for the large-sized interconnect. Furthermore, the directly truncated matrix  $\hat{G}$  may be not accurate enough to represent the original full  $\hat{G}$  matrix. As shown in [11], all entries of the  $L$  inverse matrix can be approximately reconstructed from entries of the submatrices in  $L$  corresponding to the coupling window of the active aggressor. Using this windowing technique, the authors further present two wVPEC models based on the geometry (gwVPEC) and numerical value (nwVPEC), respectively.

##### A. Geometrical Windowing

Owing to the regularity of the aligned parallel bus, a coupling window with uniform size  $b$  for each wire can also be defined. For each wire in turn as the aggressor, the authors first construct  $N$  small submatrices (coupling windows) all with size  $b$ , then invert each submatrix and build a sparse approximated inverse for  $L$ . It is described in details in the following two steps.

1) *Submatrix Construction*: For aggressor  $m$  and all its victims within a window of size  $b$ , the authors construct a submatrix  $L^{(m)}$  as

$$L_{ij}^{(m)} = \begin{cases} L_{ij}, & \text{if } (i, j) \text{ inside the window} \\ 0, & \text{if } (i, j) \text{ outside the window.} \end{cases}$$

The authors then solve vector  $\mathbf{s}^{(m)}$  from  $L^{(m)}\mathbf{s}^{(m)} = \mathbf{i}^{(m)}$ , where  $\mathbf{i}^{(m)}$  is the unit vector, correspondent to applying a unit current source at the  $m$ th aggressor, i.e.,  $\mathbf{i}_n^{(m)} = \delta_{mn}$ . With further iterating the above procedure for all conductors in turn as the active aggressor, the authors obtain  $N$  dimension-reduced vectors  $\mathbf{s}^{(m)}$ . Because this process is only related to the submatrix, the complexity of full inversion is reduced from  $O(N^3)$  to  $O(Nb^3)$  when  $b$  is small.

2) *Heuristic Selection*: The authors then merge all  $\mathbf{s}^{(m)}$  vectors into one complete and sparse matrix  $S'$  that can approximate  $L^{-1}$ , the inverse of inductance matrix. The entry of  $S'$  is

$$S'_{mn} = S'_{nm} = \max\left(\mathbf{s}_n^{(m)}, \mathbf{s}_m^{(n)}\right) \quad (18)$$

where  $\mathbf{s}_n^{(m)}$  is the element between the  $m$ th aggressor and its  $n$ th victim inside the coupling window. Note that  $\mathbf{s}_n^{(m)}$  is always negative with sufficient discretizations [13]. The circuit matrix of a stable system needs

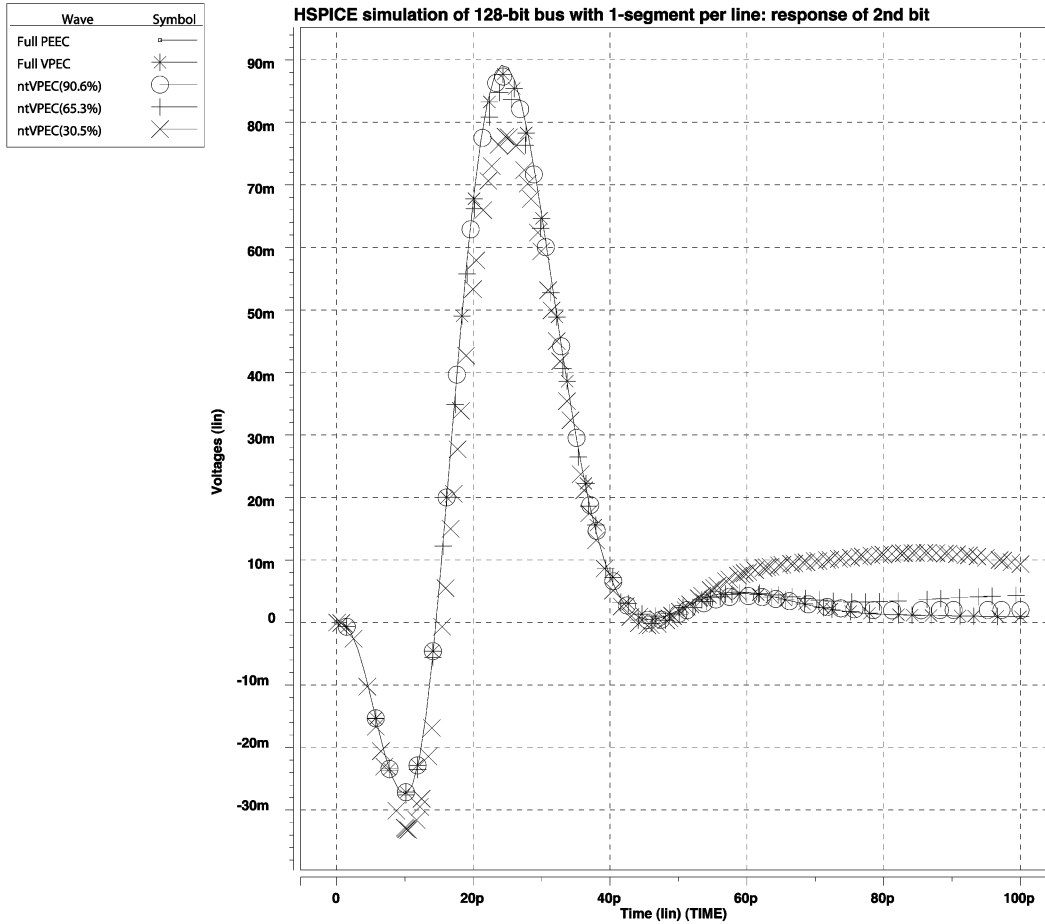


Fig. 3. For a 128-bit bus by numerical truncation, a 1-V step voltage with 10 ps of rising time is applied to the first bit and all other bits are quiet. The responses of the PEEC model, the full VPEC model, and the tVPEC model are measured at the far end of the second bit.

TABLE III  
SETTINGS AND RESULTS OF NUMERICAL tVPEC MODELS

Models and Truncation Thresholds	No. of Elements	Run Time (second) and Speedup	Average Voltage Difference (volt)	Standard Deviation (volt)
Full PEEC	8256	281.02 (1x)	0	0
Full VPEC(0.0)	8256	36.40 (7x)	-1.64e-6	3.41e-4
ntVPEC(5e-5)	7482	30.89 (9x)	4.64e-6	4.97e-4
ntVPEC(1e-4)	5392	19.55 (14x)	1.29e-5	1.37e-3
ntVPEC(5e-4)	2517	8.35 (28x)	3.77e-4	5.20e-3

to be symmetric positive definite (s.p.d.). This is guaranteed by the heuristic in (18). That is, the authors always have

$$S'_{mm} \geq \sum_{n \neq m} |S'_{mn}|. \quad (19)$$

As a result, the authors can construct the sparsified yet passive VPEC model based on (10) with the sparse approximated inverse  $S'$ .

The authors first compare the extraction efficiency of geometrical tVPEC and wVPEC models in Fig. 4 by extracting the VPEC model for buses up to 2000 bits. The size for geometrical truncation is  $(N_W, N_L) = (8, 1)$  and for the geometrical wVPEC is  $b = 8$ . The extraction time for a truncation-based method includes the full inversion and truncation. When the scale of interconnects is small (below 128 bits), the truncation-based method is actually as efficient as the window-based method. But when the scale of interconnects becomes larger, the window-based extraction is faster than the truncation-based approach with a 90x speedup for the 2048-bit bus (8.6 s versus 543.1

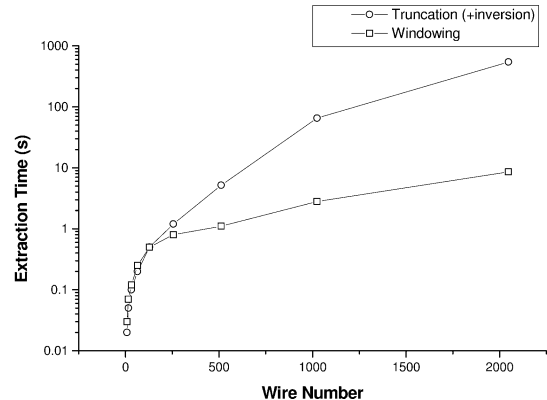


Fig. 4. Extraction time comparisons of bus lines with one segment each line using geometrical tVPEC and wVPEC models.

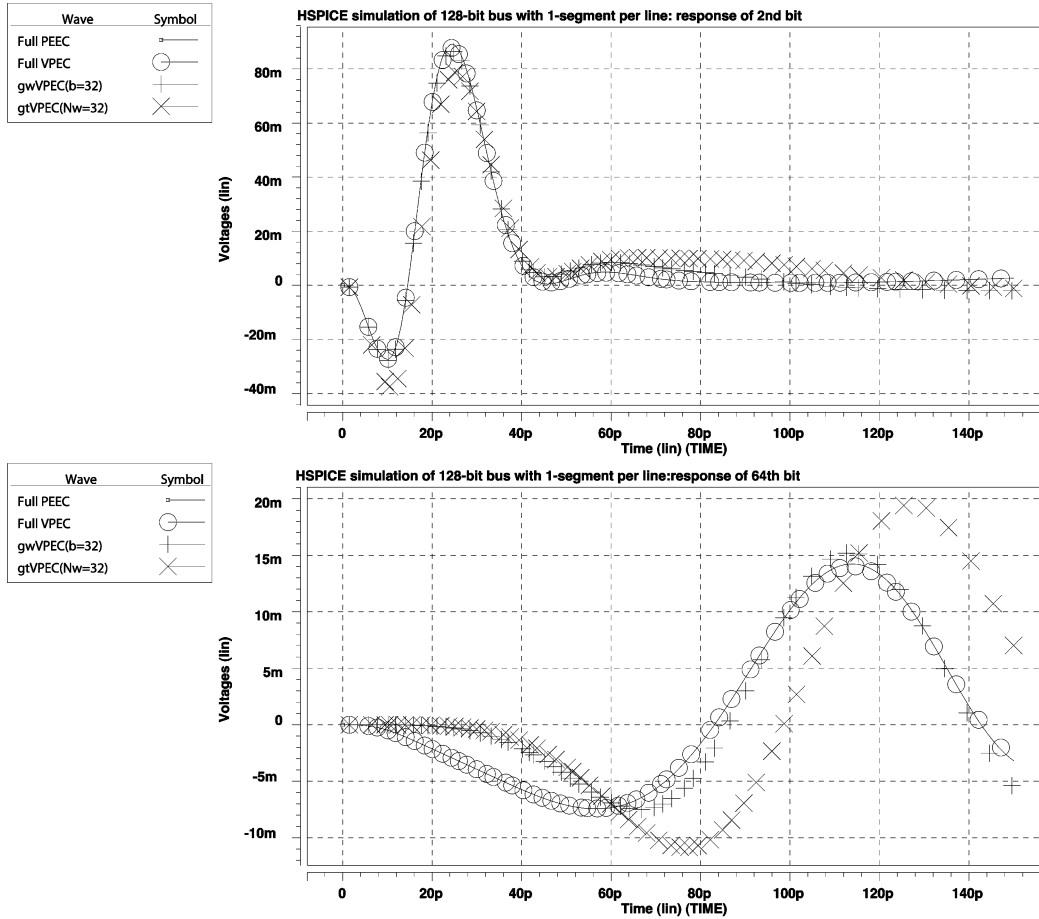


Fig. 5. For a 128-bit bus by geometrical windowing, a 1-V step voltage with 10 ps of rising time is applied to the first bit and all other bits are quiet. The responses of the PEEC model, full VPEC model, gtVPEC model, and gwVPEC model are measured at the far end of the second and 64th bits, respectively.

TABLE IV  
WAVEFORM ACCURACY COMPARISONS OF gtVPEC AND gwVPEC MODELS

Waveform Difference (volt)	b = 64	b = 32	b = 16	b = 8
gtVPEC(Avg. $\pm$ STD)	$-3.47e-4 \pm 2.74e-3$	$-5.19e-4 \pm 4.85e-3$	$-6.32e-4 \pm 6.72e-3$	$-1.57e-3 \pm 1.06e-2$
gwVPEC(Avg. $\pm$ STD)	$-3.28e-4 \pm 1.27e-3$	$-5.02e-4 \pm 2.31e-3$	$-5.28e-4 \pm 3.29e-3$	$-1.12e-3 \pm 5.13e-3$

s). Therefore, it is more efficient to apply the winnowed VPEC model for large-scale interconnects.

The authors further compare the waveforms between gtVPEC and ntVPEC models for the 128-bit bus with one segment per line. The authors apply a pulse voltage at the first bit and observe the transient responses at the far ends of second and 64th bit bus, respectively. The window size is  $b = 32$  for the gwVPEC model and  $(N_W, N_L) = (32, 1)$  is set for the gtVPEC model to achieve the same sparsification ratio. Fig. 5 shows waveforms of the PEEC model, full VPEC model, gtVPEC model, and gwVPEC model. Compared to accurate models such as the PEEC model and full VPEC model, the gwVPEC and gtVPEC models have virtually no error at the second bit bus. But for the 64th bit, the gtVPEC model has nonnegligible error but the gwVPEC model still has a high accuracy. More accuracy comparisons are presented in Table IV by changing the window size  $b$  to 64, 32, 16, and 8, where the waveform difference is calculated from responses at far ends of the 64th bit between the sparsified VPEC and PEEC models. The authors find that the window-based extraction has  $2\times$  higher accuracy than the truncation-based approach on average. It is due to the fact that the matrix element generated from windowing is interpolated with other elements in the inductance matrix.

### B. Numerical Windowing

The coupling window usually has different sizes for different wires because the general layout does not have the regularity as the aligned parallel bus. Therefore, the authors first need to determine the size of coupling window for each wire. Similar to the numerical truncation approach, the authors define the coupling strength as the ratio of an off-diagonal element to its correspondent diagonal element at each row of the  $L$  matrix. The authors then construct the coupling window by only considering those off-diagonal elements that have coupling strength larger than a specified threshold value. With the heuristic selection (18), the authors can build the sparse approximated inverse and consequently a sparsified VPEC model.

In an example shown in Fig. 6, the authors extract the partial inductance by FastHenry at 10 GHz for a three-turn spiral inductor on the lossy substrate. The heavily doped substrate modeled as lossy ground plane with  $\rho = 1.0 \times 10^{-5} \Omega\text{m}$ . The metal is volume discretized according to skin depth and longitudinal segmented by one-tenth of the wavelength, resulting in 92 segments. The substrate is also discretized according to [26], and its contribution (Eddy current loss) is lumped to the segmented conductor on top of the substrate.



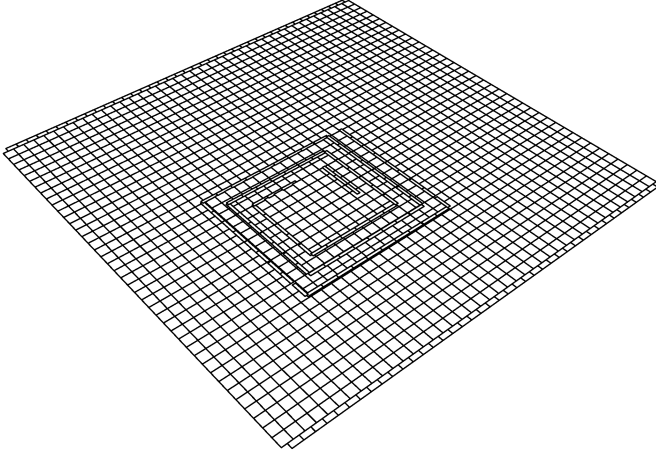


Fig. 6. Discretized spiral inductor on the lossy substrate for the generation of the distributed RLCM PEEC/VPEC model.

The authors construct the distributed RLCM PEEC model with 5120 circuit elements and then apply the numerical window-based method by setting the threshold as  $1.5e-4$ . It results in a 56.7% sparsification ratio. To check the accuracy of the resulting model, the authors apply a 1-V pulse voltage at input and observe the response at the output port. Fig. 7 shows the waveforms obtained by the PEEC model, full VPEC model, and nwVPEC model. The three waveforms are virtually identical to each other but the wVPEC model results in an  $8\times$  runtime speedup compared to the full PEEC model (9.3 s versus 70.5 s).

## VI. COMPLEXITY SCALING OF VPEC MODELS

The authors further compare runtimes and model size by extracting and simulating a number of aligned parallel buses using the PEEC model, full VPEC model, and gwVPEC model ( $b = 8$ ), respectively. The runtime for the full or wVPEC model includes both VPEC extraction and SPICE simulation times. The model size refers to the file size of the resulting SPICE netlists. The authors plot the runtime versus the bus size in Fig. 8(a) and the model size versus the bus size in Fig. 8(b).

Due to the additional introduced circuit elements, the size of SPICE netlist for the full VPEC model is around 10% larger than the full PEEC model on average. Further, when the scale of wire number is small, there is no runtime speedup observed for the full VPEC model. However, when the scale of wire becomes larger (greater than 64 bits), the runtime of the full VPEC model is found to be 10 times faster than the PEEC model on average. For the 256-bit bus, the full VPEC model is  $47\times$  (185.39 s versus 8726.85 s) faster than the PEEC model. This is due to the fact that: 1) its resultant network has fewer reactive elements (i.e. inductances); and 2) its resultant MNA matrix in SPICE is sparser than the direct inductance formulation. SPICE converges faster with fewer time derivatives and integrals, and its internal sparse solver is more efficient for a less dense matrix.

Moreover, both PEEC and full VPEC models can only handle a bus circuit with up to 256 bits due to memory limitations. On the other hand, the gwVPEC model ( $b = 8$ ) can handle a larger size of up to thousand bits. Moreover, it is easy to see that the scalability of the gwVPEC models shows a slow increase with respect to the increase of the bus line numbers. For example, it achieves over  $1000\times$  (9.71 s versus 8726.85 s) speedup for a 256-bit bus in runtime compared to the PEEC model. In all the simulation, the wVPEC model has a very small waveform difference (less than 3%) in terms of delay when compared to the PEEC model.

## VII. CONCLUSION

Using the equivalent resistance network and controlled voltage and current sources to replace the inductance network, the authors develop the full VPEC model that is as accurate as the PEEC model but takes less simulation time. Although the full VPEC model has a slightly higher circuit complexity compared to the PEEC model, SPICE can handle the VPEC model more efficiently because the VPEC model has fewer reactive elements (i.e., inductances) and the modified nodal admittance matrix becomes sparser under VPEC model than that under the PEEC model.

Moreover, the resulting circuit matrix  $\hat{G}$  for the equivalent resistance network in the full VPEC model is passive and strictly diagonal dominant. This enables truncation-based sparsification methods with guaranteed passivity. The authors have presented the truncation-based method and have achieved orders of magnitude speedup in circuit simulation with small errors compared to the PEEC model. Furthermore, the window-based extraction method has been developed to avoid the full inductance matrix inversion and can obtain a higher accuracy compared to the truncation-based approach. The authors have also shown that the matrix  $\hat{G}$  can be used to justify the  $K$  element or susceptance-based simulation [10]–[14] from first principles. Note that SPICE is able to directly simulate the VPEC model but not the  $K$  element-based model.

The primary contribution of this paper is to derive the inversion-based full VPEC model for multiple inductive interconnects and illustrate how to build sparsified VPEC for SPICE simulation with guaranteed passivity. To further reduce the complexity of the resulting sparsified VPEC models, the authors intend to develop model order reduction for the VPEC model.

## APPENDIX

To model the inductive effect, the authors start with differential Maxwell equations in terms of  $\mathbf{A}$  [19]

$$\nabla^2 A^k = -\mu J^k \quad (20)$$

$$\frac{\partial A^k}{\partial t} = -E^k \quad (21)$$

where the vector potential  $\mathbf{A}$  is in the  $z$  direction same as the current density  $\mathbf{J}$ ,  $\mathbf{E}$  is the electrical field, and  $\mu$  is the permeability constant. Note that the resistive voltage drop by  $(-\nabla^k \phi)$  is not included in (21) since the authors are interested in the inductive voltage drop here. Given the distribution of the current density  $J^k$ , the vector potential  $A^k$  is determined by

$$A^k = \frac{\mu}{4\pi} \int \frac{J^k}{|\mathbf{r} - \mathbf{r}'_i|} d\tau(\mathbf{r}'_i). \quad (22)$$

To construct the system equation in the form of the integral equation, the authors apply the volume and line integration to (20) and (21), respectively. For filament  $a_i$ , when (20) is integrated within the volume  $\tau_i$  of filament  $a_i$ , using Gauss' law

$$\int_S \mathbf{a} \cdot d\mathbf{S} = \int_\tau \nabla \cdot \mathbf{a} d\tau \quad (23)$$

the authors can obtain

$$\begin{aligned} -\mu \int_{\tau_i} J^k d\tau &= \int_{S_i} \nabla A^k \cdot d\mathbf{S} \\ &= \mathcal{B}_{i0}^k + \sum_{j \neq i} \mathcal{B}_{ij}^k. \end{aligned} \quad (24)$$

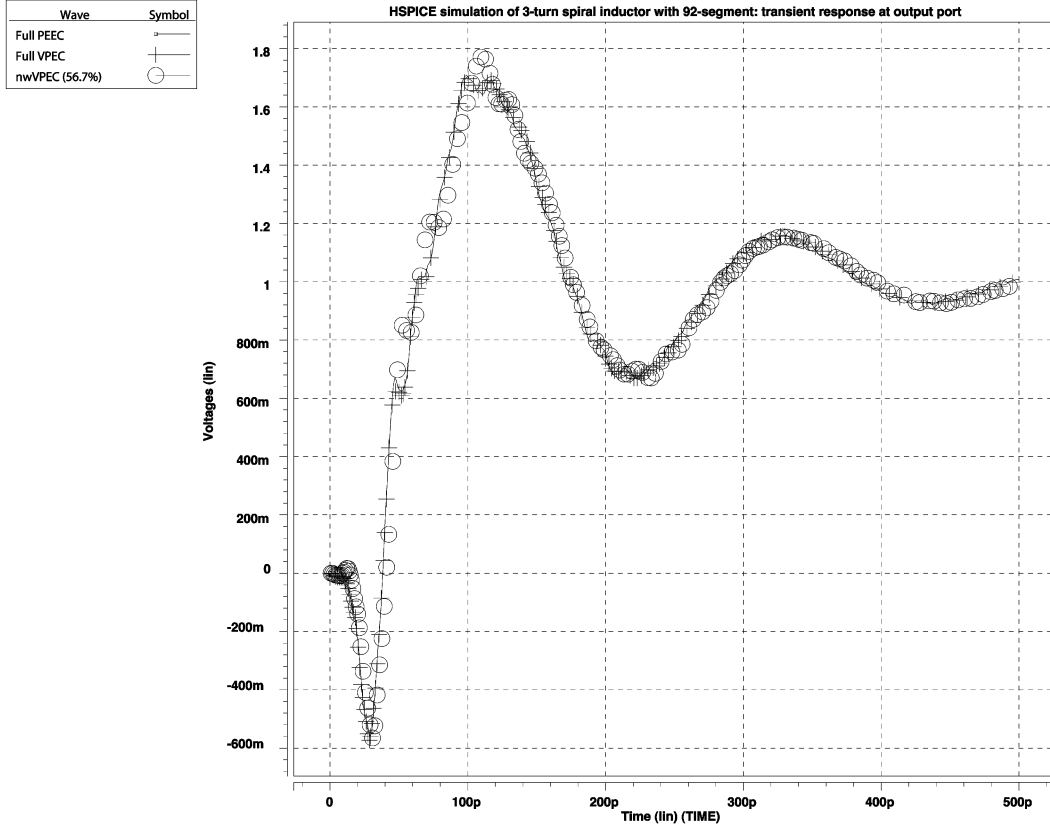


Fig. 7. For a three-turn spiral inductor with 92 segments by the numerical windowing, a 1-V step voltage with 10 ps of rising time is applied to the input port. The responses of the PEEC model, full VPEC model, and nwVPEC model are measured at the output port.

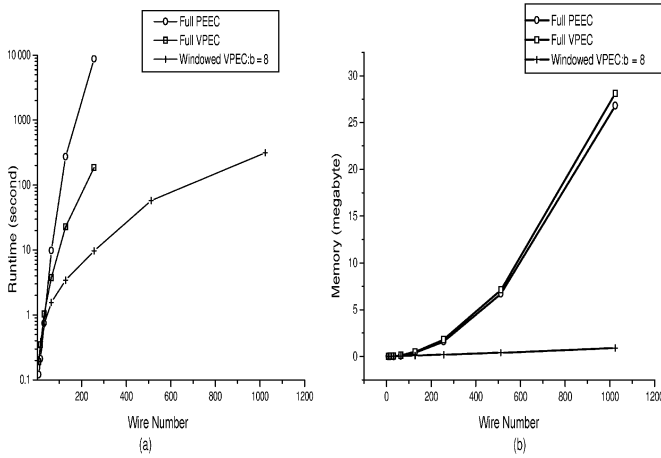


Fig. 8. Runtime and memory usage comparisons of bus lines with one segment each line using the PEEC model, full VPEC model, and gwVPEC model ( $b = 8$ ).

Note that the surface integral  $\int_{S_i} dS \nabla A^k$  is actually the flux of the gradient of  $k$ th component of the vector potential caused by the filament current of  $a_i$  in  $\tau_i$ . It consists of following parts [15]: 1) the flux to the infinity (vector potential ground)  $\mathcal{B}_{i0}^k$

$$\mathcal{B}_{i0}^k = \int_{S_{i0}} \nabla A^k \cdot d\mathbf{S} \quad (25)$$

and 2) the flux to all other filaments  $a_j$  ( $j \in N, j \neq i$ )  $\mathcal{B}_{ij}^k$

$$\mathcal{B}_{ij}^k = \int_{S_{ij}} \nabla A^k \cdot d\mathbf{S}. \quad (26)$$

However, to explicitly determine the value of  $\mathcal{B}_{ij}^k$  is difficult because it is hard to partition the flux between filament  $a_i$ , all other filaments  $a_j$ , and the vector potential ground.

Moreover, integrating (21) along the projected length in the  $k$  direction of filament  $a_i$  leads to

$$\int_{l_i} \frac{\partial A^k}{\partial t} dl = - \int_{l_i} E^k \cdot dl. \quad (27)$$

Based on (24) and (27), the authors can further construct the circuit-level system equation in matrix form. By defining the filament vector potential [15] as the average volume integral of  $A^k$  within  $\tau_i$  (surrounded by the surface  $S_i$ )

$$A_i^k = \frac{1}{\tau_i} \int_{\tau_i} A^k(\mathbf{r}) d\tau(\mathbf{r}). \quad (28)$$

The authors can define an effective coupling resistance

$$\hat{R}_{ij}^k = -\mu \frac{(A_i^k - A_j^k)}{\mathcal{B}_{ij}^k} \quad (29)$$

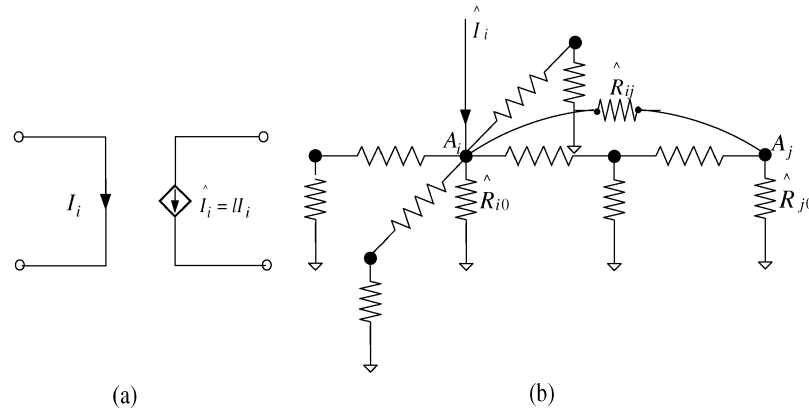


Fig. 9. (a) Electronic current-controlled vector potential current source. (b) Kirchhoff's current law for the vector potential circuit. An invoking vector potential current source is employed at  $a_i$  and the responding vector potential at  $a_j$   $A_j^k$  determined by the full effective resistance network.

to model (i.e., replace) the mutual inductive coupling between  $a_i$  and  $a_j$ . In addition, there also exists an effective ground resistance to model the self-inductive effect

$$\hat{R}_{i0}^k = -\mu \frac{A_i^k}{B_{i0}^k}. \quad (30)$$

Because the filament current is invariant along the  $k$  direction, the volume integral of the current density inside the volume  $\tau_i$  is reduced to  $II_i^k$ , where  $I_i^k$  is the electrical current at the cross section of  $a_i$ . Therefore, (24) becomes the KCL under the full VPEC model

$$\frac{A_i^k}{\hat{R}_{i0}^k} + \sum_{j \neq i} \frac{(A_i^k - A_j^k)}{\hat{R}_{ij}^k} = II_i^k \quad (31)$$

where a vector potential current source  $\hat{I}_i^k$  can be defined as

$$\hat{I}_i^k = II_i^k \quad (32)$$

that is controlled by the electrical current  $I_i^k$ . An equivalent circuit to illustrate the VPEC KCL (31) is shown in Fig. 9. Clearly, we can see the physical meaning of the effective resistance: given a unit current change at the  $i$ th filament, the vector potential observed at the  $j$ th filament is exactly  $\hat{R}_{ij}^k$  when all other filaments are connected to the vector potential ground.

Similar for (27), the authors have the inductive nodal voltage equation

$$l \frac{\partial A_i^k}{\partial t} = V_i^k \quad (33)$$

that describes the relation between the vector potential and its corresponding electrical voltage drop caused by the inductive effect. As a result, a voltage-controlled vector potential voltage source  $\hat{V}_i^k$  is

$$\hat{V}_i^k = \frac{V_i^k}{l}. \quad (34)$$

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## Sequential Circuit ATPG Using Combinational Algorithms

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**Abstract**—In this paper, we introduce two design-for-testability (DFT) techniques based on clock partitioning and clock freezing to ease the test generation process for sequential circuits. In the first DFT technique, a circuit is mapped into overlapping pipelines by selectively freezing different sets of registers so that all feedback loops are temporarily cut. An opportunistic algorithm takes advantage of the pipeline structures and detects most faults using combinational techniques. This technique is feasible to circuits with no or only a few self-loops.

In the second DFT technique, we use selective clock freezing to temporarily cut only the global feedback loops. The resulting circuit, called a *loopy pipe*, may have any number of self-loops. We present a new clocking technique that generates *clock waves* to test the loopy pipe. Another opportunistic algorithm is proposed for test generation for the loopy pipe. Experimental results show that the fault coverage obtained is significantly higher and test generation time is one order of magnitude shorter for many circuits compared to conventional sequential circuit test generators. The DFT techniques do not introduce any delay penalty into the data path, have small area overhead, allow for at-speed application of tests, and have low power consumption.

**Index Terms**—Automatic test pattern generation, clock freezing, clock partitioning, clock waves, design for testability, power consumption, sequential circuit test generation.

### I. INTRODUCTION

Automatic test-pattern generation (ATPG) for sequential circuits has long been recognized as a difficult and time-consuming problem [1]–[3], so that ATPG algorithms working on complex circuits can spend many hours of CPU time and still obtain poor results in terms

of fault coverage. Among the factors contributing to the complexity of this problem [3] are: 1) the difficulty in controlling and observing deeply buried flip-flops (FFs); 2) the need to work with a model consisting of an iterative array of time-frames whose number is, in the worst case, an exponential function ( $4^n$ ) of the number of FFs in the circuit ( $n$ ); 3) the existence of illegal states, which may cause the ATPG algorithm to waste a lot of time trying to justify them; and 4) the existence of untestable faults, which require the ATPG algorithm to complete an exhaustive search before they are identified as untestable.

Several different approaches have been proposed for sequential circuit test generation, including deterministic techniques, genetic techniques, symbolic techniques, and various combinations of the three [4]–[15]. Deterministic algorithms tend to be highly complex and time consuming [4]–[6]. As an example, the HITEC test generator [6] uses both forward and reverse time processing to generate a test for a target fault. During test generation, each target fault must be excited and the fault effects propagated to a primary output (PO), either in the same time-frame in which the fault is excited or in a subsequent time-frame. The required state must then be justified. If conflicts are found, backtracking is required, and alternative decisions must be made. Genetic algorithm (GA) based approaches simplify test generation by processing in the forward direction only [8]–[12]. Populations of candidate test sequences are evolved over several generations, with more highly fit sequences propagating from one generation to the next. Fitness is determined based on fault detection capabilities, amount of circuit activity induced, and other factors related to detecting the target faults. GA-based techniques have been especially effective for data-dominant circuits. Symbolic techniques [7], [14] based on binary decision diagrams (BDDs) have also been used very effectively on control-dominant circuits. Very high fault coverages have been achieved, although the size of the circuit that can be handled is limited.

Various design-for-testability (DFT) techniques have also been proposed to ease the test generation process and improve the fault coverage for sequential circuits, including full scan design [16], [17], partial scan design [18]–[21], clock control [22], [23], and probe point insertion [24], [25]. With full scan design, all flip-flops are arranged in a chain when a circuit is being tested, and node values at the flip-flops are scanned in before each test and scanned out after each test. Complete controllability and observability are thus provided at the flip-flops, reducing the complexity of the test generation process to that for a combinational circuit. In partial scan design, only a subset of flip-flops are placed in the scan chain. Partial scan design is a cost effective alternative; delay and area penalties are reduced, and test application time may be reduced as well. However, the remaining circuit is still sequential, so a sequential circuit test generator is needed. With clock control, flip-flops in a circuit are divided into groups, and each group is controlled by a single clock signal, thus reducing the correlation between flip-flops and increasing the number of reachable states. By using probe points, the observability of some internal lines, including the outputs of flip-flops and any other lines, can be enhanced.

In this paper, we propose two DFT techniques based on clock partitioning and clock freezing, *selective clock freezing* and *CLOCK-WAVE*, to ease the test generation process for sequential circuits and two opportunistic ATPG algorithms that take advantage of the DFT techniques and detect most faults using combinational techniques [26], [27]. With the selective clock freezing DFT technique, a circuit is mapped into various overlapping pipeline configurations by selectively freezing different sets of registers. An opportunistic algorithm, called *PIPEXPRESS*, is then used for test generation on different pipeline

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