EE 201A

Fundamentals to Computer-Aided Design of VLSI Circuits and Systems

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Instructor Info

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  - or email for appointments

- The best way to reach me:
  - Email with EE201 in subject line

Course Prerequisites

- Official prerequisite
  - EE116B VLSI System Design
  - But mainly self-contained
- Knowledge to help you appreciate more
  - CS 180, Introduction to algorithms
  - EE 136, Introduction to engineering optimization techniques

EE201A Outline and Schedule

- Circuit platforms and models (2 weeks)
  - ASIC, FPGA, and uProcessor platforms
  - Timing, power and thermal modeling
- Basics of logic and physical design algorithms (2 weeks)
  - RTL synthesis and technology mapping
  - Partitioning, placement and routing for ASIC and FPGA
- Applications of FPGA (3 weeks)
  - RTL-based design for FPGA
  - Dynamic configuration of FPGA
  - Reliability and security of FPGA
- More synthesis and testing algorithms (3 weeks)
  - Logic optimization and layout optimization
  - Fault model, D algorithm and design for testing

Project Topics and Schedule

- Default projects (choose one by student):
  - Parallel programming of a routing algorithm
  - Implementing DSP algorithms on FPGA
- Advanced or customized topics:
  - System reliability study using FPGA emulators for uP or networking
  - Logic reliability metrics for soft errors
  - Anti-cloning methods for FPGA-based systems
- Project assigned 4th or 5th week, and due by the last day of the quarter

References for this Course

- No textbook required
- Class wiki web-site
  - http://eda.ee.ucla.edu/EE201A
- Selected papers leading journals and conferences

Grading Policy

- Homework (maybe small programming projects) 70%
- Final project 30%

Who should take this course

- It is another course
  - Discuss wide scope of knowledge
  - But research (presentation + project) on your own focus
- For students who are motivated to
  - Learn timing, power/thermal, DFM for system and ckt designs
  - Understand CAD better
  - Become a CAD professional

Related, 201C to be offered in Winter

- Interconnect and timing modeling (3 weeks)
  - Interconnect extraction
  - Delay modeling and model order reduction
  - Project 1 (model order reduction in Matlab)
- On-chip timing and integrity (4 weeks)
  - Stochastic static timing and noise analysis for logic and on-chip interconnects
  - Process variation, stochastic timing, power and noise analysis
  - Stochastic power and thermal integrity
  - Project 2 (stochastic modeling in Matlab)
- Beyond-die signal and power integrity (3 weeks)
  - Chip-package co-design with power integrity
  - TSV modeling for 3D IC
  - Noise analysis for high-speed signaling and other analog components