Wei Wu

CONTACT

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EDUCATION

University of California, Los Angeles — Los Angeles, CA — Advisor: Prof. Lei He
Ph.D., Electrical Engineering Department — GPA:4.0/4.0 — Jan 2012 - Mar 2016

Beihang University — Beijing, China
Master of Science in Electrical Engineering — GPA:3.76/4.0 — Sep 2007 - Jul 2010
Bachelor of Science in Electrical Engineering — Rank: 2/31 — Sep 2003 - Jul 2007

INTERESTS

- **Machine Learning**: Deep Neural Nets and their Compact Equivalents, Applications
- **FPGA based Computing System**: Deep Learning on FPGA, Analog Circuit Emulation

INDUSTRY EXPERIENCE

Google Inc. — Mountain View, CA
Senior Software Engineer — Manager: Sunita Verma — Apr 2018 - present
Software Engineer — Apr 2016 - Mar 2018
Software Engineer Intern (Pittsburgh) — Manager: Shijie Zhang — Mar 2015 - Jun 2015

- Machine learning modeling for Google's payment risk (fraud detection) system.

IBM T.J. Watson Research Center — Yorktown Heights, NY
Research Intern — Manager: Jinjun Xiong — Jun 2015 - Sep 2015

- Knowledge transfer & network compression for deep learning inference on mobile devices.

Samsung Research America — San Jose, CA
Research Intern — Manager: Pranav Mistry — Jun 2014 - Sep 2014

- Think Tank Team: the next-gen wearable computing and indoor positioning system prototyping.

ACADEMIA EXPERIENCE

UCLA — Los Angeles, CA — Jan 2012 - Mar 2016
Graduate Student Researcher — Advisor: Prof. Lei He

- **Machine learning, statistical algorithms** and their applications on circuit reliability.
- **FPGA based Computing System**: Deep Learning on FPGA, Analog Circuit Emulation
- Parallel computing for CAD algorithms, large scale linear algebra on FPGA/multicore CPU/GPGPU.

Nanyang Technological University — Singapore, Singapore — Jan 2011 - Dec 2011
Research Staff — Advisor: Prof. Hao Yu, Prof. Lei He

- Parallel algorithms for frequency-domain circuit simulation.

Tsinghua University — Beijing, China — Jun 2010 - Jan 2011
Research Staff — Advisor: Prof. Yu Wang, Prof. Huazhong Yang

- **Parallel algorithms and architecture** of large-scale sparse matrix solver for circuit simulator.

SELECTED PROJECTS

ML Modeling and Infrastructure for Financial Risk System — Apr 2016 - present
Google Inc.

- Experimented various modeling technique (neural nets, boosting trees, etc.) for fraud detection.
- Developed a generative adversarial network (GAN) that generates synthetic data for ML modeling.

Deep Convolutional Neural Network on FPGA — Sep 2015 - Mar 2016
Design Automation Lab, UCLA

- Designed the hardware accelerator for deep convolutional network inference on FPGA.
- Developed the automated Verilog code generator for given network parameters.

Knowledge Transfer & Network Compression for Deep Learning Jun 2015 - Sep 2015
IBM T.J. Watson Research Center

• Conducted research related to deep neural networks and their more compact equivalents. (based on Caffe)
• Developed algorithms that generated artificial samples when we do not have sufficient training samples.

Reliability, Statistical Analysis Algorithms for Circuits Sep 2013 - Mar 2016
Design Automation Lab, UCLA

• **HSCS** [ISPD'16]: estimated yield rate by clustering failure examples and applying importance sampling.
• **REscope** [DAC'14]: predicted whether a design would be success/failure using a nonlinear classifier.
• **HDIS** [ASPDAC'14]: accurately calculated the yield rate of a circuit with more than 1000 variations.

Parallel sparse matrix solver on multi-core CPU and FPGA Jun 2010 - Jan 2011
NICS lab, Tsinghua University

• **NICSLU** http://nicslu.weebly.com: a multicore-CPU based parallel sparse LU solver, achieved up to 4.55x speedup over KLU (University of Florida), and outperformed SuperLU (UC Berkeley).
• **FPGA based parallel LU solver** [ARC'11]: a FPGA prototype of LU solver, achieved 0.5x-5.36x acceleration over CPU implementation with 200x less energy consumption.

SELECTED AWARDS AND HONORS

Best Paper Award Nomination	ISPD	2016
Electrical Engineering Departmental Fellowship	UCLA	2015, 2014
UCLA-PKU Joint Research Scholarship	UCLA, PKU	2013
Outstanding Undergraduate/Graduate Student	Beihang Univestiy	2007, 2010
1st Place Award in Undergrad Electronic Design Contest	Beijing	2006

SELECTED PUBLICATIONS

* The full list of about 20 publications are available at http://eda.ee.ucla.edu/wei/publications.

Journal Papers

1. Rahul Krishnan, **Wei Wu**, Srinivas Bodapati, and Lei He, "Accurate Multi-segment Density Estimation Through Moment Matching", **TCAD**, 2016
2. Wensheng Guo, Guowu Yang, **Wei Wu**, Lei He, and Mingyu Sun, "A Parallel Attractor Finding Algorithm Based on Boolean Satisfiability for Genetic Regulatory Networks", **PLOS ONE**, 2014.
3. **Wei Wu**, Fang Gong, Rahul Krishnan, Hao Yu and Lei He, "Exploiting Parallelism by Data Dependency Elimination: A Case Study of Circuit Simulation Algorithms", **D&T**, 2013.
4. Xiaoming Chen, **Wei Wu**, Yu Wang, Hao Yu and Huazhong Yang, "An EScheduler based Data Dependency Analysis and Task Scheduling for Parallel Circuit Simulation", **TCAS-II**, 2011

Conference Papers

1. **Wei Wu**, Yen-Lung Chen, Yue Ma, Chien-Nan Liu, Sudhakar Pamarti, Jing-Yang Jou, and Lei He, "Wave Digital Filter based Analog Circuit Emulation on FPGA", **ISCAS**, 2016.
2. **Wei Wu**, Srinivas Bodapati, and Lei He, "Hyperspherical Clustering and Sampling for Rare Event Analysis with Multiple Failure Region Coverage", **ISPD**, 2016. (**Nominated for Best Paper Award**)
3. **Wei Wu**, Peng Gu, Yen-Lung Chen, Chien-Nan Liu, Sudhakar Pamarti, and Lei He, "Toward Wave Digital Filter based Analog Circuit Emulation on FPGA", **FPGA**, 2015.
4. Yen-Lung Chen, **Wei Wu**, Chien-Nan Liu and Lei He, "Incremental Latin Hypercube Sampling for Lifetime Stochastic Behavioral Modeling of Analog Circuits", **ASPDAC**, 2015.
5. **Wei Wu**, Wenyao Xu, Rahul Krishnan, Yen-lung Chen, and Lei He, "REscope: High-dimensional Statistical Circuit Simulation towards Full Failure Region Coverage", **DAC**, 2014.
6. **Wei Wu**, Fang Gong, Gengsheng Chen, and Lei He, "A Fast and Provably Bounded Failure Analysis of Memory Circuits in High Dimensions", **ASPDAC**, 2014.

Patents

1. Yu Wang, **Wei Wu**, Xiaoming Chen, Huazhong Yang. "A Fast Sparse LU Factorization Algorithm for Sparse Matrix in Circuit Simulation", CN Patent: CN102142052 B.
2. Huazhong Yang, **Wei Wu**, Xiaoming Chen, Yu Wang. "A parallel Sparse LU Factorization Algorithm based on Elimination Graph for Circuit Simulation Applications", CN Patent: CN102156777 A.